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CLERK U.S. DISTRICT COURT
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BY FAX

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

(SOUTHERN DIVISION)

Koninklijke Philips Electronics N.V.; and Philips Lumileds Lighting Company LLC,

Plaintiffs,

v.

Seoul Semiconductor Company, Ltd.; and Seoul Semiconductor, Inc.,

Defendants.

CASE NO. SACV11-00356 AG (RNBx)

COMPLAINT FOR PATENT INFRINGEMENT AND DECLARATORY JUDGMENT OF PATENT NON-INFRINGEMENT AND INVALIDITY

DEMAND FOR JURY TRIAL

Plaintiffs Koninklijke Philips Electronics N.V. ("Philips") and Philips Lumileds Lighting Company LLC ("Lumileds," and together with Philips "Plaintiffs") allege upon knowledge as to themselves and their own actions, and upon information and belief as to all other matters, against Defendants Seoul Semiconductor Company, Ltd. ("SSC") and Seoul Semiconductor, Inc. ("SSI," and together with SSC the "Defendants") as follows:

Jurisdiction and Venue

1. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. The Court has subject matter jurisdiction over patent infringement claims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

2. This also is an action for a declaration of patent invalidity and patent non-infringement under the Declaratory Judgment Act, 28 U.S.C. §§ 2201, *et seq.*, and the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331, 1338(a), 1367, 2201, and 2202.

3. This Court has personal jurisdiction over each Defendant. On information and belief, each Defendant conducts and has conducted business within the State of California and within this District. Each Defendant, directly and/or through intermediaries—including subsidiaries, distributors, retailers, third party administrators, and/or others—offers for sale, sells, advertises, ships, distributes, and/or imports infringing light-emitting diode ("LED") products and related devices in the United States, the State of California, and within this District. On information and belief, each Defendant also offers for sale, sells, advertises, ships, distributes, and/or imports infringing LEDs that are incorporated into products that use LEDs that are sold in the United States, the State of California, and within this District. On information and belief, Defendants have established a distribution

chain to purposefully direct their infringing LED products to the State of California with the expectation that those products will be purchased by consumers in this District. Each Defendant, directly and/or through intermediaries, has committed the tort of patent infringement directly, jointly, contributorily, and/or by inducement within the State of California and within this District.

4. Venue is proper in this District pursuant to 28 U.S.C. §§ 1391(b) and (c), and 1400(b) because Defendants have committed acts of infringement within this District giving rise to this action, Defendants have and continue to conduct business in this District, including one or more acts of making, selling, using, offering for sale, and/or importing infringing products in this District, and at least one Defendant resides in this District.

5. An immediate, real, and justiciable controversy exists between Plaintiffs and SSC with respect to the validity and infringement of the claims of United States Patent No. 5,075,742, which, based on information and belief, SSC owns by assignment.

The Parties

6. Philips is a Dutch corporation having its registered office in Eindhoven, The Netherlands.

7. Lumileds is a Delaware limited liability company having a place of business at 370 West Trimble Road, San Jose, California 95131.

8. On information and belief, Defendant SSC is a company organized and existing under the laws of the Republic of Korea, having its principle place of business at 148-29, Gasan-dong, Geumcheon-gu, Seoul, South Korea. On information and belief, Defendant SSC also maintains a regular and established place of business in this District at 5856 Corporate Ave., Suite 240, Cypress, California 90630.

9. On information and belief, Defendant SSI is a California corporation

having its principle place of business in this District at 5856 Corporate Ave., Suite 240, Cypress, California 90630.

10. On information and belief, SSC wholly owns and controls SSI.

Background of the Patent Infringement Action

11. Lumileds is a worldwide leader in the field of LEDs. A pioneer in the use of solid-state lighting solutions for everyday purposes, Lumileds markets LED solutions designed for automotive applications, general lighting, portable applications, signs, traffic signals, and other segments. Lumileds also supplies core LED material and LED packaging, manufacturing billions of LEDs annually, and ranks as the producer of the world's brightest red, amber, blue, green, and white LEDs.

12. Lumileds, through its predecessors Hewlett Packard Company and Agilent Technologies, Inc.—and through its own work—is an innovator in the field of LEDs. Lumileds has expended many millions of dollars researching and developing such LEDs and their applications. These research and development efforts have made Lumileds a leader in LED technology, having been the first to combine the brightness of conventional lighting with the small footprint, long life, and other advantages of LEDs. The United States Patent and Trademark Office ("USPTO") has recognized Lumileds' and its predecessors' achievements by awarding numerous patents to Lumileds and its inventors for product and process innovation in LED technology.

13. Lumileds is a Philips subsidiary. Philips and Lumileds jointly own by assignment the Lumileds-developed patents.

14. On information and belief, Defendants are engaged in the business of supplying and importing LEDs into the United States, including LEDs that infringe one or more patents owned by Plaintiffs. On information and belief, Defendants have established a global distribution and sales network for selling and importing

infringing LEDs into the United States.

15. On information and belief, Defendants, directly and/or through intermediaries—including subsidiaries, retailers, distributors, third party administrators, and/or others—offer for sale, sell, advertise, ship, distribute, import, and/or otherwise introduce LED products into commerce within the United States, including, but not limited to, LEDs with brand, trade, product, and/or model names such as Acriche (*e.g.*, A2, A3, A4), Top View (*e.g.*, KWT801-S, SFT-722N-S), High Flux, Side View (*e.g.*, SWAA07, SWAA05), and Z-Power (*e.g.*, Z1, Z5, P4, P7, P9).

16. On information and belief, Defendants' distributors include such companies as Avnet, Inc., Digi-Key Corporation, and Mouser Electronics, Inc. On information and belief, one or more of the Defendants sells and/or offers to sell infringing LEDs to distributors—including Avnet, Inc., Digi-Key Corporation, and Mouser Electronics, Inc.—in the United States. Those distributors then offer to sell, sell, advertise, ship, distribute, import, and/or otherwise introduce infringing LED products in the State of California and in this District. On information and belief, one or more of the Defendants sell and/or otherwise provide infringing LEDs that are incorporated into products that use LEDs that are sold in the State of California and in this District.

17. By and through their actions in the State of California and this District, Defendants have infringed and continue to infringe directly, jointly, contributorily, and/or by inducement United States Patent Nos. 5,779,924; 6,274,924; 6,547,249; 6,590,235; and 6,717,353.

The Asserted Patents

<u>United States Patent No. 5,779,924</u>

18. Plaintiffs jointly own by assignment all right, title, and interest in and to United States Patent No. 5,779,924 ("the '9924 Patent"), titled "Ordered

Interface Texturing for a Light Emitting Device." The USPTO duly and legally issued the '9924 Patent on July 14, 1998. A true and correct copy of the '9924 Patent is attached as Exhibit A.

19. By virtue of their ownership of the '9924 Patent, Plaintiffs maintain all rights to enforce the '9924 Patent.

United States Patent No. 6,274,924

20. Plaintiffs jointly own by assignment all right, title, and interest in and to United States Patent No. 6,274,924 ("the '4924 patent"), titled "Surface Mountable LED Package." The USPTO duly and legally issued the '4924 Patent on August 14, 2001. A true and correct copy of the '4924 Patent is attached as Exhibit B.

21. By virtue of their ownership of the '4924 Patent, Plaintiffs maintain all rights to enforce the '4924 Patent.

United States Patent No. 6,547,249

22. Plaintiffs jointly own by assignment all right, title, and interest in and to United States Patent No. 6,547,249 ("the '249 Patent"), titled "Monolithic Series/Parallel LED Arrays Formed On Highly Resistive Substrates." The USPTO duly and legally issued the '249 Patent on April 15, 2003. A true and correct copy of the '249 Patent is attached as Exhibit C.

23. By virtue of their ownership of the '249 Patent, Plaintiffs maintain all rights to enforce the '249 Patent.

United States Patent No. 6,590,235

24. Plaintiffs jointly own by assignment all right, title, and interest in and to United States Patent No. 6,590,235 ("the '235 Patent"), titled "High Stability Optical Encapsulation and Packaging for Light-Emitting Diodes in the Green, Blue, and Near UV Range." The USPTO duly and legally issued the '235 Patent on July 8, 2003. A true and correct copy of the '235 Patent is attached as Exhibit D.

25. By virtue of their ownership of the '235 Patent, Plaintiffs maintain all

rights to enforce the ’235 Patent.

United States Patent No. 6,717,353

26. Plaintiffs jointly own by assignment all right, title, and interest in and to United States Patent No. 6,717,353 (“the ’353 Patent”), titled “Phosphor Converted Light Emitting Device.” The USPTO duly and legally issued the ’353 Patent on April 6, 2004. A true and correct copy of the ’353 Patent is attached as Exhibit E.

27. By virtue of their ownership of the ’353 Patent, Plaintiffs maintain all rights to enforce the ’353 Patent.

Background of the Declaratory Judgment Action

28. On information and belief, SSC is the owner by assignment of United States Patent No. 5,075,742 (“the ’742 Patent”), titled “Semiconductor Structure for Optoelectronic Components with Inclusions.” A true and correct copy of the ’742 Patent is attached as Exhibit F.

29. SSC has engaged in a course of conduct that shows a preparedness and willingness to sue on ’742 Patent.

30. On information and belief, in 2007, SSC sued LED manufacturers Nichia Corporation and Nichia America Corporation in the Eastern District of Texas for alleged patent infringement of the ’742 Patent. *See Seoul Semiconductor Co., Ltd. v. Nichia Corp.*, Case No. 9:07-cv-273 (E.D. Tex. Nov. 6, 2007).

31. On information and belief, on or about February 26, 2009, SSC issued a press release (a) claiming that “companies manufacturing or packaging blue, green, white, or UV light emitting devices made from the semiconductor indium gallium nitride may be subject to patents owned by Seoul,” (b) specifically referencing the ’742 Patent and Seoul’s belief that “the patent is fundamental to indium gallium nitride-based light emitting device technology,” and (c) threatening that “Seoul will also take the necessary steps to protect its intellectual property

rights against those who fail to respect its intellectual property rights."

32. On information and belief, on or about March 6, 2009, the head of SSC's research and development center, Sang Min Lee, stated in an interview that "I would like to emphasize that we also have patents that can be referred to as fundamental. One of them is our US patent 5,075,742 (patent 742). Just recently, the US District Court for Texas judged it impossible for LEDs that use InGaN in their active layers to avoid using the patent 742 because of their structural characteristics. This technology is also patented in Japan, Germany, the UK and France." Mr. Min Lee went on to threaten the entire LED community, stating that "From now on, we will be proactive in exercising our patent rights against the companies that infringe on our intellectual property rights."

33. On information and belief, on or about July 17, 2009, during the course of discussions between SSC and Philips, SSC wrote to Philips Lighting B.V.—a Philips subsidiary and Lumileds affiliate—specifically mentioning the patent "EP 437 385 B1 (registered in United States, Germany, Japan, France, and UK)," and stating that "it is [SSC's] strong belief that this patent is fundamental to the operation of light emitting diodes (LEDs) and covers all blue, white, green, and UV LEDs." On information and belief, both EP 437 385 B1 and the '742 Patent claim priority to the same French parent application.

34. Lumileds is in the business of manufacturing and selling LEDs in the United States and elsewhere.

35. The totality of SSC's conduct evidences that an actual controversy exists between SSC and Plaintiffs.

36. Plaintiffs reasonably apprehend that they will be improperly sued by SSC on the '742 Patent.

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First Cause of Action

Infringement of the ’9924 Patent

37. The allegations contained in Paragraphs 1 through 36 are incorporated here by reference with the same force and effect as if set forth in full.

38. On information and belief, Defendants have directly infringed, jointly infringed, actively induced the infringement of, and/or contributorily infringed one or more claims of the ’9924 Patent, including but not limited to Claim 1, in violation of 35 U.S.C. § 271 by (a) making, using, selling, offering for sale, and/or importing into the United States and this District products including, but not limited to, the Acriche (A2, A3, A4), Top View (KWT801-S; SFT-722N-S), Side View (SWAA07, SWAA05), and Z-Power (Z1) LEDs; and/or (b) actively inducing others to make, use, sell, offer for sale, and/or import into the United States and this District products including, but not limited to, the Acriche (A2, A3, A4), Top View (KWT801-S; SFT-722N-S), Side View (SWAA07, SWAA05), and Z-Power (Z1) LEDs, or products incorporating those infringing LEDs.

39. As a direct and proximate result of Defendants’ infringement of the ’9924 Patent, Plaintiffs have suffered monetary damages in an amount not yet determined, and will continue to suffer damages in the future unless Defendants’ infringing activities are enjoined by this Court.

40. Unless a permanent injunction is issued enjoining Defendants and their officers, agents, servants, employees, and those persons acting in active concert or participation with them from infringing the ’9924 Patent, Plaintiffs will be greatly and irreparably harmed.

41. To the extent that facts learned in discovery show that Defendants’ infringement is, or has been, willful, Plaintiffs reserve the right to request such a finding at trial.

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<u>Second Cause of Action</u>

Infringement of the ’4924 Patent

42. The allegations contained in Paragraphs 1 through 41 are incorporated here by reference with the same force and effect as if set forth in full.

43. On information and belief, Defendants have directly infringed, jointly infringed, actively induced the infringement of, and/or contributorily infringed one or more claims of the ’4924 Patent, including but not limited to Claim 1, in violation of 35 U.S.C. § 271 by (a) making, using, selling, offering for sale, and/or importing into the United States and this District products including, but not limited to, the Acriche (A3, A4) and Z-Power (Z5, P4, P7, P9) LEDs; and/or (b) actively inducing others to make, use, sell, offer for sale, and/or import into the United States and this District products including, but not limited to, the Acriche (A3, A4) and Z-Power (Z5, P4, P7, P9) LEDs, or products incorporating those infringing LEDs.

44. As a direct and proximate result of Defendants’ infringement of the ’4924 Patent, Plaintiffs have suffered monetary damages in an amount not yet determined, and will continue to suffer damages in the future unless Defendants’ infringing activities are enjoined by this Court.

45. Unless a permanent injunction is issued enjoining Defendants and their officers, agents, servants, employees, and those persons acting in active concert or participation with them from infringing the ’4924 Patent, Plaintiffs will be greatly and irreparably harmed.

46. To the extent that facts learned in discovery show that Defendants’ infringement is, or has been, willful, Plaintiffs reserve the right to request such a finding at trial.

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Third Cause of Action

Infringement of the ’249 Patent

47. The allegations contained in Paragraphs 1 through 46 are incorporated here by reference with the same force and effect as if set forth in full.

48. On information and belief, Defendants have directly infringed, jointly infringed, actively induced the infringement of, and/or contributorily infringed one or more claims of the ’249 Patent, including but not limited to Claim 1, in violation of 35 U.S.C. § 271 by (a) making, using, selling, offering for sale, and/or importing into the United States and this District products including, but not limited to, the Acriche (A2, A3, A4) LEDs; and/or (b) actively inducing others to make, use, sell, offer for sale, and/or import into the United States and this District products including, but not limited to, the Acriche (A2, A3, A4) LEDs, or products incorporating those infringing LEDs.

49. As a direct and proximate result of Defendants’ infringement of the ’249 Patent, Plaintiffs have suffered monetary damages in an amount not yet determined, and will continue to suffer damages in the future unless Defendants’ infringing activities are enjoined by this Court.

50. Unless a permanent injunction is issued enjoining Defendants and their officers, agents, servants, employees, and those persons acting in active concert or participation with them from infringing the ’249 Patent, Plaintiffs will be greatly and irreparably harmed.

51. To the extent that facts learned in discovery show that Defendants’ infringement is, or has been, willful, Plaintiffs reserve the right to request such a finding at trial.

Fourth Cause of Action

Infringement of the ’235 Patent

52. The allegations contained in Paragraphs 1 through 51 are incorporated

here by reference with the same force and effect as if set forth in full.

53. On information and belief, Defendants have directly infringed, jointly infringed, actively induced the infringement of, and/or contributorily infringed one or more claims of the '235 Patent, including but not limited to Claim 1, in violation of 35 U.S.C. § 271 by (a) making, using, selling, offering for sale, and/or importing into the United States and this District products including, but not limited to, the Acriche (A2, A3, A4) and High Flux LEDs; and/or (b) actively inducing others to make, use, sell, offer for sale, and/or import into the United States and this District products including, but not limited to, the Acriche (A2, A3, A4) and High Flux LEDs, or products incorporating those infringing LEDs.

54. As a direct and proximate result of Defendants' infringement of the '235 Patent, Plaintiffs have suffered monetary damages in an amount not yet determined, and will continue to suffer damages in the future unless Defendants' infringing activities are enjoined by this Court.

55. Unless a permanent injunction is issued enjoining Defendants and their officers, agents, servants, employees, and those persons acting in active concert or participation with them from infringing the '235 Patent, Plaintiffs will be greatly and irreparably harmed.

56. To the extent that facts learned in discovery show that Defendants' infringement is, or has been, willful, Plaintiffs reserve the right to request such a finding at trial.

Fifth Cause of Action

Infringement of the '353 Patent

57. The allegations contained in Paragraphs 1 through 56 are incorporated here by reference with the same force and effect as if set forth in full.

58. On information and belief, Defendants have directly infringed, jointly infringed, actively induced the infringement of, and/or contributorily infringed one

or more claims of the ’353 Patent, including but not limited to Claim 1, in violation of 35 U.S.C. § 271 by (a) making, using, selling, offering for sale, and/or importing into the United States and this District products including, but not limited to, the Acriche (A2, A3), High Flux, Side View (SWAA05), and Z-Power (Z1, Z5, P4, P7, P9) LEDs; and/or (b) actively inducing others to make, use, sell, offer for sale, and/or import into the United States and this District products including, but not limited to, the Acriche (A2, A3), High Flux, Side View (SWAA05), and Z-Power (Z1, Z5, P4, P7, P9) LEDs, or products incorporating those infringing LEDs.

59. As a direct and proximate result of Defendants’ infringement of the ’353 Patent, Plaintiffs have suffered monetary damages in an amount not yet determined, and will continue to suffer damages in the future unless Defendants’ infringing activities are enjoined by this Court.

60. Unless a permanent injunction is issued enjoining Defendants and their officers, agents, servants, employees, and those persons acting in active concert or participation with them from infringing the ’353 Patent, Plaintiffs will be greatly and irreparably harmed.

61. To the extent that facts learned in discovery show that Defendants’ infringement is, or has been, willful, Plaintiffs reserve the right to request such a finding at trial.

<u>Sixth Cause of Action</u>

Declaratory Judgment of Invalidity

62. The allegations contained in Paragraphs 1 through 61 are incorporated here by reference with the same force and effect as if set forth in full.

63. The ’742 Patent and each of every claim of the ’742 Patent are invalid because they fail to comply with the requirements of 35 U.S.C. §§ 1, *et seq.*, including, but not limited to, §§ 101, 102, 103, and/or 112.

64. Based on the foregoing, Plaintiffs seek a declaratory judgment that the

'742 Patent and each and every claim of the '742 Patent are invalid.

65. This is an exceptional case under 35 U.S.C. § 285, entitling Plaintiffs to an award of their attorneys' fees incurred in connection with this action.

Seventh Cause of Action

Declaratory Judgment of Non-infringement

66. The allegations contained in Paragraphs 1 through 65 are incorporated here by reference with the same force and effect as if set forth in full.

67. Plaintiffs' LED products have not infringed, do not infringe, and are in no way liable for any party's infringement of any valid and enforceable claim of the '742 Patent.

68. Plaintiffs seek a declaratory judgment that they have not infringed any valid and enforceable claim of the '742 Patent, either directly or indirectly, jointly, literally, or under the doctrine of equivalents, or in any way, willfully or otherwise.

69. This is an exceptional case under 35 U.S.C. § 285, entitling Plaintiffs to an award of their attorneys' fees incurred in connection with this action.

Prayer for Relief

WHEREFORE, Plaintiffs pray for:

a. A judgment that Defendants have directly infringed, induced the infringement of, and/or contributed to the infringement of, and directly infringe, induce the infringement of, and/or contribute to the infringement of the '9924 Patent, the '4924 Patent, the '249 Patent, the '235 Patent, and the '353 Patent;

b. A permanent injunction enjoining Defendants, their officers, agents, servants, employees, and those persons acting in active concert or participation with them or any of them from directly infringing, inducing the infringement of, or contributorily infringing the '9924

Patent, the ’4924 Patent, the ’249 Patent, the ’235 Patent, and the ’353 Patent;

c. An award of damages adequate to compensate Plaintiffs, together with pre-judgment and post-judgment interest, costs, and a judgment that the damages so adjudged be increased by the Court pursuant to 35 U.S.C. § 284;

d. That the ’742 Patent be declared invalid;

e. That the Court declare that Plaintiffs have not infringed, are not infringing, and are in no way liable for any party’s infringement, directly or indirectly, of any valid and enforceable claim of the ’742 Patent;

f. A judgment that this is an exceptional case and that Plaintiffs be awarded their attorneys’ fees, costs, and expenses incurred in this action pursuant to 35 U.S.C. § 285; and

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g. That the Court award Plaintiffs any other relief as the Court deems just and proper.

Dated: March 4, 2011

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Attorneys for Plaintiffs Koninklijke Philips Electronics N.V. and Philips Lumileds Lighting Company LLC

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b) and Local Rule 38-1, Plaintiffs request a jury trial on all triable issues.

Dated: March 4, 2011

MAYER BROWN LLP

By: ______________________

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Attorneys for Plaintiffs Koninklijke Philips Electronics N.V. and Philips Lumileds Lighting Company LLC

Exhibit A

US005779924A

United States Patent [19]

Krames et al.

[11] Patent Number: 5,779,924

[45] Date of Patent: Jul. 14, 1998

[54] **ORDERED INTERFACE TEXTURING FOR A LIGHT EMITTING DEVICE**

[75] Inventors: **Michael R. Krames**, Mountain View; **Fred A. Kish, Jr.**, San Jose, both of Calif.

[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **620,518**

[22] Filed: **Mar. 22, 1996**

[51] **Int. Cl.**[6] **B44C 1/22**

[52] **U.S. Cl.** **216/24**; 216/41

[58] **Field of Search** 216/2, 24, 41; 156/649.1, 654.1, 655.1, 659.11

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Primary Examiner—William Powell

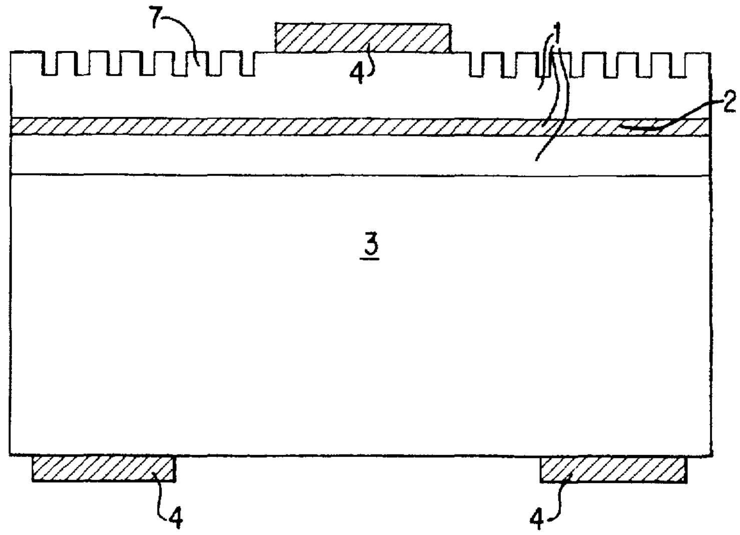
Attorney, Agent, or Firm—Pamela Lau Kee

[57] **ABSTRACT**

This method relates to the fabrication of semiconductor light-emitting devices having at least one ordered textured interface. Controlled interface texturing with an ordered pattern is provided on any or all interfaces of such a device to enhance light extraction from these interfaces and thus improve the performance of the device.

Ordered interface texturing offers an improvement in light extraction by increasing the transmission of total optical power from the device into the ambient. This improvement is possible because ordered interface texturing can provide: 1) a reduction in Fresnel losses at the interface between the device and the ambient and, 2) a change or increase in the angular bandwidth of light which may transmit power into the ambient. This latter effect may be thought of a change or increase in the escape cone at an interface. Both effects can result in an overall increase in total light extraction efficiency for the LED.

22 Claims, 16 Drawing Sheets



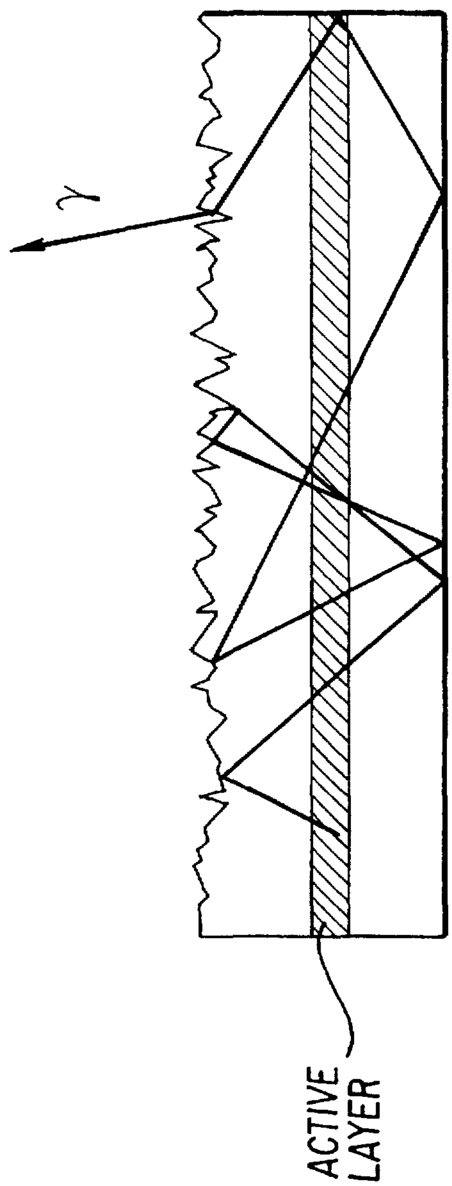


FIG. 1 (PRIOR ART)

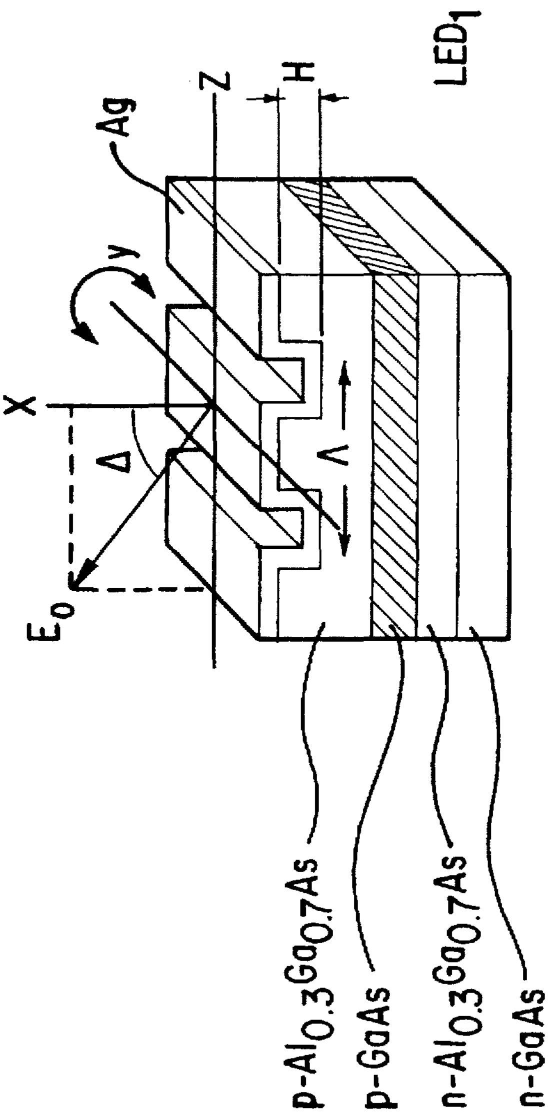


FIG. 2 (PRIOR ART)

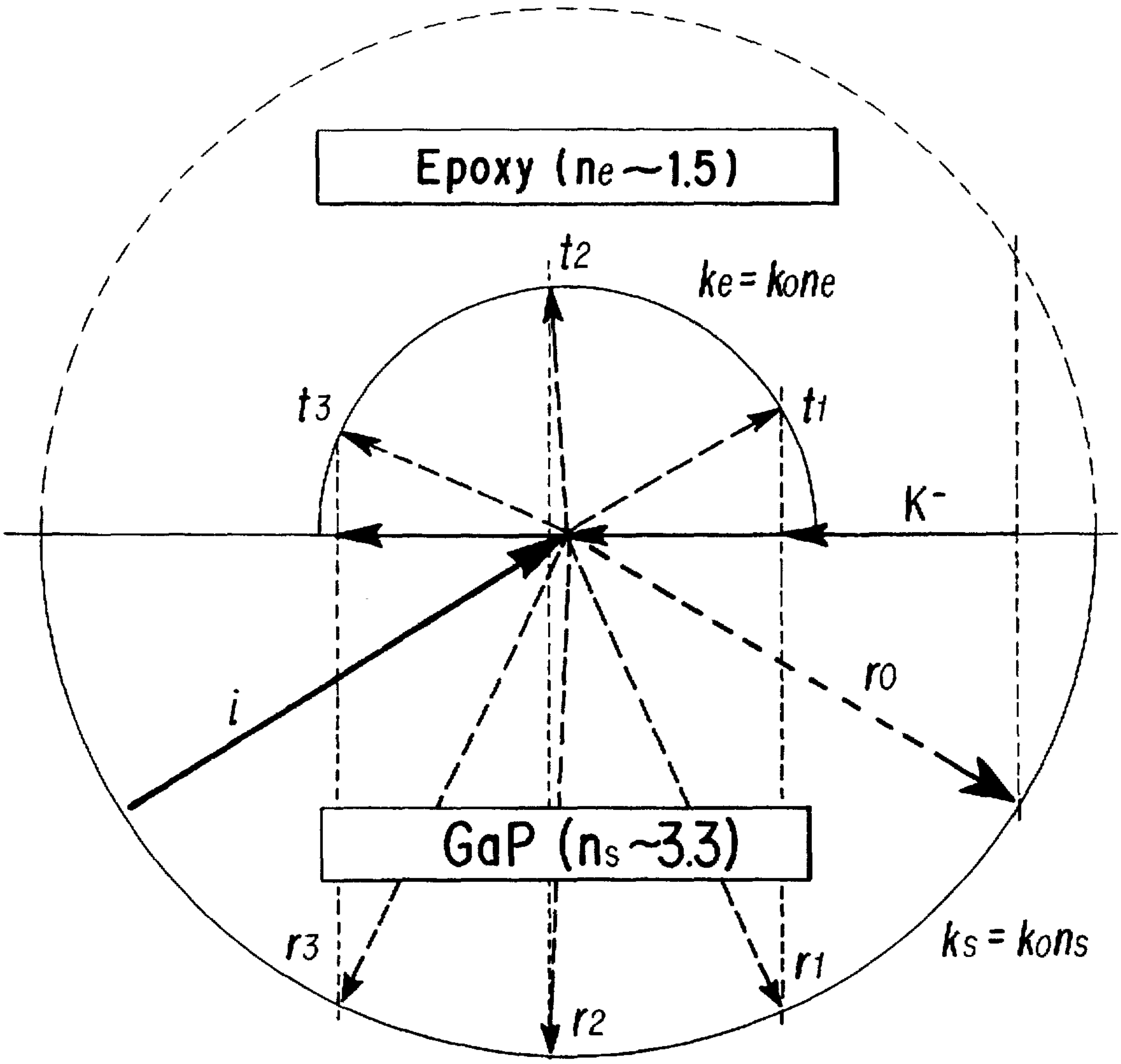


FIG. 3

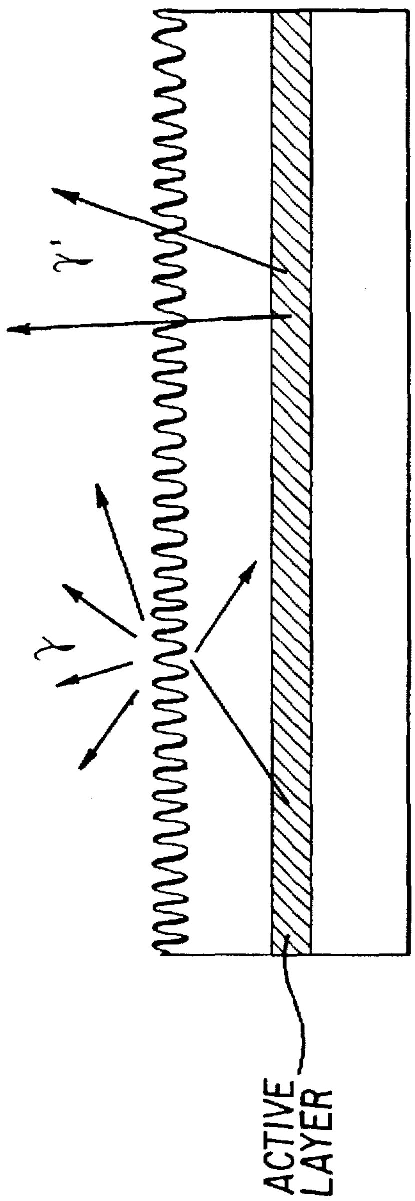


FIG. 4

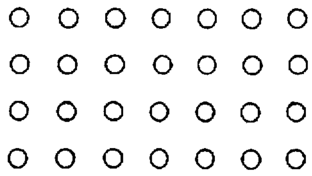


FIG. 5a

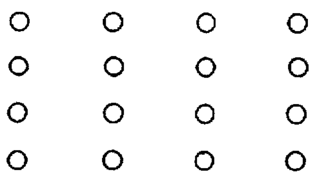


FIG. 5b

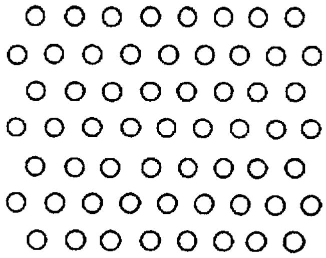


FIG. 5c

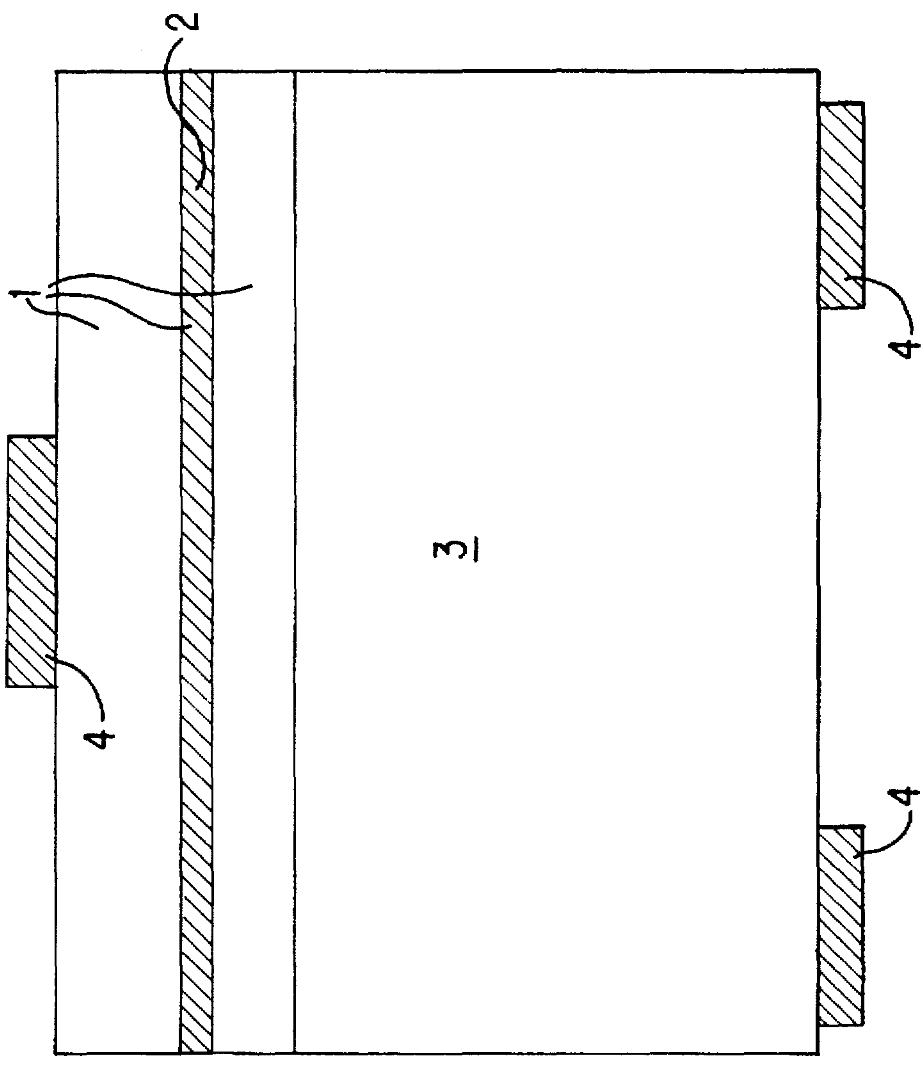


FIG. 6

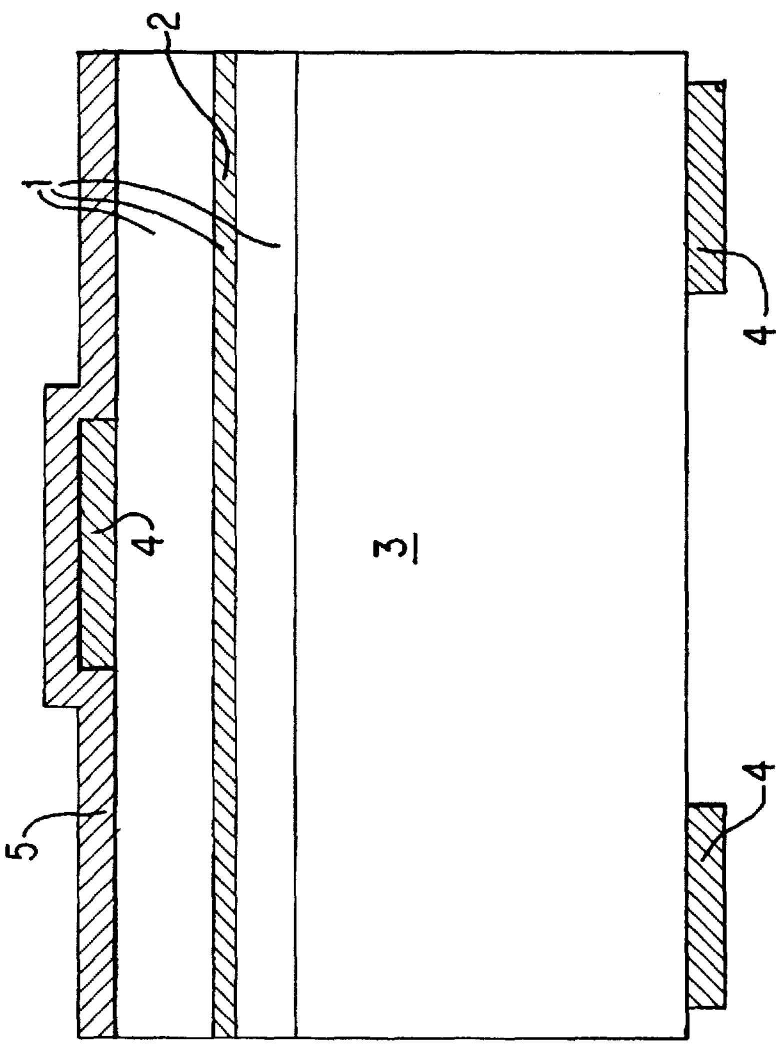


FIG. 7a

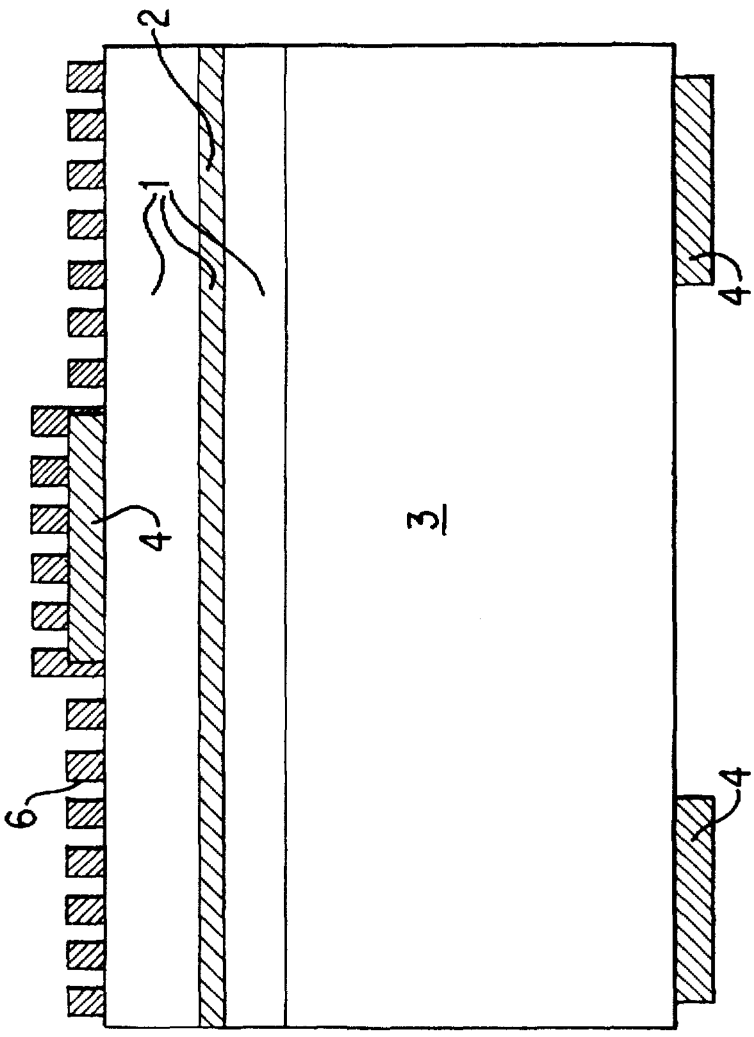


FIG. 7b

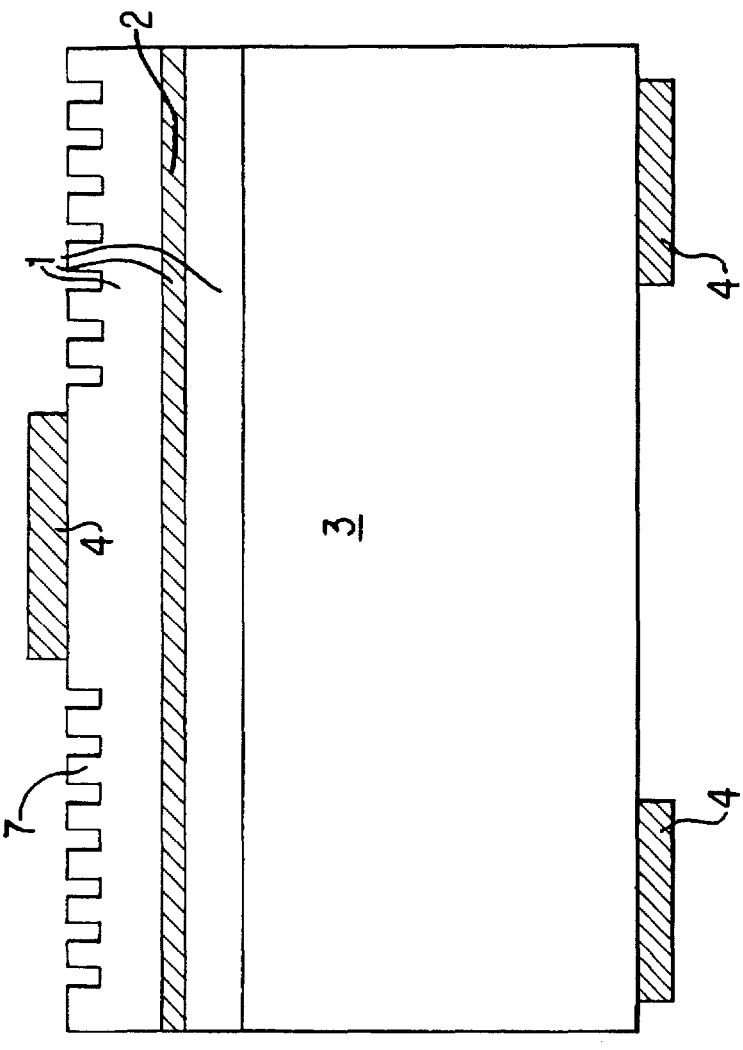


FIG. 7c

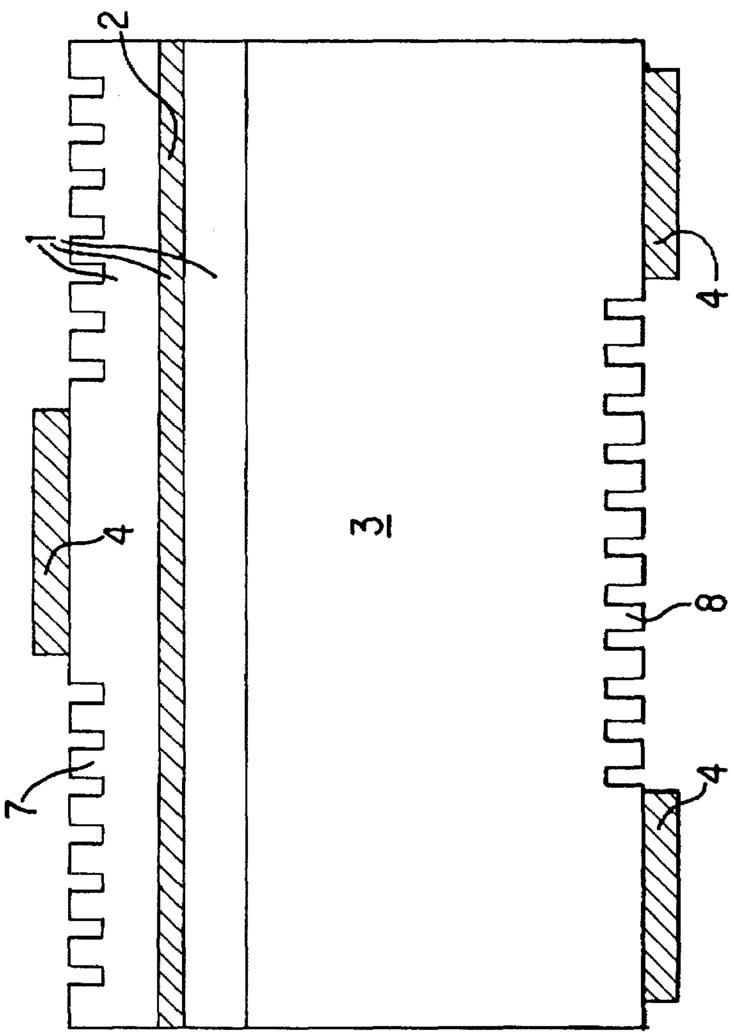


FIG. 8

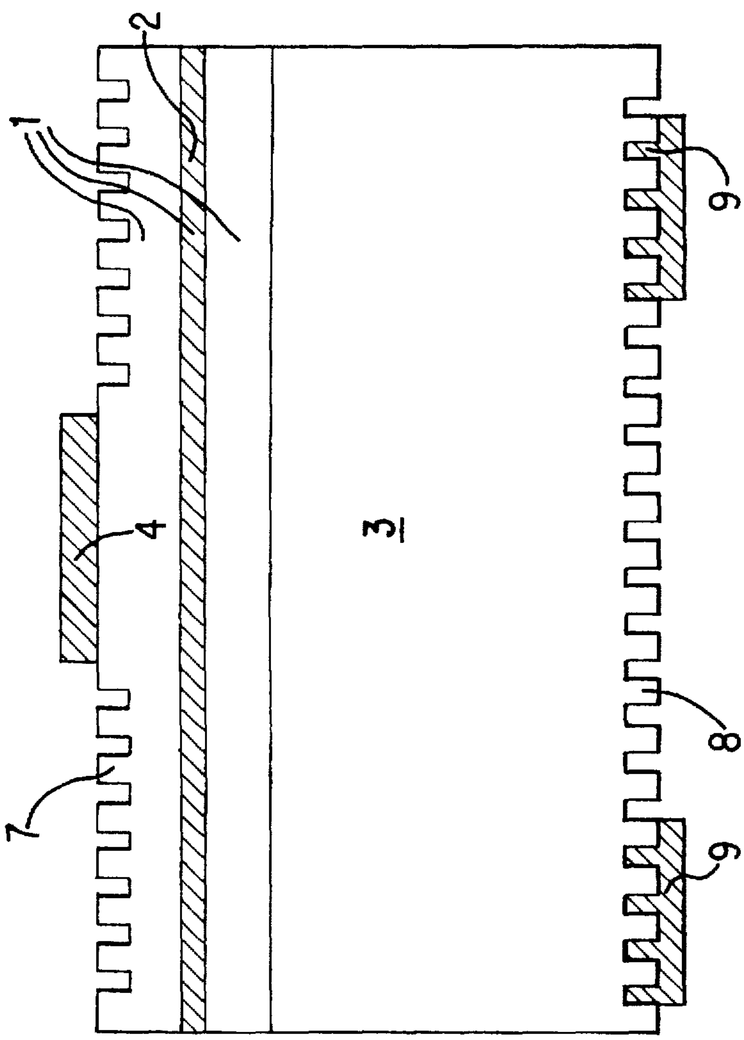


FIG. 9

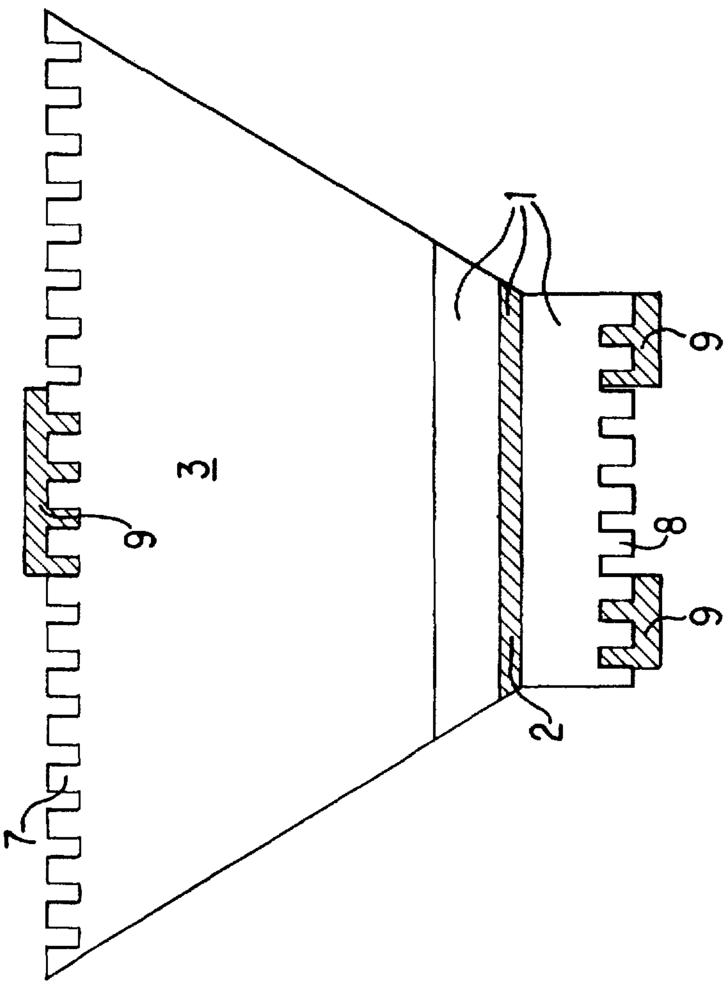


FIG. 10

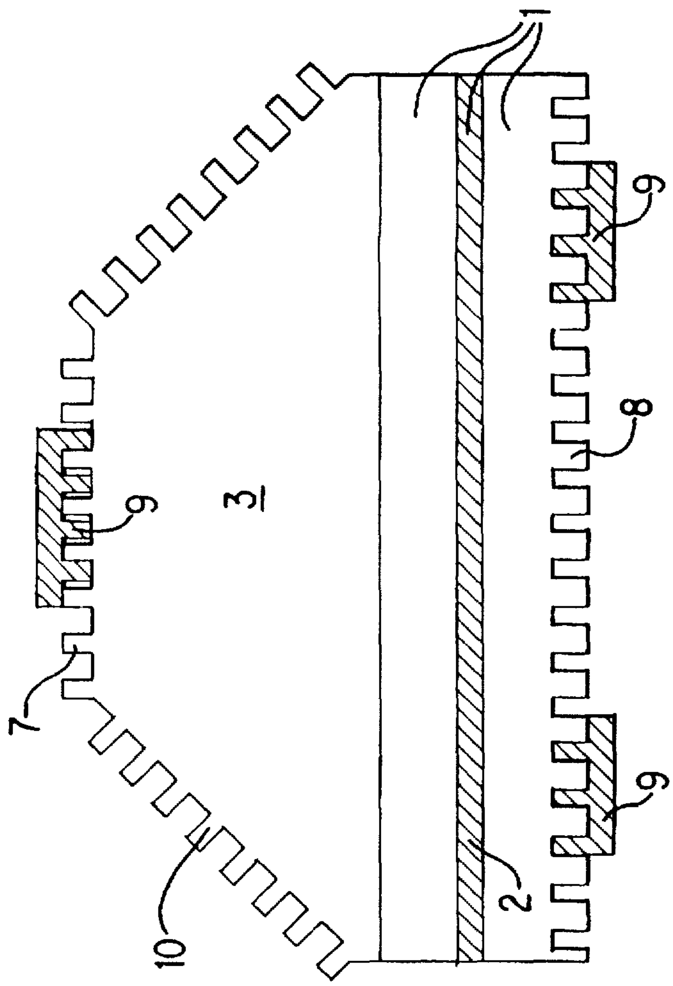


FIG. 11

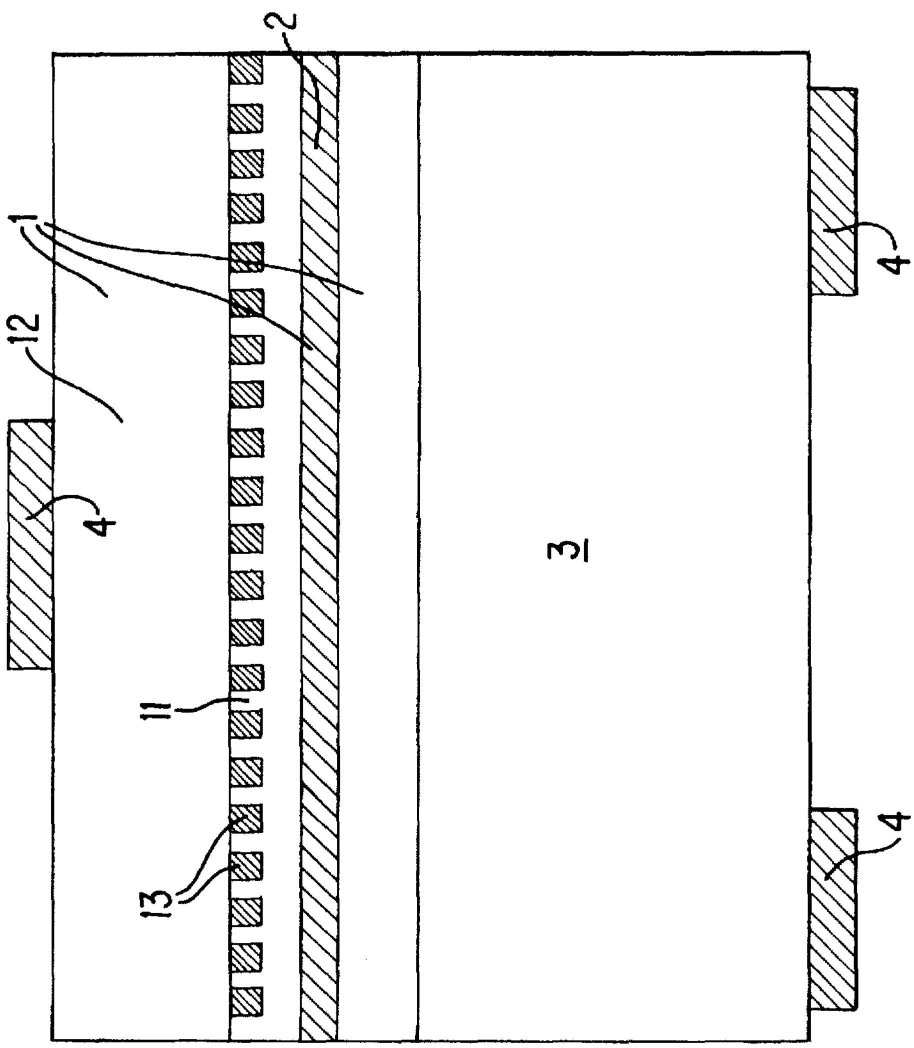


FIG. 12

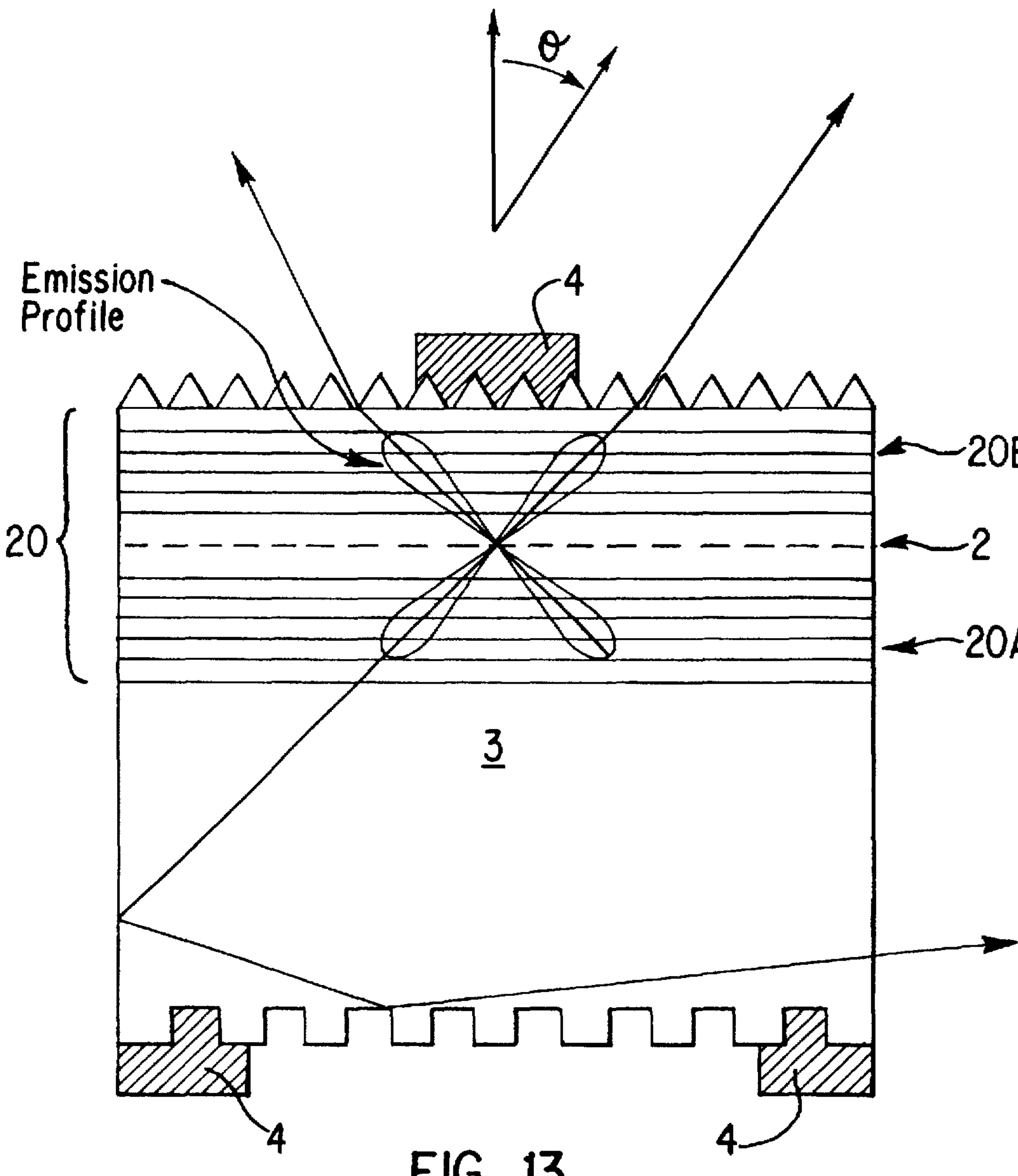


FIG. 13

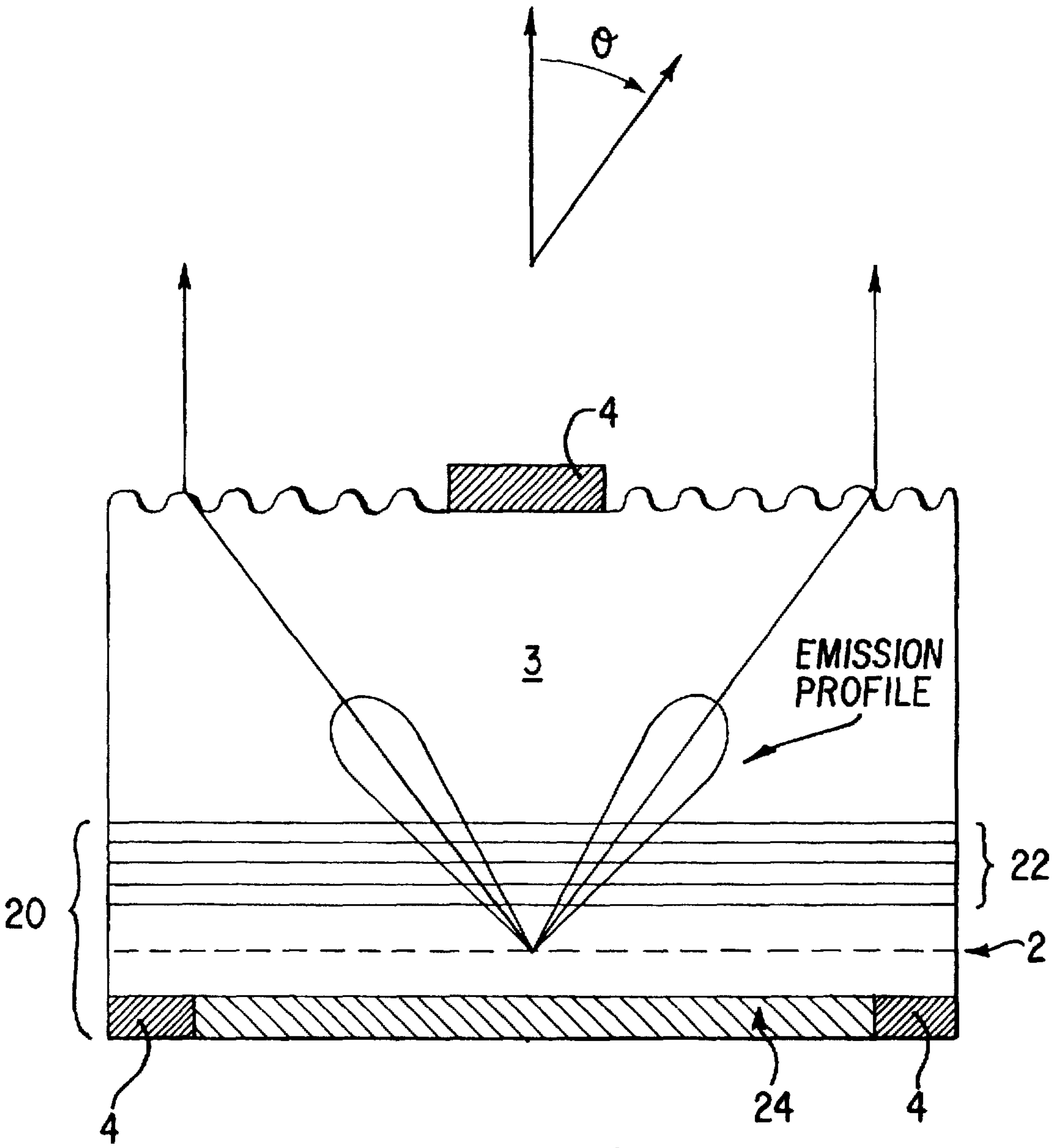


FIG. 14

ORDERED INTERFACE TEXTURING FOR A LIGHT EMITTING DEVICE

FIELD OF THE INVENTION

This invention relates to the manufacture of semiconductor light-emitting devices. In particular, the invention is directed towards improving light extraction from such devices.

BACKGROUND OF THE INVENTION

Light extraction from a semiconductor light-emitting device (LED) is typically limited due to the large optical refractive index, (n~2.2–3.8) of the semiconductor material relative to the surrounding ambient, typically air (n~1) or transparent epoxy (n~1.5). The amount of extraction depends heavily on the macroscopic geometry of the LED and the three-dimensional emission profile of light generated within the active region. The light emitting capability of the active region is defined by the structure of the surrounding materials such as the epitaxial layers, confining regions, etc..

The problem of light extraction from a semiconductor may be understood using an example from elementary electromagnetics: an electromagnetic plane wave that is incident from one medium (I) to another (II) must satisfy a phase-matching condition at the interface between the two media in order to be transmitted. Waves that do not meet this condition undergo total internal reflection (TIR) and do not propagate into medium II. For conventional semiconductor LEDs, when the speed of light in medium I is significantly slower than that of medium II, $n_I >> n_{II}$, and the interface between these media is planar or untextured, the phase-matching condition restricts transmission to rays which are incident from medium I at a narrow range of angles centered about normal incidence.

For a gallium-phosphide, GaP (n_1~3.3) interface with transparent epoxy (n_2~1.5), TIR occurs for angles of incidence, θ_i, greater than the critical angle, $\theta_c = \arcsin(n_2/n_1) = 27.0°$. Only light incident within the escape cone, $\theta_i < \theta_c$, will be transmitted. For an isotropic point-source of light within the GaP, the fraction of light emitted into the escape cone at the interface is only

$$\frac{1-\cos\theta_c}{2} = 5.5\%$$

of the available emitted light. When Fresnel losses at the interface are included, approximately 4.7% of the available emitted light will be transmitted through the interface into the epoxy. For a cubic-shaped device having a completely reflective bottom surface, no top contact, and no internal absorption, there are six such interfaces and the fraction of total emitted light escaping the LED is 6×4.7%=28.2%.

The effect described above severely limits the extraction efficiency of LEDs. Typical devices generate photons at the p-n junction that are emitted into a wide range of directions (nearly isotropic emission). As a result, a large percentage of emitted light rays may be incident at the device/ambient interface at large, oblique angles. If the interface is planar or untextured, these rays undergo TIR and will not escape upon first pass and are susceptible to absorption within the device.

Several methods for improving the light extraction from an LED have been proposed. One method is to change the macroscopic geometry of the LED to allow all or most of the light generated within the device to enter an escape cone at the interface with the ambient. A preferred shape is a spherical device with a point-source active region located at the center of the sphere. All of the emitted light strikes the interface at normal incidence and escapes into the ambient with minimal Fresnel loss and no TIR. Dierschke, et al. in Applied Physics Letters 19, 98 (1971) noted large improvements in extraction efficiency for a hemispherical device. Carr in Infrared Physics 6, 1 (1966) observed that other shapes, such as truncated cones, truncated pyramids, etc. also improve extraction efficiency. Macroscopic shaping methods are costly and have associated manufacturability issues such as inefficient material utilization and complicated fabrication processes and techniques.

Another approach is to use an anti-reflective coating on the top surface of the device. The coating results in reduced Fresnel losses for light rays near normally incident at the interface. However, since the thin film coating typically maintains planarity with respect to the semiconductor surface, the effective escape cone at the device/ambient interface is not increased and this technique provides a limited improvement in light extraction.

Another prior art approach is random texturing or roughening of the surfaces of the semiconductor LED, as shown in FIG. 1 and taught by Schnitzer, et al in Applied Physics Letters 63, 2174 (1993). A random surface texture randomizes the angular distribution of light rays within the device. This randomization increases the overall probability that light will enter an escape cone after many multiple passes through the device structure. Light emitted from the active region strikes the top surface many times before entering an escape cone. In Applied Physics Letters 62, 131 (1993), Schnitzer, et al. noted that very high total external quantum efficiencies (>72%) could be realized in optically pumped structures by the extraction of multiple-pass light. In this case, careful attention was made to minimize absorption within the device. In a practical, electrically pumped device, lossy or absorptive regions within the device (e.g., absorbing substrate, active layer, defects, doped regions, etc.) or at its extremities (e.g., metal contacts, die-attach epoxy, etc.) significantly reduce the intensity of multiple-pass light rays and thus limit the extraction efficiency gains. Thus, multiple-pass light extraction techniques provide only a modest improvement since in practical devices photons are not allowed many passes through the device before being absorbed.

Another prior art method is to couple photons into surface plasmon modes (within a thin film metallic layer on the top surface) which are subsequently out-coupled into radiated modes into the ambient. Kock, et al., in *Applied Physics Letters* 57, 2327 (1990) taught that a periodic surface structure, shown in FIG. 2, used in combination with a thin metal film to enhance the plasmon mode coupling can improve the quantum efficiency of LEDs. These structures rely on coupling photons from the semiconductor into surface plasmons in the metallic layer which are further coupled into photons which are finally extracted. The periodic structure is a one-dimensional ruled grating with shallow groove depths (<0.1 μm). The overall external quantum efficiencies are low for these devices (1.4–1.5%) likely due to inefficiencies of photon-to-surface plasmon and surface plasmon-to-ambient photon conversion mechanisms.

An efficient method for improving light extraction from a semiconductor by favorably altering the reflection and transmission properties of the semiconductor interfaces is highly desirable.

SUMMARY OF THE INVENTION

An LED having an ordered interface texture that is periodic in at least one dimension on any or all interfaces of an LED will improve the extraction of first-pass light. Patterning the interfaces is controlled to direct more light into the ambient without requiring many multiple passes through the device in order to escape. In addition, ordered interface texturing can reduce Fresnel loss for light rays escaping into the ambient. The regularly-patterned textured interface may have feature spacings comparable to a single wavelength of light in the device. The shapes and dimensions of the texture features are chosen to optimize light extraction for the application of interest.

An ordered, controlled interface texturing can result in light extraction gains by changing or increasing the effective escape cone at the device/ambient interface. Compared to macroscopic shaping techniques, ordered texturing involves simpler fabrication processes. Fresnel losses may be reduced in much the way reflections are minimized by anti-reflective coatings. Finally, light extraction gains are provided immediately for first-pass light and do not require that light make many multiple passes within the device structure before escaping.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a prior art example.

FIG. 2 illustrates another prior art example.

FIG. 3 illustrates a k-space diagram.

FIG. 4 illustrates a periodic texture along an interface.

FIGS. 5*a–c* illustrate ordering arrangements for the periodic texture.

FIG. 6 illustrates a conventional semiconductor light-emitting diode.

FIGS. 7*a–c* illustrate a method for texturing the top surface of an LED.

FIG. 8 illustrates a textured transparent substrate device.

FIG. 9 illustrates another embodiment for a textured transparent substrate device.

FIG. 10 illustrates another embodiment for a textured transparent substrate device.

FIG. 11 illustrates another embodiment for a textured transparent substrate device.

FIG. 12 illustrates another embodiment for a textured transparent substrate device.

FIG. 13 illustrates a resonant cavity LED chip, comprised of two DBR mirror stacks, with ordered textured interfaces.

FIG. 14 illustrates a resonant cavity LED chip, comprised of one DBR stack and one metal mirror, with an ordered textured interface on the transparent substrate surface.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The electromagnetic phase-matching conditions for a planar interface are altered when the interface is textured. An ordered textured pattern may be designed to increase first-pass light extraction and to increase power transmitted from a semiconductor into the ambient. The effects of ordered texturing of a semiconductor LED may be understood by referring to **FIG. 3** which illustrates a wave-momentum or k-space diagram for an interface of GaP (n_i~3.3) with a transparent epoxy (n_2~1.5). The two media at the interface are represented by their allowed wavenumber surfaces: half-circles of radii k_s and k_e, respectively, where $k=k_o n=2\theta n/\lambda_O$, n is the material index of refraction, and λ_O is the free-space wavelength of interest. Without texturing, a ray I from within the device is incident on the interface at a large, oblique angle greater than θ_c and does not satisfy the necessary phase-matching condition to allow transmission of power into the epoxy. Therefore, ray I undergoes total internal reflection and transmits its power into a reflected ray, r_o, back into the GaP.

In the present invention, the periodic spacing of the ordered texturing is chosen to be sufficiently small in order to alter the phase-matching condition at the interface. In **FIG. 3**, a periodic texture along the interface, with wave-number $K=2\pi/\Delta$ along the plane of incidence, imparts momentum to the incident ray and couples energy into the epoxy via transmitted modes t_1, t_2, and t_3. Energy is also transmitted into reflected modes r_1, r_2, . . . , back into the GaP. The periodic spacing and the shape and depth of the individual topical features of the texturing are chosen to favor power transfer into the transmitted modes.

Since light emission from the active layer is essentially three-dimensional, the interfacial texturing should preferably provide a wave-vector component along the plane of incidence for any azimuthal angle. Thus, the texturing arrangement is preferably two-dimensional along the interface, as opposed to one-dimensional like a simple ruled grating. The two-dimensional nature of the texture arrangement offers considerable flexibility. For example, the periodicity in two orthogonal directions along the plane of the interface are allowed to be different, in which case an anisotropic beam pattern may be generated. Such a beam pattern may be useful in certain applications.

The period of the ordered texturing should be short enough in order to transmit power into the ambient from rays that would normally undergo TIR at the interface, but not so short that it redirects significant amounts of light from near normally incident rays (which would otherwise escape) into TIR modes back into the device. For this same reason, "sharp" texture may be less desirable than "soft" texture features. Textures with "sharp" features are those that react with light to produce several higher-order diffracted modes. This increases the probability that significant amounts of light may be coupled into TIR modes back into the device. On the other hand, textures with "soft" features are those that redirect light primarily into lower-order diffracted modes, which should escape into the ambient in a proper texture design. A typical texture profile with "sharp" features might be a square-wave profile (with sharp corners), while an example of one with "soft" features might be a sinusoidal profile with a smooth variation along the plane of the interface.

For purposes of the present invention, an interface shall be defined as any region between dissimilar media, or any contiguous combination of such regions. Furthermore, an interface shall be specified by not only these dissimilar media, but also by its location and orientation relative to the rest of the device geometry.

FIG. 4 shows an LED with an ordered textured top surface. A light ray γ that would normally undergo TIR instead transmits power into the ambient upon reaching the top surface. This power transfer occurs upon first pass, and reduces the probability for optical loss at absorptive regions within or at the edges of the device. The light rays (γ') within the angular bandwidth defined by the critical angle of an untextured surface are also allowed to escape. The overall effect of the ordered texturing should be to match the active layer emission with the device geometry and surrounding ambient so as to result in a significant increase in total extraction efficiency.

Ordered texturing at the interface may also result in significantly reduced reflection losses for light rays transmitted from the device into the ambient. Gaylord et. al., in Applied Optics 25, 4562 (1986) noted that ordered surface textures will exhibit good anti-reflective characteristics over large angular bandwidths. The abruptness of the refractive index step between the device and the ambient is reduced to provide an intermediary region with an effective refractive index value graded between that of the device material and that of the ambient.

The texture pattern for optimal light depends upon the angular distribution of the light emission incident at the interface and upon the shape of the interface, both of which largely define the probability that a light ray strikes the interface at a given angle. If an LED active region consists of many (nearly) isotropic emitters, then the texture design must be such that light incident at a flat interface must be efficiently transmitted over a large range of angles, i.e., the textured-interface transmission must have a large angular bandwidth. If the emission from the active region is anisotropic, e.g. micro cavity emission, the ordered texturing should transmit efficiently within the angular bandwidth resulting from the anisotropic emission and the orientation of the interface(s).

The geometry or shape of the LED structure defines the angular light distribution that will strike any interface. In a cubic structure, a reasonable maximum angle of incidence at a top planar surface might be

$$\tan^{-1}\left(\frac{\sqrt{2a}}{h}\right),$$

where α is the width of the cube and h is the distance from the active layer to the top surface (e.g., α=10 mil, h=2 mil, θ_{max}=82°). However, light within the critical angle at the side surfaces will escape out the side surfaces, so $\theta_{max}=90-\theta_c=63°$ (if n_s=3.3, n_c=1.5). Thus, the ordered texturing should be designed to transmit efficiently over an angle bandwidth of $-63°<\theta<63°$.

In addition, the three-dimensional nature of the angular light distribution should be taken into account. For example, for an isotropic emitter below a planar interface, the percentage of light emitted for $|\theta|<20°$ is

$$\frac{1-\cos 20}{2}=3\%.$$

This is less than that emitted for $20°<|\theta|<40°$, which is

$$\frac{\cos 20-\cos 40}{2}=8.7\%.$$

For $40°<|\theta|<60°$, the percentage is

$$\frac{\cos 40-\cos 60}{2}=13.3\%.$$

The ordered texturing of the interface can be designed to transmit light more efficiently at the larger oblique angles at the expense of smaller ones, if desired. This may be important due to the trade-off generally inherent between diffraction efficiency and angular bandwidth in diffractive structures. As a result, it may be desirable to tune the grating for maximum extraction efficiency at large oblique angles (where the majority of light is incident).

The active layer and the surrounding structures can also effect the angular light distribution incident at a interface. For a thick, absorbing active layer, light emission at larger values of θ is less likely, due to the longer probable path

length within the absorbing active layer. The angular bandwidth of light incident at the top surface would be reduced relative to a thin active layer device or an active layer with high internal quantum efficiency (high probability of photon recycling).

In resonant cavity LED structures (see for example, Schubert et al., Science 265, 943 [1994]), the active layer and cavity design have strong effects in the angular light distribution. The active layer is positioned within a small vertical cavity defined by highly reflecting mirrors, which may be reflective metals, dielectric distributed-Bragg-reflector (DBR) stacks, or semiconductor DBR stacks. If the active layer is positioned at a cavity-field antinode and the DBR(s) are tuned to maximum reflectivity at normal incidence, much of the emitted light is clustered within a narrow range of angles about 0°. However, if the active layer is positioned away from a field antinode or the cavity is detuned, the angular light distribution is confined to a narrow range of off-axis angles. The percentage of total emitted light increases at more oblique angles (relative to the top surface) for a given angular light distribution, as stated earlier. If 80% of the upward emitted light could be contained narrow range of angles, for which an ordered textured interface might provide transmission at 60%, then the resulting upward extraction efficiency would be 0.8×0.6=48%.

The particular shapes, dimensions, and arrangement of the ordered texturing necessary for optimum performance are application dependent. A feature shape might be cone-like protuberance or indentation. A typical ordering arrangement might be a square, rectangular, or hexagonal-close-packed (HCP) array. These arrangements are illustrated in FIGS. *5a–c*, each of which show a plan-view of an ordered textured interface. The periodic spacings are preferably comparable to or less than a wavelength of light within the device. Cross-sectional profiles of the textured interface will exhibit peaks and valleys according to the protuberances or indentations, and the extent of any individual feature along the plane of the interface, as defined by its full-width-at-half-maximum (FWHM) height or depth, may also be comparable to several multiples or less than a wavelength of light within the device. The maximum height or depth of a protuberance or indentation may be comparable to one or several wavelengths of light within the device. The spacing of the ordered pattern is wavelength dependent. It is therefore critical to optimally alter the electromagnetic phase-matching condition at the interface to increase total power transmitted into the ambient. The extent and depth of the topical features of the pattern effects the efficiency of the phase condition alteration to transmit light. Also, the pattern may be chirped or otherwise interspersed with respect to its individual topical feature sizes and/or shapes in order to maximize total optical transmission and device performance.

As an example, consider visible-wavelength LEDs for which λ~400–700 nm. In this case, for the interface described in FIG. 4, the ordered texturing might exhibit a square or HCP arrangement. Features are potentially 0.1–0.9 μm in extent and on a spacing of 0.1–5.0 μm, with feature depths on the order of 0.2–15.0 μm. The period or spacing must be short enough to couple light at large oblique angles into the ambient. For typical visible-wavelength LED structures, the period will be less than 1.0 μm. The maximum depth of the features may be 0.5 μm or greater in order to achieve higher extraction efficiencies. Since the interfaces of interest are two-dimensional, the grating pattern must be two-dimensional, not one-dimensional like a simple grating.

A conventional semiconductor light-emitting device is shown in FIG. 6. It is comprised of semiconductor epitaxial layers (**1**) containing a p-n junction active region (**2**) on a substrate (**3**) with electrical contacts (**4**) provided for current injection. The electrical contacts as shown in FIG. **6** are made on both the top and bottom surfaces of the device, but it is possible to put both contacts on one side of the device to increase light extraction efficiency out the other side. In this latter case, the substrate (**3**) need not be conductive nor even be a semiconductor, provided that the epitaxial layers (**1**) may be grown upon or attached to the substrate in a satisfactory manner.

FIGS. 7*a–c* illustrate process flow steps for texturing the top surface of a light-emitting device. An electro-or photo-sensitive thin film (**5**) is applied to the top of the device (FIG. 7*a*). This film is exposed using electron-beam lithography, laser beam interference, or UV radiation, etc., and the desired pattern is developed (**6**) (FIG. 7*b*). After developing, the remaining masking pattern protects areas of the device material from a subsequent etching or milling process (e.g., ion milling, reactive ion etching, wet chemical etching, electrochemical etching, photochemical etching, chemical assisted ion beam etching, or combinations thereof, etc.) to transfer the desired pattern (**7**) into the device material, and the masking layer (**6**) is removed (FIG. 7*c*). The metal contact acts as a mask against the etching or milling process and is itself not textured. The photo-sensitive masking film (**5**) may be eliminated by utilizing a self-patterning etching technique (e.g., photo electrochemical etching, local laser melting and selective etching of melted regions, etc.), wherein the chemical, mechanical, or electrical state of the device material is altered according to the pattern and material is subsequently or simultaneously selectively removed to create an ordered textured interface.

Alternatively, a dielectric masking film or other thin film (metal, polymer, etc.) is applied before the photo-sensitive film. The type and thickness of this mask is selected to achieve the necessary etch ratio between the masking material and the device material in order to achieve deeply etched texturing which may be desirable for optimum light extraction. Additionally, this film may comprise part of the finished device since it is a suitable transparent window layer which may be textured to improve light extraction into the ambient. This may be useful if the index of the dielectric is greater than that of the ambient since the resulting structure will provide an increase in the effective escape cone out of the device.

FIG. **8** illustrates another embodiment wherein the top and back surfaces of a transparent substrate device are textured. Because the active region is typically heavily absorbing at the emission length, the back surface is textured (**8**) to redirect light that is reflected from the back surface towards the sides of the device to avoid a second pass through the active region and the top metal contact. The texturing of the top and bottom surfaces may be different since light is being redirected differently at either surface. In the case of a thin-active-layer device or one with high internal quantum efficiency (>80%), with little absorption occurring in that layer, the bottom surface texture may instead be designed to re-direct light into an escape angle at the top surface.

FIG. **9** illustrates an embodiment where the back metal contacts are put down on top of the textured surface. Alternatively, the front and/or back contacts may be applied outside the textured regions. In the case of FIG. **9**, the corrugation of the back metal contacts (**9**) offers increased surface-area for a given contact dimension and these contacts will exhibit reduced electrical resistance as compared to flat contacts of the same dimension. The corrugated contacts may be smaller in dimension relative to flat contacts for an equivalent contact resistance. They may be less absorbing than conventional flat contacts because the corrugation may act as an efficient reflective or diffractive barrier to incident light. Patterning within the contact regions may be optimized independently of the patterning on the rest of the device interfaces for increased TIR or Fresnel reflection in the contact regions in order to reduce absorption at the contacts. The optimal patterning in these regions may or may not be similar to the optimal patterning for other regions of the device.

FIG. **10** illustrates an embodiment that combines macroscopic shaping and interface texturing. Surface texturing is provided on either or both the top and the bottom of a truncated-cone-shaped light-emitting device. This transparent substrate device is mounted upside-down relative to the device of FIG. **9** to exploit the extraction gains provided by the thick cone-shaped window. Texturing may be performed on the back and designed to redirect light towards the sides of the device to avoid its passing through the absorbing active region. Alternatively, both the top and back metal contacts may be corrugated or "flat". The cone-shaped window helps to direct much of the light emitted from the active region towards the top surface at near normal incidence. This reduces the angular bandwidth of light incident at the top surface, and allows for a more efficient texturing design since, in general, there is a trade-off between diffraction efficiency and bandwidth in diffractive structures. The reverse case also holds, wherein an increase in the effective escape cone at the top surface (due to texturing) may allow relaxed design constraints in chip-shaping, leading to less costly designs. The top-surface texturing provides maximum light extraction at the wavelength and angles of interest, while the contact-area texturing may be designed to maximize reflectivity in order to reduce absorption at the metal contacts.

FIG. **11** depicts an embodiment that combines ordered interface texturing with chip-shaping. A truncated-pyramid shape is chosen for its similarity to a hemisphere. Texturing is provided on at least one of the exposed surfaces. Preferably, it is performed on the beveled sides (**10**) of the device as well as the top and bottom to reduce Fresnel loss and increase extraction efficiency. The patterning on the beveled surfaces (**10**) is best effected by non-contact patterning techniques such as photochemical etching using a laser. Additional variations may include some type of ordered texturing on the extreme edges of a device as well, to alter the emission patterns and/or to further enhance extraction efficiency.

FIG. **12** illustrates a device having an ordered textured interface near the active layer. A transparent window layer (**12**) is attached to the textured interface. This window layer may be provided to increase current spreading from the top contact for uniform injection into the active layer. The sandwiched interface between the window layer and the textured interface would normally consist of voids (**13**) but these voids may be filled with a suitable material (e.g., dielectric, semiconductor material, native oxide) before window layer attachment in order to provide structural integrity and to favorably modify the current pumping geometry of the device. The texturing and choice of "sandwiching" material should be chosen to optimize the electrical and optical characteristics of the device for the application of interest. The proximity of the ordered texturing to the active layer may result in improved light emission characteristics, wherein light is forced to emit upward from the active layer at near normal incidence to the top surface. In this latter case, the grating should be placed within ~5λ of the active region and preferably within less than ~2λ. The grating may also be placed below the active layer to redirect light upward or preferentially towards the edges of the LED.

FIG. **13** shows an LED with a resonant cavity (RC) structure (**20**) consisting of an active region (**2**) sandwiched between two DBR mirror stacks (**22A**, **22B**). The cavity is detuned to result in anisotropic emission from the active layer (off-axis emission). The ordered textured top surface is designed to efficiently couple this light out into the ambient. If the device is mounted on a transparent substrate, the bottom surface may be textured to preferentially direct light into escape cones at the sides of the device. Additionally, the textured interfaces may be instead embedded within the device at interfaces nearer the active region.

FIG. **14** shows an RCLED where one side of the cavity (**20**) is defined by a high-reflectivity metal mirror (**24**) and the other side is a DBR stack (**22**). The device is mounted with the (transparent) substrate on top. The cavity is detuned for off-axis emission and the top surface is textured to provide efficient coupling of the emission into the ambient. Additionally, the RCLED devices of FIGS. **13** and **14** may be shaped (in addition to texturing) to optimally out-couple light from the off-axis emission.

What is claimed is:

1. A light emitting device comprising:

a device that includes,

a substrate,

a p-n junction region having multiple layers, wherein subsets of the multiple layers have opposing polarity such that a p-n junction is formed, one of the layers being adjacent the substrate,

a transparent window layer, positioned adjacent the p-n junction region, and

electrical contacts, connecting to the p-n junction region, being operative to forward bias the p-n junction; and

a primary interface, positioned in the device, that is textured with repeated features in at least one selected direction, having an associated periodicity in each of the selected directions to increase light extraction and, within a period, having a cross-sectional profile having at least one peak and at least one valley.

2. A light emitting device, as defined in claim **1**, wherein the primary interface has repeated features in at least two selected directions that have identical periodicities.

3. A light emitting device, as defined in claim **1**, wherein the primary interface has repeated features that form a rectangular array.

4. A light emitting device, as defined in claim **1**, wherein the primary interface has repeated features that form a hexagonally close-packed pattern.

5. A light emitting device, as defined in claim **1**, wherein the maximum peak-to-valley depth is between 0.2 and 15 microns.

6. A light emitting device, as defined in claim **1**, wherein the periodicities have associated periods between 0.1 and 5.0 microns.

7. A light emitting device, as defined in claim **1**, wherein the valley is within 2 microns of the p-n junction region.

8. A light emitting device, as defined in claim **1**, wherein the peaks and valleys of the cross-sectional profile of the primary interface have full-width-at-half-maximum of 10–90% of one period of the textured arrangement.

9. A light emitting device, as defined in claim **1**, wherein a portion of the primary interface is electrically conducting.

10. A light emitting device, as defined in claim **1**, further comprising a metallic film at a portion of the primary interface.

11. A light emitting device, as defined in claim **1**, wherein at least some portion of the valley is filled in by a material having an index of refraction less than 2.0.

12. A light emitting device, as defined in claim **11**, wherein:

the material having an index of refraction less than 2.0 is a dielectric material; and

the device further including a layer of metal positioned over the dielectric material.

13. A light emitting device, as defined in claim **1**, further comprising:

N secondary interfaces (where N≧1), positioned in the device, wherein each of the secondary interfaces is textured with repeated features in at least one selected direction, having a periodicity in each selected direction to increase light extraction and, within any period, having a cross-sectional profile having at least one peak and at least one valley.

14. A light emitting device, as defined in claim **13**, wherein at least one of the N secondary interfaces and the primary interface have different cross-sectional profiles.

15. A light emitting device, as defined in claim **13**, wherein at least one of the N secondary interfaces and the primary interface are textured with different periodicities.

16. A method for manufacturing a textured interface for a light emitting device made by the steps of:

transferring at least one pattern to at least one interface of the device, wherein each pattern has repeating features having a periodicity in all directions and

removing some of the device material according to the pattern to create an interface that is textured with the repeating features having a periodicity in all of the directions, wherein the periodicity for at least two of the directions has an associated period between 0.1 and 5.0 microns.

17. A method, as defined in claim **16**, wherein the step of transferring the pattern comprises the steps of:

depositing a layer of photoresist over the interface of the device;

exposing a portion the layer of photoresist to create the pattern; and

removing the unpatterned regions of photoresist to create the masking layer.

18. A method, as defined in claim **16**, wherein the transferring the pattern comprises the steps of:

depositing a layer of dielectric material over the interface of the device;

depositing a layer of photoresist over the layer of dielectric material;

exposing a portion of the layer of photoresist to create the pattern;

removing the unpatterned regions of photoresist; and

etching the layer of dielectric material according to the pattern.

19. A method for manufacturing a textured interface for a light emitting device made by the steps of:

transferring at least one pattern to at least one interface of the device, wherein each pattern has repeating features having a periodicity in at least one selected direction;

removing some of the device material according to the pattern to create an interface that is textured with the repeating features having a periodicity in at least one direction; and

filling in the at least some portion of interface using a material having a refractive index less than 3.

20. A method for manufacturing a textured interface for a light emitting device made by the steps of:

transferring at least one pattern to at least one interface of the device, wherein each pattern has repeating features having a periodicity in at least one selected direction;

removing some of the device material according to the pattern to create an interface that is textured with the repeating features having a periodicity in at least one direction; and

applying electrical contacts to the interface.

21. A method, as defined in claim **16**, wherein the step of transferring the pattern comprises the step of modifying the state of the device material according to a pattern, wherein the pattern has repeating features having a periodicity in at least one direction.

22. A method, as defined in claim **21**, wherein the step of modifying and the step of removing are performed simultaneously.

* * * * *

Exhibit B

US006274924B1

(12) **United States Patent**
Carey et al.

(10) **Patent No.: US 6,274,924 B1**
(45) **Date of Patent: Aug. 14, 2001**

(54) **SURFACE MOUNTABLE LED PACKAGE**

(75) Inventors: **Julian A. Carey**, Sunnyvale; **William D. Collins, III**, San Jose; **Ban Poh Loh**, San Jose; **Gary D. Sasser**, San Jose, all of CA (US)

(73) Assignee: **LumiLeds Lighting, U.S. LLC**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/187,547**

(22) Filed: **Nov. 5, 1998**

(51) **Int. Cl.**[7] **H01L 23/495**
(52) **U.S. Cl.** **257/676**; 257/98
(58) **Field of Search** 257/98, 99, 431, 257/676

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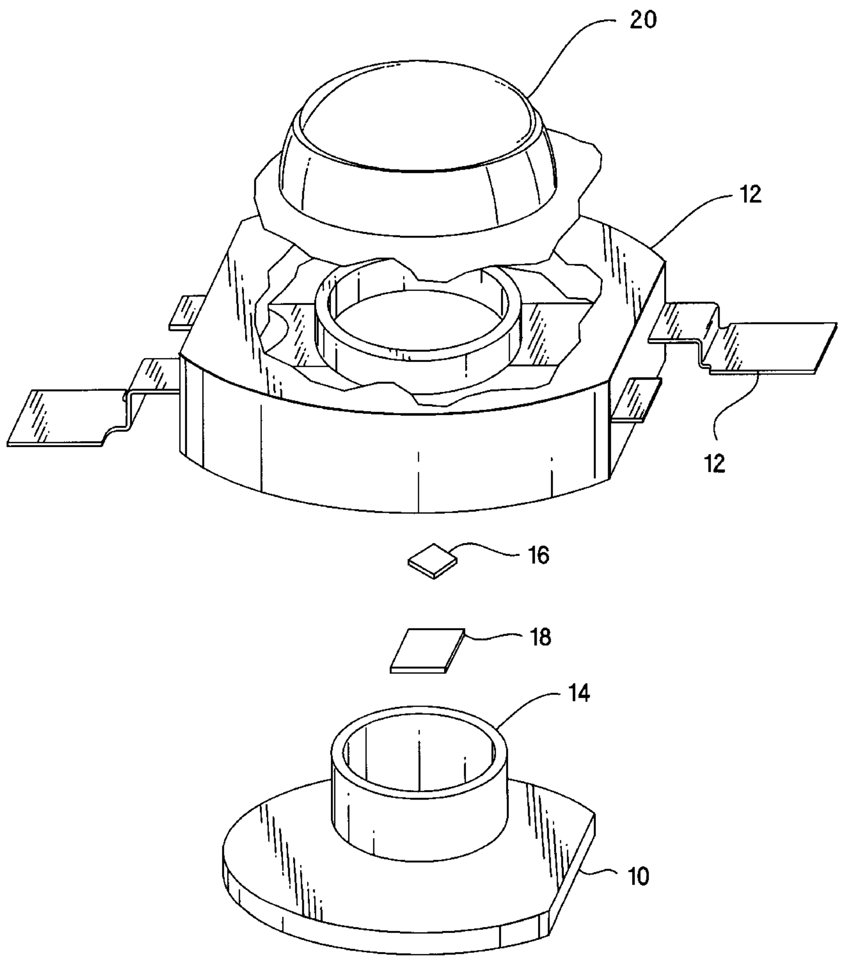
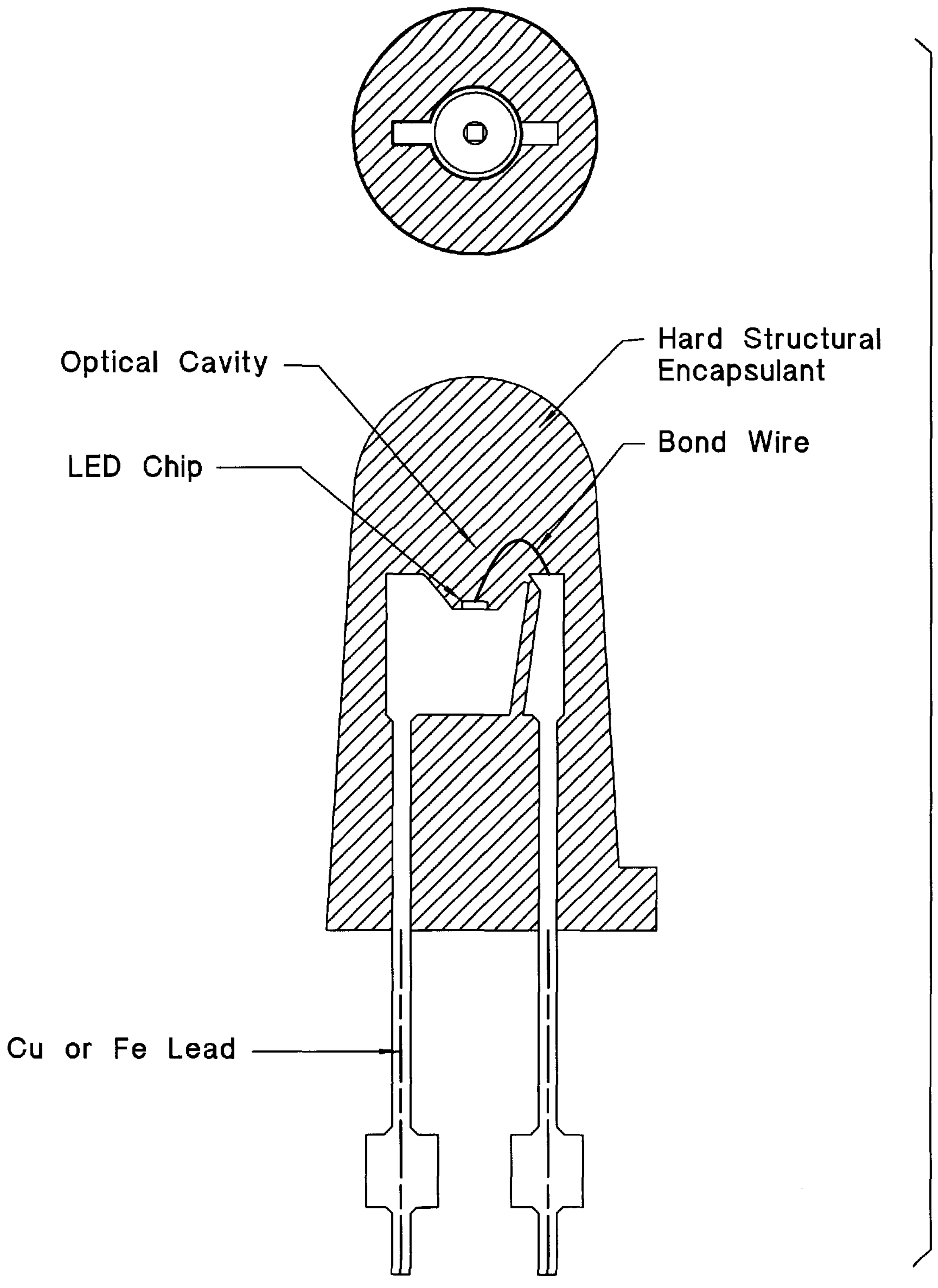
Primary Examiner—Roy Potter
(74) *Attorney, Agent, or Firm*—Skjerven Morrill MacPherson LLP; Brian D. Ogonowsky

(57) **ABSTRACT**

An LED package includes a heat-sinking slug that is inserted into an insert-molded leadframe. The slug may include an optional reflector cup. Within this cup, the LED and a thermally conducting sub-mount may be attached. Wire bonds extend from the LEDs to metal leads. The metal leads are electrically and thermally isolated from the slug. An optical lens may be added by mounting a pre-molded thermoplastic lens and a soft encapsulant or by casting epoxy to cover the LED or by a cast epoxy lens over a soft encapsulant.

28 Claims, 2 Drawing Sheets





(Prior Art)

Figure 1

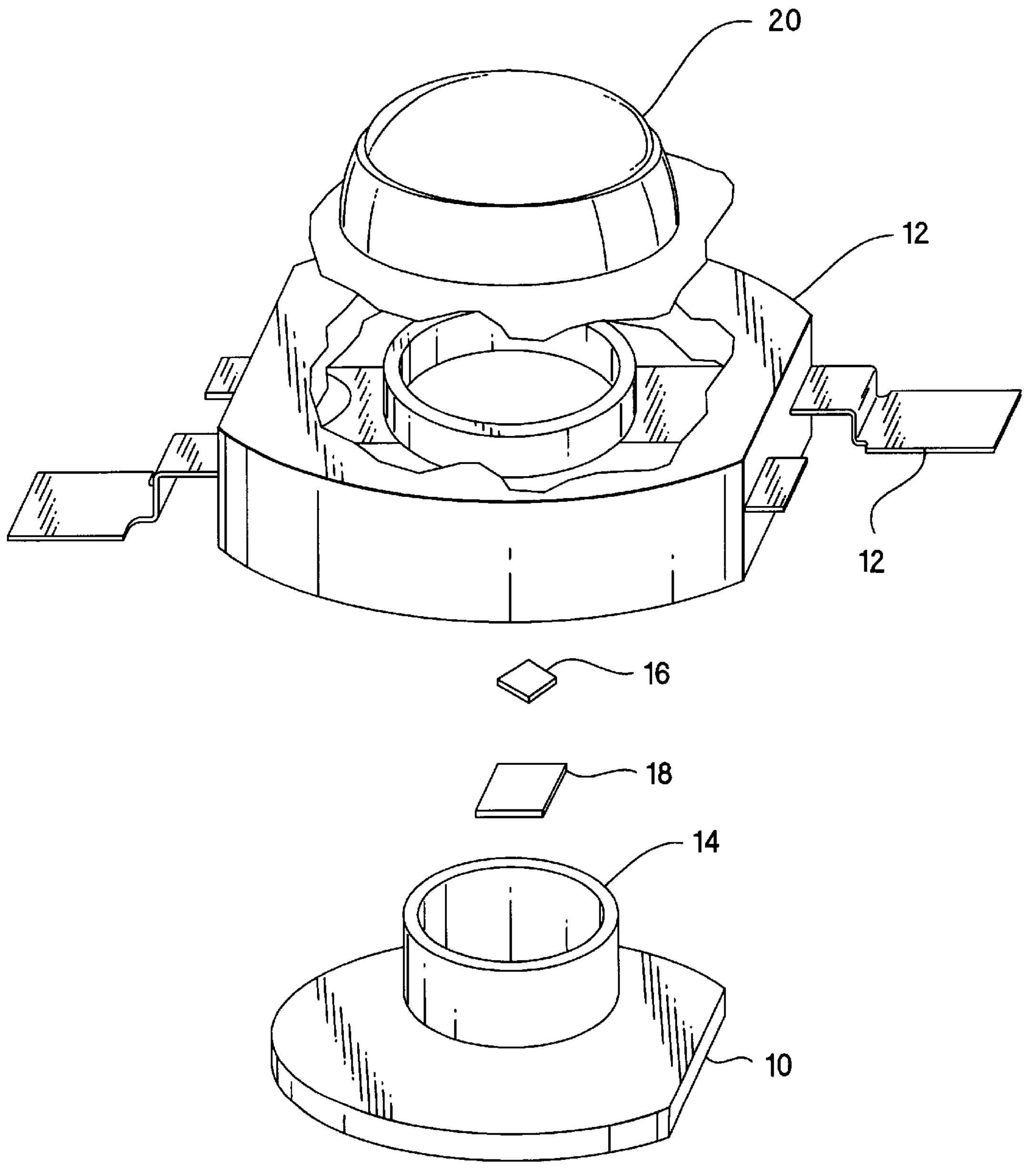


Figure 2

SURFACE MOUNTABLE LED PACKAGE

FIELD OF THE INVENTION

The present invention is directed towards the field of packaging light emitting diodes.

BACKGROUND OF THE INVENTION

Most light emitting devices (LEDs) emit incoherent light. One performance measure of an LED is photometric efficiency, e.g. the conversion of input energy into visible light. Photometric efficiency is inversely proportional to the junction temperature of the LED. A major concern of the LED package designer is keeping the die cool to provide good overall performance.

For low power LEDs, e.g.≦200 mW, or die with small area, a large optical cavity size limits the ability to meet the desired reliability conditions. A smaller than optimum cavity size reduces the light extraction efficiency, e.g. the amount of generated light that exits the device. The prior art packages e.g. T1-3/4 and SnapLED, use cast epoxy as the hard encapsulant. The cast epoxy provides both optical and structural functionality. A prior art package design for an LED is shown in FIG. **1**. The die is seated at the base of the optical cavity. A hard encapsulant, e.g. rigid unfilled epoxy, fills the optical cavity. Because the die, the optical cavity, and the encapsulant have different thermal coefficients, they expand and contract at different rates during operation. This places a high mechanical stress on the LED. In addition, the prior art packages lack thermal isolation between the electrical and the thermal paths because the electrical leads are the primary thermal paths. As a result, the packaged die are subject to thermal stresses from the temperature cycling, especially during assembly into end products.

These problems are exacerbated as the die increases in area or input power. Because a device having a larger junction area, e.g.>0.25 mm^2 requires a larger optical element than a small die, e.g.<<0.25 mm^2, to provide comparable light extraction efficiency, a large optical cavity is necessary. The mechanical stress applied to the LED increases with the volume of the encapsulant. In addition, the stress increases as the packaged LED is exposed to temperature cycling and high moisture conditions. The accumulated mechanical stresses reduce the overall LED reliability.

Since prior art packages use their electrical leads as primary thermal paths, the high thermal resistance of these paths combined with the high thermal resistance of the external system creates high junction temperatures, when power dissipation increases, e.g.≧200 mW. High junction temperature contributes to accelerating the irreversible loss of photometric efficiency in the LED chip and also accelerates processes that contribute to the failure of mechanical integrity of the LED package.

None of the available LED packages provide reliable optically efficient operation for applications approaching LED average input power of 0.2 W, especially when operating under high (>35%) duty factors or long pulse widths>1 second.

SUMMARY OF THE INVENTION

The present invention is an LED package that has separate optical and structural functionality. A heat-sinking slug is inserted into an insert-molded leadframe. The insert-molded leadframe consists of a patterned metal part, overmolded by a filled plastic material to provide structural integrity. The slug may include an optional reflector cup. The LED die is mounted directly or indirectly via an electrically insulating and thermally conducting sub-mount to the slug. Bond wires extend from the LEDs to metal leads that are electrically and thermally isolated from the slug. An optical lens may be added by mounting a pre-molded optically transparent thermoplastic lens and a soft optically transparent encapsulant or by casting an optically transparent epoxy to cover the LED or by a cast optically transparent epoxy lens over soft optically transparent encapsulant. The soft optically transparent encapsulant is a soft material that provides low stress or cushioning to the LED die.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a prior art LED assembly.

FIG. **2** illustrates an embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **2** illustrates an embodiment of the present invention, an LED package that has decoupled optical and structural functionality. A heat-sinking slug **10** is placed into an insert-molded leadframe **12**. The insert-molded leadframe **12** is a filled plastic material molded around a metal frame that provides an electrical path. The slug **10** may include an optional reflector cup **14**. The light-emitting diode (LED) die **16** is mounted directly or indirectly via a thermally conducting sub-mount **18** to the slug **10**. Bond wires extend from the LED **16** and the submount **18** to metal leads on leadframe **12** that are electrically and thermally isolated from the slug **10**. An optical lens **20** may be added by mounting a pre-molded thermoplastic lens and an encapsulant (not shown) or by casting epoxy to cover the LED or by a cast epoxy lens over the encapsulant (not shown). The encapsulant is preferably a soft material that provides low stress or cushioning to the LED die. Because the LED die is thermally coupled to the heatsinking slug, the die can be maintained at a junction temperature lower than conventional packages. The lower operating temperature maintains reliability and performance under high-power conditions because the die is not subject to high thermal stress.

The heatsinking slug **10** is isolated thermally from the leadframe **12**. If an insulating submount **18** is used, then the slug **10** is electrically insulating. Hence, the slug **10** may be attached to an external heat sink (not shown) with minimal thermal resistance to prevent a thermal build-up within the package. The massive slug **10** provides a low thermal resistance path to conduct heat away from the LED die **16**. While the preferred embodiment employs a copper slug, other suitable materials include thermally conductive materials such as diamond, silicon, aluminum, molybdenum, aluminum nitride, aluminum oxide, beryllia or composites and alloys thereof. Alternatively, composites of molybdenum-copper and tungsten-copper may be used. Suitable thermally conductive materials include pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

The submount **18** provides a thermally conducting path and thermal expansion buffer between the slug material and the LED die. It preferably has a thermal coefficient of expansion comparable to the LED die. The submount **18** may be electrically conducting or insulating. The submount **18** may be made of a thermally conductive material selected from the group consisting of pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

The insert-molded leadframe **12** is a patterned metal part that provides high electrical conductivity but only low thermal conductivity. The leadframe may be over-molded by a plastic structural part that provides low thermal conductivity and electrical insulation. The insulating part of the leadframe is a filled plastic material that provides structural integrity. The strong plastic body provides the structural integrity of the package and has hardness on the order of Durometer Shore 50-90 D. Separating the optical and structural functions allows the package to maintain optical quality without compromising its structural integrity.

The encapsulant is a soft optically transparent material having a refractive index>1.3, e.g. silicone, liquid or gelatinous optical compound, and fills the optical path between an LED die **16** and the optical lens **20**. The soft optically transparent material protects the LED die **16**. The soft encapsulant has a hardness less than Durometer Shore 10 A.

The optional reflector cup **14** may be made of thermally conductive materials that have been plated for reflectivity. The optional reflector cup **14** may be made of thermally conductive materials that have been coated for reflectivity. Similar to the slug **10**, suitable thermally conductive materials from which the reflector cup may be composed include materials such as silver, copper, aluminum, molybdenum, diamond, silicon, alumina, aluminum nitride, aluminum oxide, and composites thereof. Unlike the slug, the reflector cup walls may also be made of thermally insulating materials, e.g. plastics with reflective coatings.

Alternatively, the walls may be formed by the un-coated surface of the optical plastic lens shell arranged such that the exterior optical surface presents a reflective surface by Total Internal Reflection CIMR) by virtue of the angle of incidence to the light rays from the chip to the surface and a high to low refraction index step change at the surface. The refraction index step change is≧0.3.

In many preferred embodiments the cup has been coated with silver. Other reflective material coatings may be used such as aluminum, gold, platinum, dielectric coated metals such as aluminum, silver, gold, or pure dielectric stacks.

We claim:

1. A light emitting die assembly comprising:

metal leads;

an insulating body attached to the metal leads, the insulating bode having a cavity;

a heat sink of a first thermally conductive material, the heat sink separate from the metal leads, connected to the insulating body and positioned relative to the cavity for being thermally coupled to a die; and

a lens, positioned relative to the cavity for transmitting light emitted from the die.

2. An assembly, as defined in claim **1**, further including a submount of a second thermally conductive material, connected to the heat sink.

3. An assembly, as defined in claim **2**, wherein the second thermally conductive material is selected from the group consisting of pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

4. An assembly, as defined in claim **1**, wherein the first thermally conductive material is selected from the group consisting of pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

5. An assembly as defined in claim **1**, further comprising:

a die thermally coupled to the heat sink.

6. An assembly, as defined in claim **5**, further comprising an optically transparent material, encapsulating the die, having a hardness less than Shore 10A.

7. An assembly, as defined in claim **5**, further comprising a submount of a second thermally conductive material connected between the die and the heat sink.

8. An assembly, as defined in claim **7**, wherein the second thermally conductive material is selected from the group consisting of pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

9. An assembly, as defined in claim **5**, wherein the first thermally conductive material is selected from the group consisting of pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

10. An assembly, as defined in claim **5**, further comprising a reflector cup, positioned near the heat sink, having a reflective surface.

11. An assembly, as defined in claim **10**, wherein the reflective surface is selected from the group consisting of silver, aluminum, gold, silver with a dielectric coating, gold with a dielectric coating, and aluminum with a dielectric coating.

12. An assembly, as defined in claim **10**, wherein the reflective surface includes a dielectric stack.

13. An assembly, as defined in claim **10**, wherein the reflective surface includes at least one totally internal reflective surface formed by refractive index step changes>0.3.

14. An assembly, as defined in claim **1**, further comprising a reflector cup, positioned near the heat sink having a reflective surface.

15. An assembly, as defined in claim **14**, wherein the reflective surface is selected from the group consisting of silver, aluminum, gold, silver with a dielectric coating, gold with a dielectric coating, and aluminum with a dielectric coating.

16. An assembly, as defined in claim **14**, wherein the reflective surface includes a dielectric stack.

17. An assemble, as defined in claim **14**, wherein the reflective surface includes at least one totally internal reflective surface formed by refractive index step changes>0.3.

18. An assembly, as defined in claim **17**, wherein the reflector cup includes a material selected from the group consisting of silver, copper, aluminum, molybdenum, diamond, silicon, alumina, aluminum nitride, aluminum oxide, and composites of silver, copper, aluminum, molybdenum, diamond, silicon, alumina, aluminum nitride, and aluminum oxide.

19. An assembly, as defined in claim **17**, wherein the reflector cup includes a thermally insulating material.

20. An assembly, as defined in claim **10**, wherein the reflector cup includes a material selected from the group consisting of silver, copper, aluminum, molybdenum, diamond, silicon, alumina, aluminum nitride, aluminum oxide, and composites of silver, copper, aluminum, molybdenum, diamond, silicon, alumina, aluminum nitride, and aluminum oxide.

21. An assembly, as defined in claim **10**, wherein the reflector cup includes a thermally insulating material.

22. A light emitting die assembly comprising:

metal leads;

an insulating body attached to the metal leads, the insulating body having a cavity; and

a heat sink of a first thermally conductive material, the heat sink separate from the metal leads, connected to the insulating body, and positioned relative to the cavity for being thermally coupled to a die.

23. The assembly of claim **22**, further including a submount of a second thermally conductive material, connected to the heat sink.

24. The assembly of claim **22**, wherein the first and second thermally conductive materials are selected from the group consisting of pure materials, compounds, and composites of silver, copper, diamond, silicon, aluminum, tungsten, molybdenum, and beryllium.

25. The assembly of claim **22**, further comprising a reflector cup positioned near the heat sink, having a reflective surface.

26. The assembly of claim **25**, wherein the reflective surface is selected from the group consisting of silver, aluminum, gold, silver with a dielectric coating, gold with a dielectric coating, and aluminum with a dielectric coating.

27. The assembly of claim **25**, wherein the reflective surface includes a dielectric stack.

28. The assembly of claim **25**, wherein the reflective surface includes at least one totally internal reflective surface formed by refractive index step changes≧0.3.

* * * * *

Exhibit C

US006547249B2

(12) **United States Patent**
Collins, III et al.

(10) **Patent No.: US 6,547,249 B2**
(45) **Date of Patent: Apr. 15, 2003**

(54) **MONOLITHIC SERIES/PARALLEL LED ARRAYS FORMED ON HIGHLY RESISTIVE SUBSTRATES**

(75) Inventors: **William David Collins, III**, San Jose, CA (US); **Jerome Chandra Bhat**, San Jose, CA (US); **Daniel Alexander Steigerwald**, Cupertino, CA (US)

(73) Assignee: **Lumileds Lighting U.S., LLC**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/823,824**

(22) Filed: **Mar. 29, 2001**

(65) **Prior Publication Data**

US 2002/0139987 A1 Oct. 3, 2002

(51) **Int. Cl.**^{7} **H01L 33/00**

(52) **U.S. Cl.** **277/88**; 257/89; 257/90; 257/97; 257/98; 257/99

(58) **Field of Search** 257/88, 89, 90, 257/98, 97, 99

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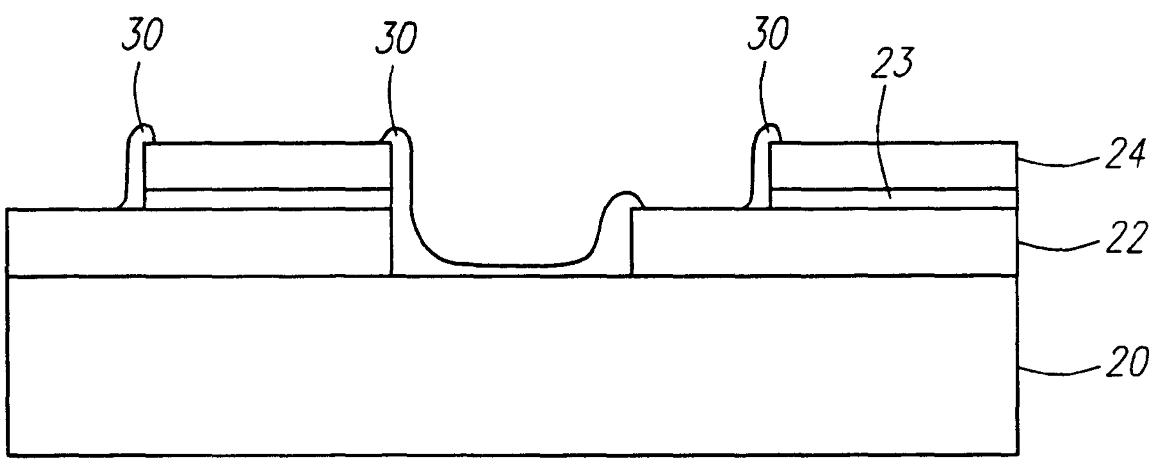
Primary Examiner—Nathan J. Flynn
Assistant Examiner—Remmon R. Fordé
(74) *Attorney, Agent, or Firm*—Patent Law Group LLP; Rachel V. Leiterman; Brian D. Ogonowsky

(57) **ABSTRACT**

Series or parallel LED arrays are formed on a highly resistive substrate, such that both the p- and n-contacts for the array are on the same side of the array. The individual LEDs are electrically isolated from each other by trenches or by ion implantation. Interconnects deposited on the array connects the contacts of the individual LEDs in the array. In some embodiments, the LEDs are III-nitride devices formed on sapphire substrates. In one embodiment, two LEDs formed on a single substrate are connected in antiparallel to form a monolithic electrostatic discharge protection circuit. In one embodiment, multiple LEDs formed on a single substrate are connected in series . In one embodiment, multiple LEDs formed on a single substrate are connected in parallel. In some embodiments, a layer of phosphor covers a portion of the substrate on which one or more individual LEDs is formed.

24 Claims, 8 Drawing Sheets



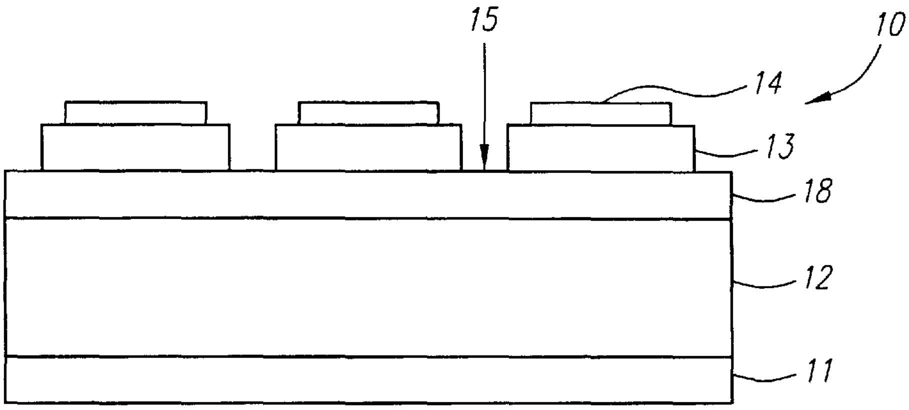


FIG. 1A

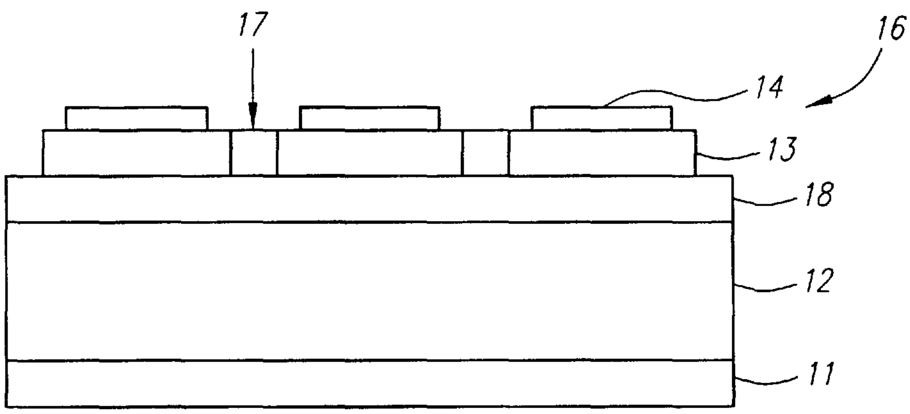


FIG. 1B

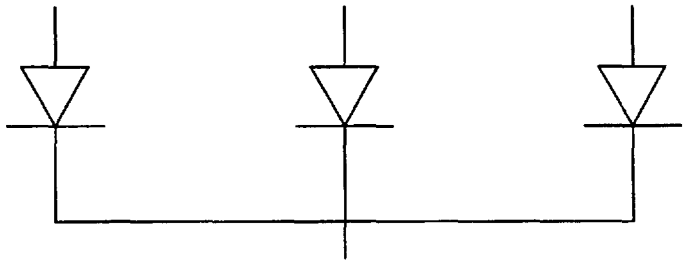


FIG. 2

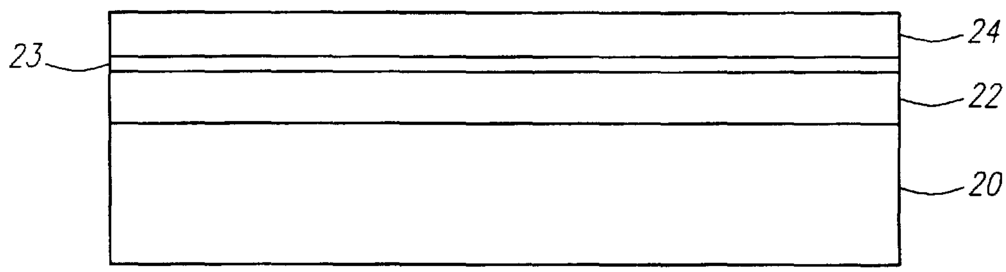


FIG. 3

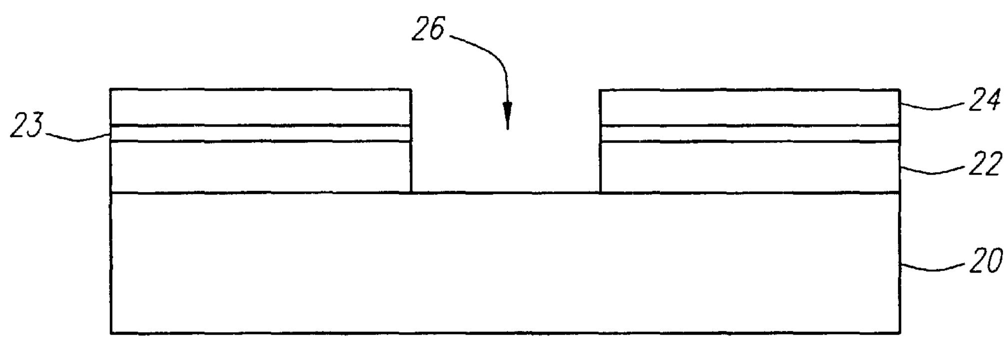


FIG. 4

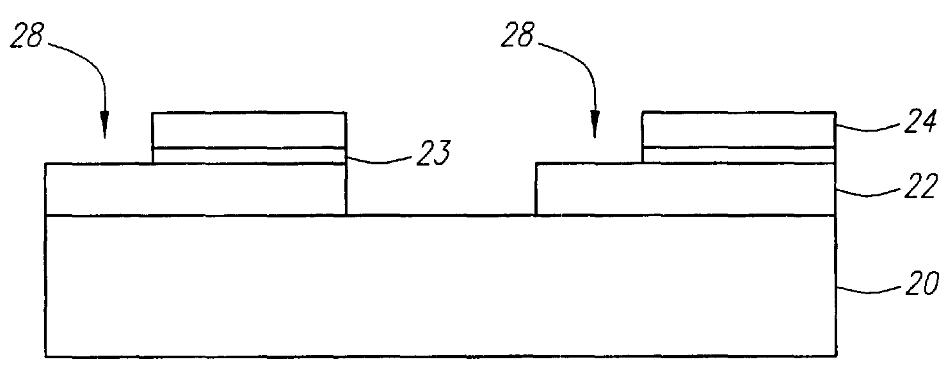


FIG. 5

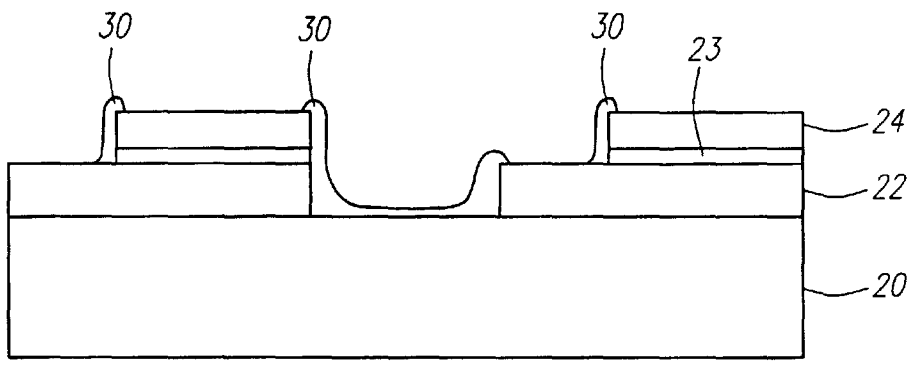


FIG. 6

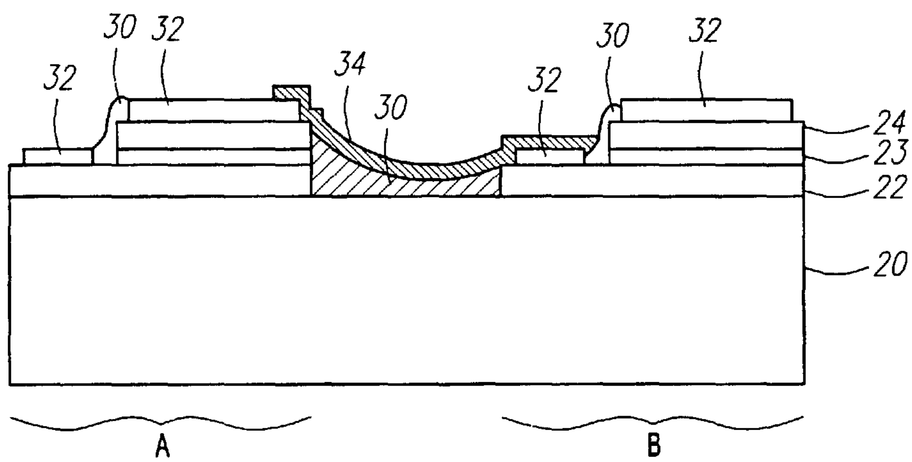


FIG. 7A

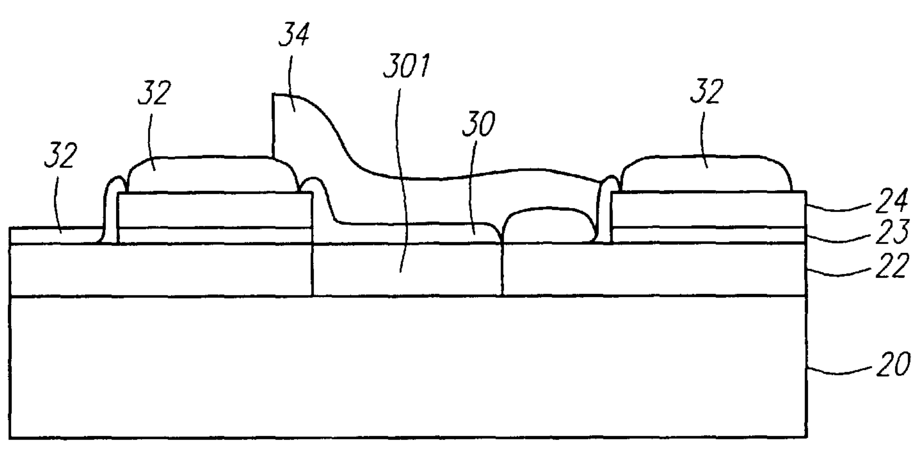


FIG. 7B

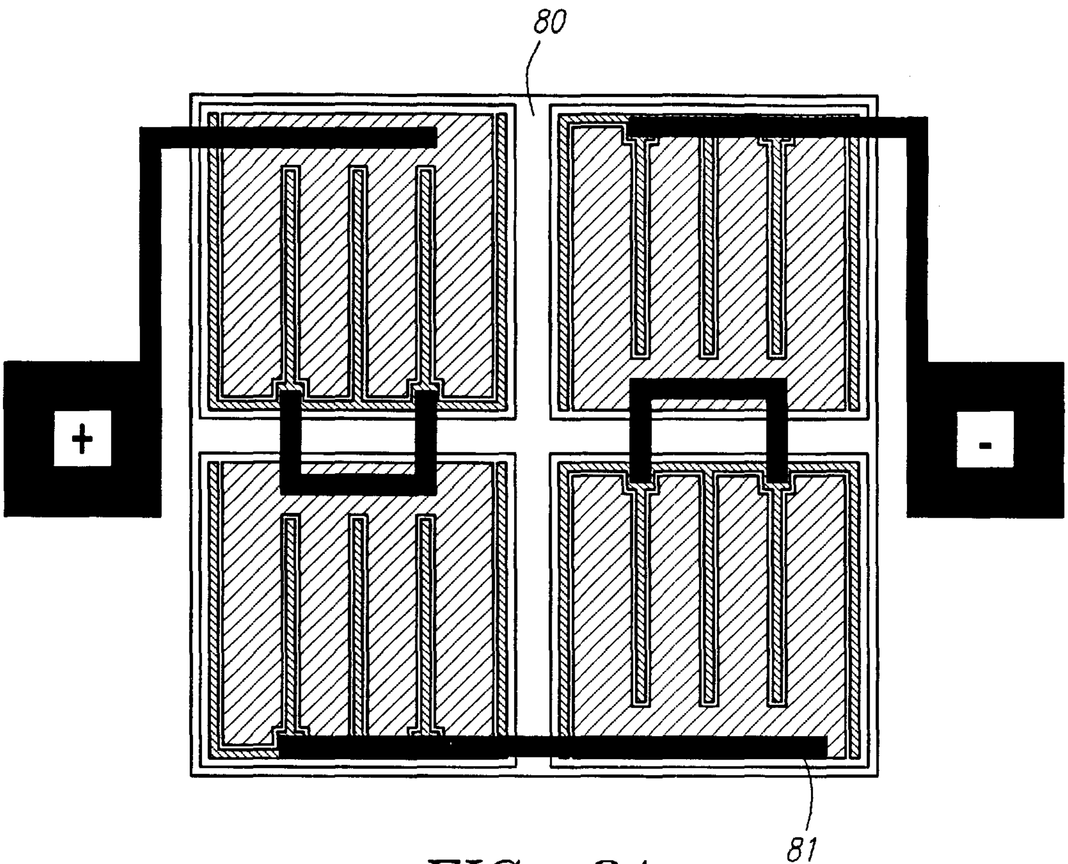


FIG. 8A

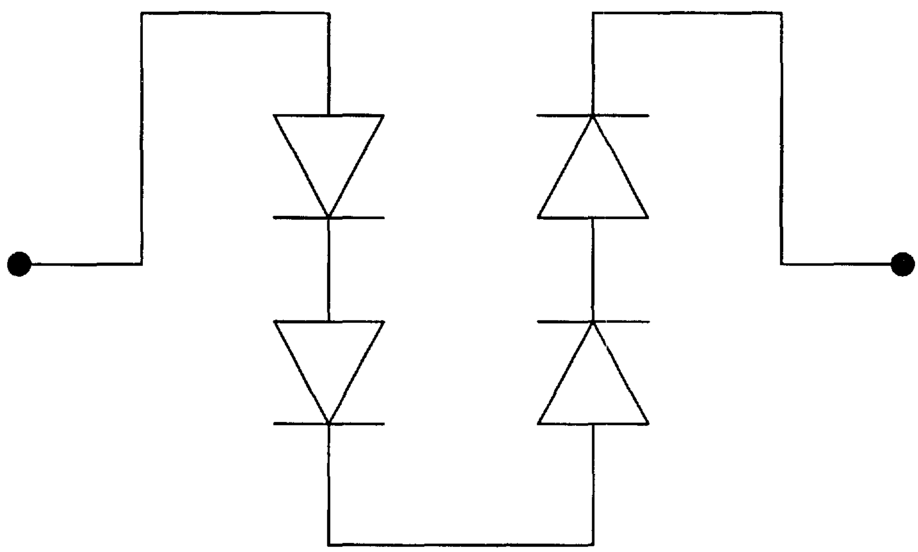


FIG. 8B

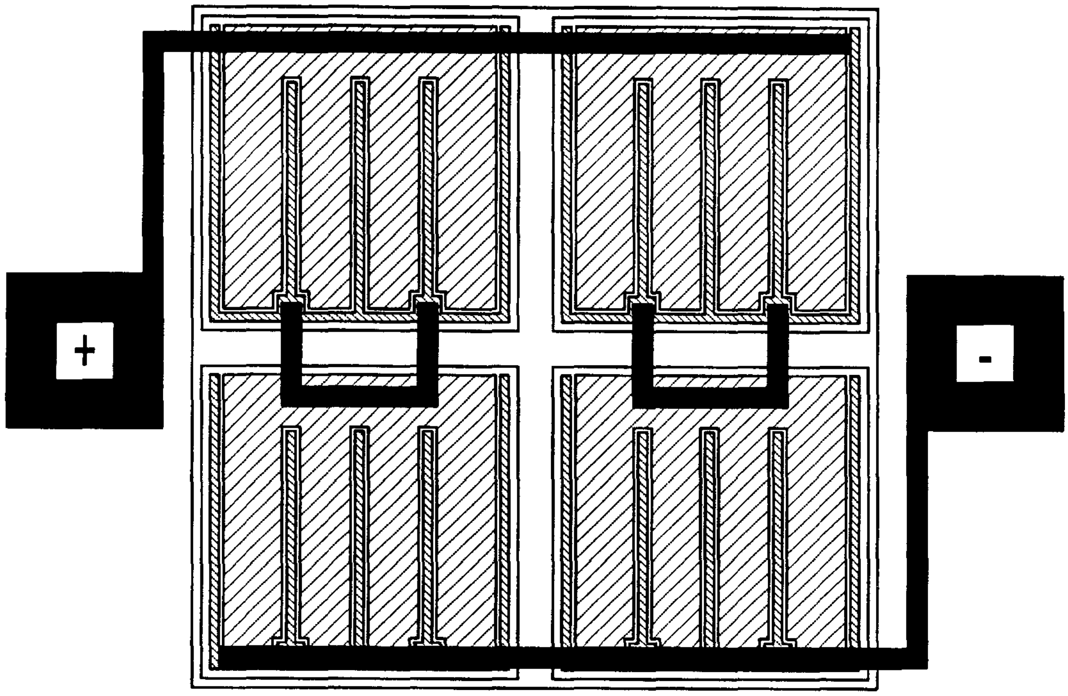


FIG. 9A

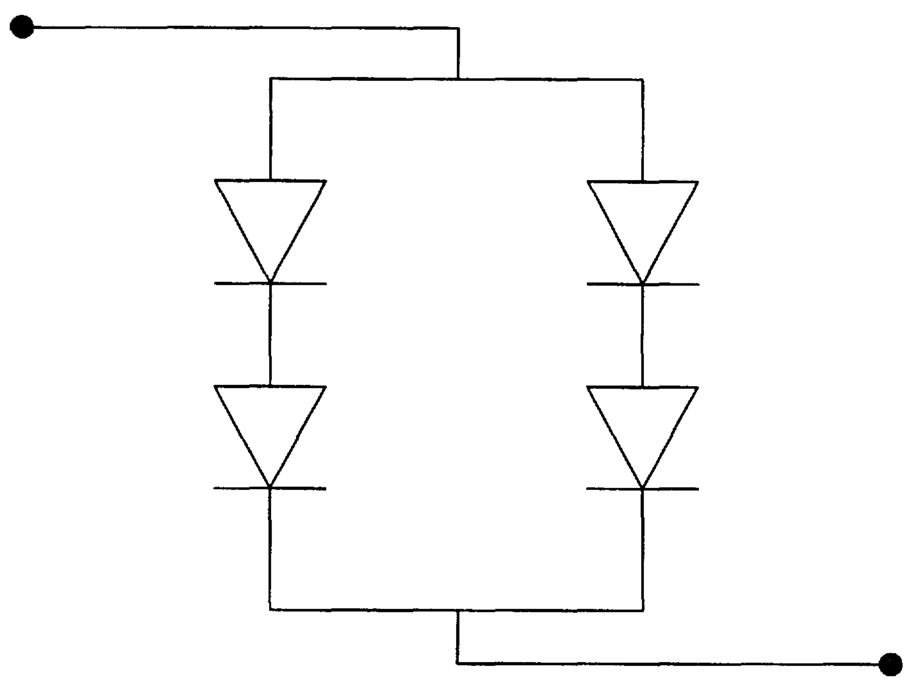


FIG. 9B

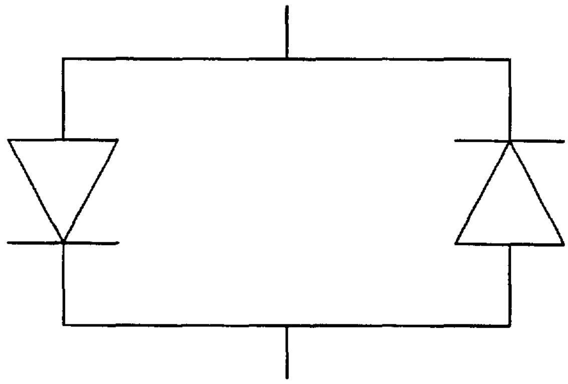


FIG. 10

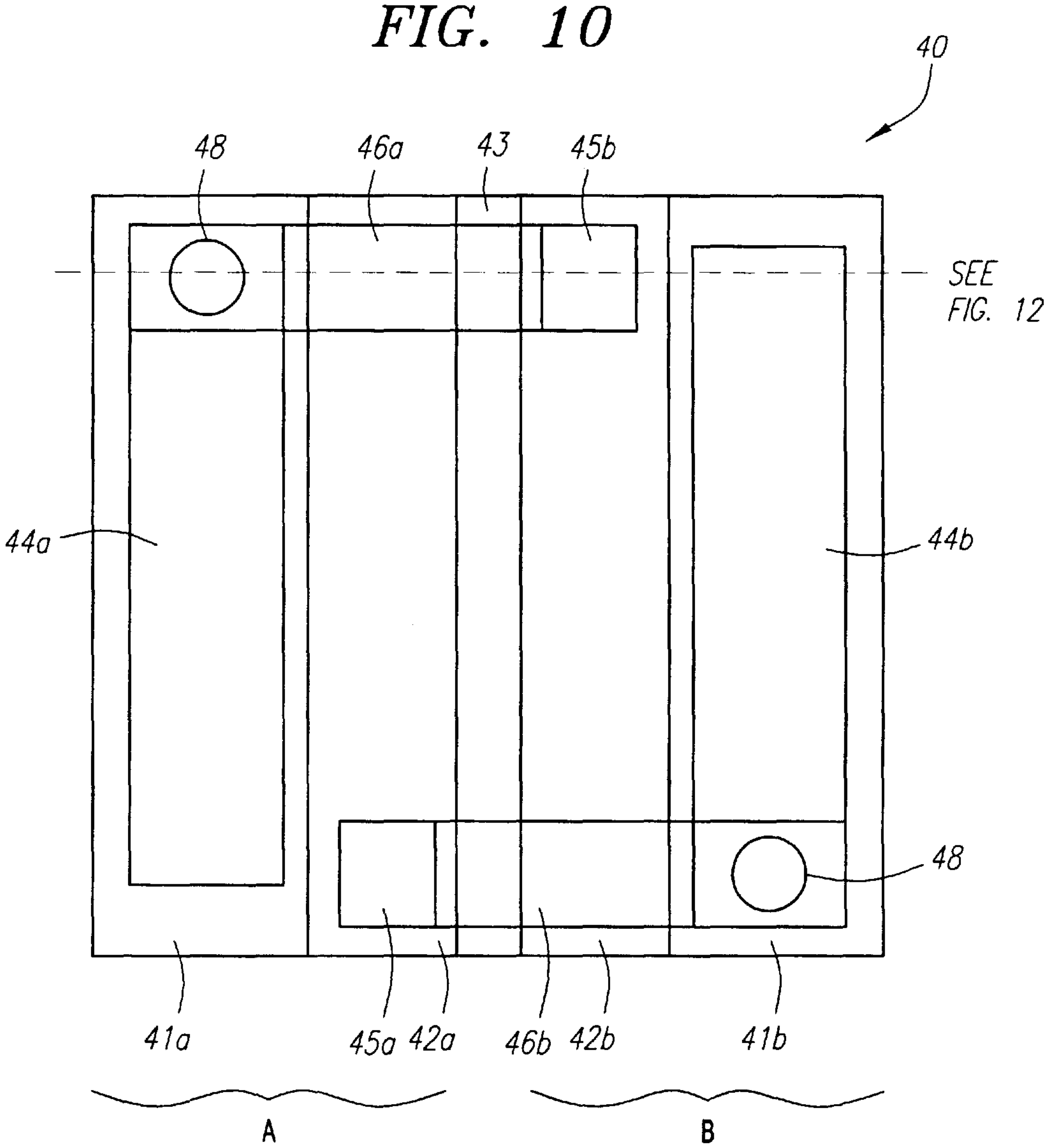
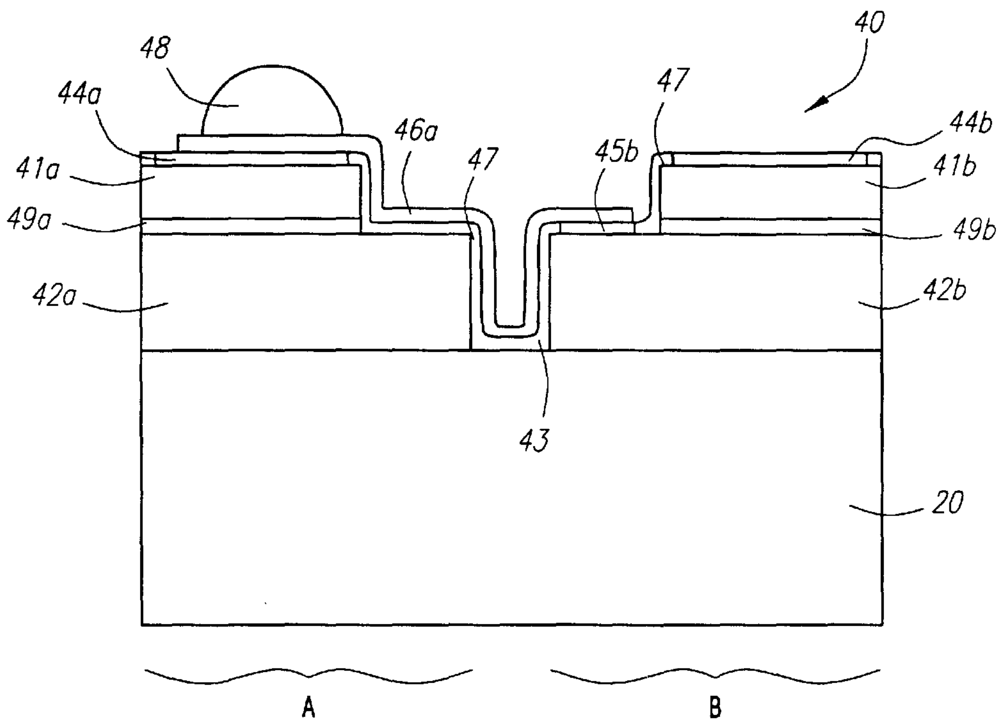


FIG. 11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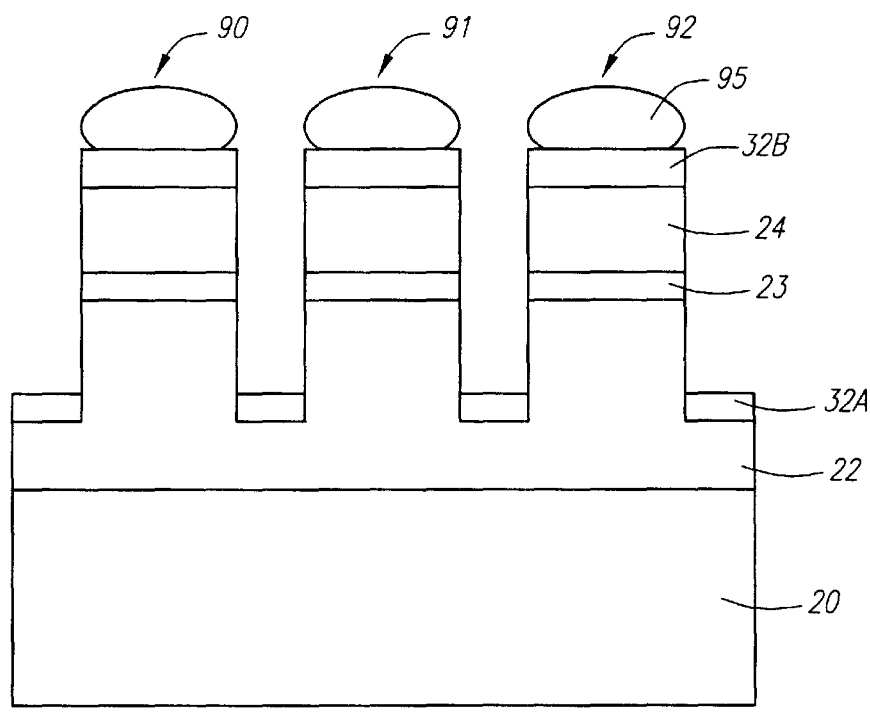
B

FIG. 12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32A
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20

FIG. 13

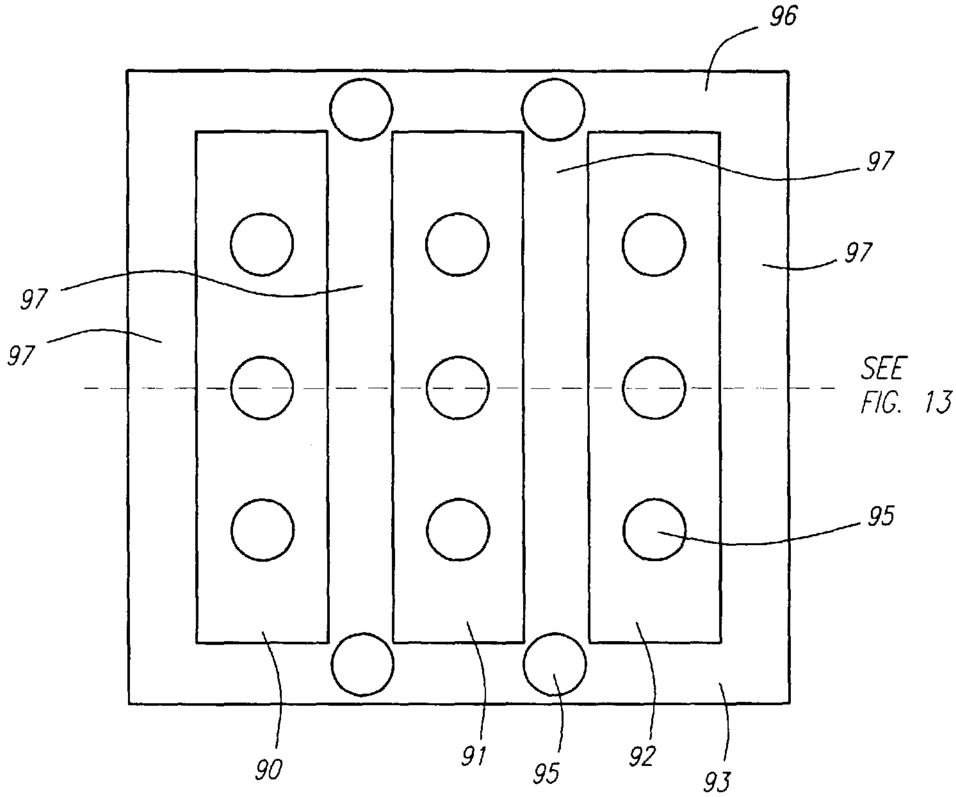

FIG. 14

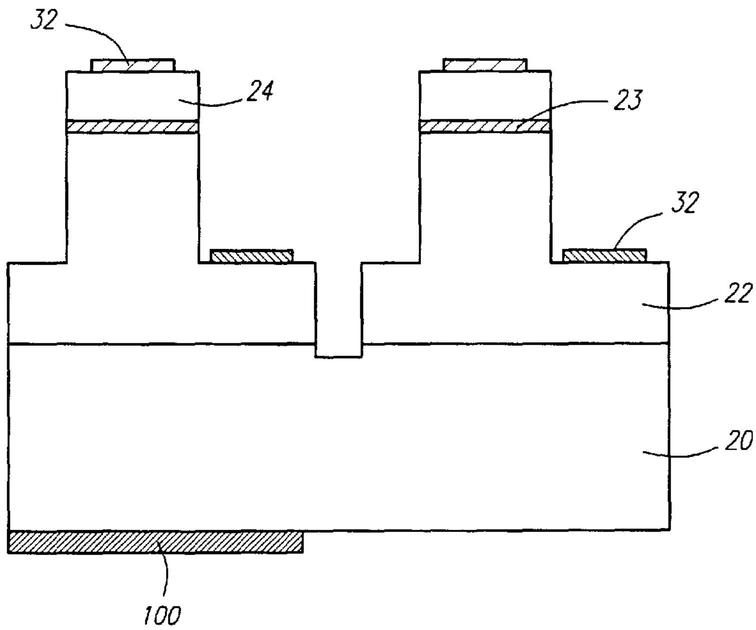

FIG. 15

MONOLITHIC SERIES/PARALLEL LED ARRAYS FORMED ON HIGHLY RESISTIVE SUBSTRATES

BACKGROUND

Conventional light emitting diode (LED) materials, such as GaAs, have allowed the construction of only single junction or multiple parallel junction devices when fabricated monolithically. FIG. **1**A illustrates a typical multiple parallel junction LED array **10**. Several p-type regions **13** are grown over a common n-type region **18**. N-contact **11** connects to n-type region **18** and several p-contacts **14** connect to p-type regions **13**. The device is fabricating by forming n-type region **18** on a substrate **12**, then forming a continuous p-type layer over the n-type region. The p-type layer is then divided into discrete regions by mechanically sawing or chemically etching trenches **15** between p-type regions **13**. FIG. **1**B illustrates another multiple parallel junction LED array **16**. Instead of mechanical sawing or chemical etching, p-type regions **13** are electrically isolated from each other by diffusion. The monolithic arrays illustrated in FIGS. **1**A and **1**B are limited to the parallel configuration illustrated in FIG. **2** because the use of contacts on opposite sides of the device requires one common conductive layer, i.e., n- or p-layer.

SUMMARY

In accordance with the present invention, a series or parallel LED array is formed on an insulating or highly resistive substrate, such that both the p- and n-contacts for the array are on the same side of the array. The individual LEDs are electrically isolated from each other by trenches or by ion implantation. Interconnects deposited on the array connect the contacts of the individual LEDs in the arrays. In some embodiments, the LEDs are III-nitride devices formed on sapphire substrates. In one embodiment, the III-nitride devices are formed on high-resistance SiC or III-nitride substrates. In one embodiment, two LEDs formed on a single substrate are connected in antiparallel to form a monolithic electrostatic discharge protection circuit. In one embodiment, multiple LEDs formed on a single substrate are connected in series. The series array can operate at a higher voltage than a single LED of the same area, thus simplifying power supply design. In one embodiment, multiple LEDs formed on a single substrate are connected in parallel. In this embodiment, multiple p-type regions are formed on a single n-type region, such that the n-type region surrounds each of the p-type regions and interposes the p-type regions. In some embodiments, a layer of phosphor covers a portion of the substrate on which one or more individual LEDs are formed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A and **1**B illustrate typical multiple parallel junction LED arrays.

FIG. **2** illustrates a circuit diagram of a parallel LED array.

FIGS. **3–6** illustrate an embodiment of a series LED array according to the present invention at various stages in fabrication.

FIGS. **7**A and **7**B illustrate two embodiments of series LED arrays.

FIG. **8**A illustrates a plan view of an embodiment of a series LED array.

FIG. **8**B illustrates a circuit diagram of a series LED array.

FIG. **9**A illustrates a plan view of a series/parallel LED array.

FIG. **9**B illustrates a circuit diagram of a series/parallel LED array.

FIG. **10** illustrates a circuit diagram of a pair of antiparallel LEDs.

FIG. **11** illustrates a plan view of an embodiment of a monolithic ESD protection structure.

FIG. **12** illustrates a cross section of the structure shown in FIG. **11**.

FIG. **13** illustrates a cross section of a parallel LED array.

FIG. **14** illustrates a plan view of the structure shown in FIG. **13**.

FIG. **15** illustrates a monolithic LED array with phosphor covering one of the individual LEDs.

DETAILED DESCRIPTION

Materials systems currently of interest in the manufacture of high-brightness light emitting diodes (LEDs) capable of operation across the visible spectrum are Group III–V semiconductors, particularly binary, ternary, and quaternary alloys of gallium, aluminum, indium, and nitrogen, also referred to as III-nitride materials. The III-nitride semiconductor layers referred to herein are compounds represented by the general formula $Al_xGa_yIn_{1-x-y}N$ ($0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, $0 \leqq x+y \leqq 1$), which may further contain group III elements such as boron and thallium and in which some of the nitrogen may be replaced by phosphorus, arsenic, or antimony. Typically, III-nitride devices are epitaxially grown on sapphire, silicon carbide, or gallium nitride substrates by metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), or other epitaxial techniques. Sapphire substrates are often used because of their wide availability and ease of use. Sapphire is an insulator. application Ser. No. 09/469,657, entitled "III-Nitride Light Emitting Device with Increased Light Generating Capability," filed Dec. 22, 1999 on an invention of Krames et al., and incorporated herein by reference, discloses III-nitride light-emitting devices grown onto high-refractive-index substrates which have low optical absorption. These substrates may be SiC or III-nitride materials and have high electrical resistance due to the low impurity content. III-nitride devices grown on insulating or highly resistive substrates must have both the positive and the negative polarity electrical contacts to the epitaxially-grown semiconductor on the same side of the device. In contrast, semiconductor devices grown on conducting substrates such as those shown in FIGS. **1**A and **1**B are typically fabricated such that one electrical contact is formed on the epitaxially grown material and the other electrical contact is formed on the substrate.

With the use of insulating or highly resistive substrates, III-nitride monolithic LED arrays may be fabricated by forming trenches or ion implantation regions between the individual LEDs to electrically isolate the individual LEDs. FIGS. **3–7** illustrate the fabrication of a III-nitride monolithic LED array in accordance with one embodiment of the present invention. In FIG. **3**, an n-type layer **22** of, for example, GaN doped with Si, Ge, or O is formed overlying highly resistive substrate **20**. An active layer **23** of, for example, InGaN is then formed overlying n-type layer **22**, and finally a p-type layer **24** of, for example, AlGaN doped with Zn, Mg, Be, Ca, or Cd is formed overlying the active layer. Layers **22**, **23**, and **24** may actually contain several sublayers of different composition and dopant concentration which are omitted for clarity. For example, n-type layer **22** may include, a nucleation layer, a highly resistive GaN layer (e.g. a GaN layer that is non-intentionally doped), and a lightly n-doped layer, then a more heavily doped n-layer. Active layer **23** may be, for example, a multiple quantum well structure.

In FIG. **4**, a portion of the n-type layer **22**, the active layer **23** and p-type layer **24** is etched away to form a trench **26**. The etch used may be, for example, a reactive ion etch with a chlorine-containing etchant gas such as BCl_3. Trench **26** is wide enough to electrically isolate the semiconductor layers on either side of the trench. Trench **26** is etched down to the substrate or to a highly resistive layer underlying n-type layer **22**, such as a non-intentionally doped GaN layer. Similarly, the adjacent LEDs may be electrically isolated by use of an ion implantation process which can render the intervening material to be highly resistive. A portion of p-type layer **24** and active layer **23** of each remaining island of semiconductor material is then etched away as illustrated in FIG. **5** using, for example, a reactive ion etch. The second etch exposes ledges **28** on n-type layer **22**, where n-type contacts are eventually formed.

Turning now to FIG. **6**, the ledges for n-contact formation are electrically isolated by depositing a dielectric material **30** over the device. The dielectric is then patterned and removed in places to open contact holes on n-type layer **22** and p-type layer **24**, such that dielectric **30** is left in trench **26** between the individual LEDs on the substrate and on the mesa walls between the exposed p-type layer and n-type layer of each LED. Dielectric **30** may be, for example, oxides of silicon, nitrides of silicon, oxynitrides of silicon, aluminum oxide, or any other suitable dielectric material.

FIGS. **7**A and **7**B show two examples of completed series LED arrays. FIG. **7**A illustrates a device where the LEDs in the array are separated by trenches. FIG. **7**B illustrates a device where the LEDs in the array are separated by ion implantation regions **301**. Electrode materials are deposited and patterned to form p- and n-contacts **32**. Typical contact materials are Al or Ti—Al for the n-contact and Ag, Au, Ni, Pt, or alloys thereof for the p-contact. Contacts **32** may be transparent, such as in devices where light is extracted through the surface of the epitaxial layers, or reflective, such as in flip-chip devices where light is extracted through the substrate. After depositing and patterning the contacts, an array of unconnected light emitting diodes has been formed on a single substrate. Other process flows can be used to develop the same final structure. The LEDs can then be connected in many different configurations.

Interconnects **34** to connect the individual LEDs on the device are then deposited. Interconnect **34** may be, for example Al, Cu, Au, Ag or alloys such as AlSiCu. P- and n-contacts **32** are materials optimized to form ohmic contact with the semiconductor layers, while interconnect **34** is a thick, highly conductive material optimized for carrying current. If light is extracted from the device through transparent contacts, interconnect **34** is deposited to block as little of the contacts as possible to minimize the amount of light absorbed in the interconnect. The two LEDs illustrated in FIGS. **7**A and **7**B are connected in series, with the n-contact of LED B connected to the p-contact of LED A. As is apparent, metal interconnects **34** can be deposited to connect the LEDs of a monolithic array in many different configurations.

In one embodiment, such as that shown in FIGS. **8**A and **8**B, a series array of four LEDs is formed in a balanced square configuration. FIG. **8**B shows a circuit diagram of four LEDs connected in series in a square array. FIG. **8**A shows a plan view of one embodiment of FIG. **8**B. It is desirable to minimize the largest dimension of the LED array, because after fabrication the array is packaged in an optic to direct light out of the packaged array. The optic typically grows geometrically with the size of the light source.

The array in FIG. **8**A has four serially connected LEDs that are electrically isolated via etching to remove III-nitride material to form a trench **80** between the individual LEDs as described above in FIGS. **3**–**7**A. The etching proceeds to at least a highly resistive III-nitride layer, such as a non-intentionally doped GaN layer. The electrical interconnections are provided by metallic traces **81**. The resulting device may be represented by the electronic circuit shown in FIG. **8**B. This device thus operates at 4× the voltage, and 4× less current, than a single LED of the same active region area. For example, a 1 mm^2 III-nitride LED may operate at 3.0 V and 350 mA. This same active junction area, broken up into four series-interconnected LEDs as shown in FIG. **8**A, provides a device operating at 12.0 V and 87.5 mA. This higher voltage, lower current operation places less demand on the electronic driver circuit for the LED array. In fact, the electronic driver circuit can run at higher efficiency at higher voltages, improving the overall efficiency of the LED lighting system. A monolithic device, according to this embodiment, is preferred over a conventional approach of attaching individual LED dice in series. In the conventional approach, the total area taken up by the LED die is increased because of the tolerances required by die-attach machines. This undesirably increases the optical source size of the total LED and requires an increase in subsequent optics sizes in the LED system. In the preferred embodiment, the diodes may be spaced as closely together as allowed by the trench etching or ion implantation for electrical isolation. The trench or ion implantation region width may be as small as a few microns, so that the packing density of diodes in the embodiment can be very high.

In accordance with the invention, monolithic series arrays of LEDs may offer several advantages. First, monolithic arrays cut down on the number of connections to external circuitry, such as a submount. If the device is formed such that light is extracted from the epitaxial side of the device through transparent contacts, a reduction in the number of connections to external circuitry means that light can be extracted from more area of the device. In such devices, the LEDs are typically connected to external circuitry by wire bonds, which partially obscure the light which is usefully extracted from the LED die. Interconnects would typically obscure this extracted light to a much smaller extent. If the device is a flip chip, fewer contacts to the submount means that the device can have more active region to generate light. Second, as described above, monolithic serial arrays operate at a higher voltage than an individual LED. A higher operating voltage can simplify the design of a power supply to drive the LED array.

FIGS. **9**A and **9**B illustrate a balanced square series/parallel LED array. FIG. **9**B shows a circuit diagram of four LEDs connected as two parallel strings of two LEDs connected in series. FIG. **9**A shows a plan view of one embodiment of FIG. **9**B. Such a series/parallel array is formed as described above in reference to FIGS. **3**–**7**A.

FIG. **10** illustrates an electrostatic discharge (ESD) protection circuit, where two diodes are connected in an anti-parallel configuration. The first LED clamps reverse breakdown in the second LED. FIGS. **11** and **12** illustrate one embodiment **40** of a monolithic ESD protection circuit.

Structures A and B are formed on a highly resistive substrate **20**. One structure A is connected as an LED to produce light, while the other structure B is used to clamp reverse breakdown in LED A. P-type layers **41***a* and **41***b* overlay active regions **49***a* and **49***b*, which are formed on n-type layers **42***a* and **42***b*. A trench **43** is formed between devices A and B. Ledges for contact formation on n-type layers **42***a* and **42***b* are exposed such that the n-electrodes **45***a* and **45***b* are opposite trench **43** from each other. A dielectric layer **47** electrically insulates the metallization layer **46***a* from all electrical contact except where openings are made for inter-layer interconnects, or for contacts to such areas as the p-contacts or n-contacts. P-electrode **44***a* and n-electrode **45***b* are connected by interconnect **46***a* such that the p-contact of LED A is connected to the n-contact of clamping device B. In the region where interconnect **46***a* is deposited, the n-contact of LED A is isolated from interconnect **46***a* by dielectric layer **47**, as illustrated in FIG. **12**. As shown in FIG. **11**, the interconnection between the p-contact of LED A and the n-contact of clamping device B is formed on one side of the device, and the interconnection between the n-contact of LED A and the p-contact of clamping device B is formed on the other side of the device. The structure can then be connected to a submount or other structure (not shown) by solder bumps or wire bonds **48**.

FIGS. **11** and **12** show a structure where the clamping device is the same size as the LED. Since the clamping device does not emit light in normal operating circumstances, the size of the clamping device can be reduced relative to the LED. In one embodiment, the p-n junction for the clamping device can be formed underneath a solder bump or wire bond **48**, such that no useful light emitting area is lost. In another embodiment, the size of the two anti-parallel diodes is approximately equal and the device can be operated with an alternating current source.

Parallel LED arrays may also be formed on highly resistive substrates. FIGS. **13** and **14** illustrate one embodiment of such an array. Three p-type regions **90**, **91**, and **92** are isolated from each other by a single continuous n-type region **93** interposing the p-type regions. P-contacts **32***b* deposited on p-type layer **24** and n-contacts **32***a* deposited on n-type layer **22** connect to a submount (not shown) by solder bumps **95**. The submount may include control circuitry or appropriate connectivity for independently addressing each p-type region. In such embodiments, each LED may be operated independently of the others.

A single LED where the n-type region interposes portions of a single p-type region is described in application Ser. No. 09/469,657, filed Dec. 22, 1999 on an invention of Krames et al., titled "III-Nitride Light-Emitting Device with Increased Light Generating Capability,". The Krames et al. device lacks the top horizontal portion **96** of n-contact **93** and the top two solder bumps on the n-contact, shown in FIG. **14**. As a result, current from the two lower n-contact solder bumps does not spread readily into the uppermost portions of the vertical arms **97** of n-contact **93**. In fact, electromigration of the n-contact material can cut off all current flow into the vertical portions of the n-contact of such a device. In contrast, the symmetrical parallel junction device shown in FIG. **14** provides more avenues for current flow and increased redundancy. The top horizontal arm **96** of the n-contact eliminates "dead ends" at the tops of vertical arms **97**, thus current spreads readily into all portions of the n-contact **93**.

One or more of the individual LEDs in either a series or a parallel monolithic array of LEDs can be covered with a phosphor to change the color of the light generated by the LED, as illustrated in FIG. **15**. In a flip chip device, a phosphor coating **100** is printed on the bottom surface of a portion of the substrate on which a single LED in the array is formed. One method of applying phosphor coatings to the substrates of flip chip devices is described in more detail in application Ser. No. 09/688,053, filed on Oct. 13, 2000 on an invention of Lowery, titled "Stenciling Phosphor Layers on Light Emitting Diodes," and incorporated herein by reference. By applying a phosphor coating over some of the LEDs in a monolithic array, LED arrays can simultaneously generate different colors of light. Such an array may be useful to mix colors in order to form white light. For an LED array which incorporates independently addressable parallel LEDs coupled with selective phosphor placement, one may create color-tunable LED arrays.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.

We claim:

1. An array of light emitting devices formed on a highly resistive substrate, the array comprising:

a first light emitting device, comprising:

a first n-type layer overlying a first portion of the substrate;

a first active region overlying the first n-type layer;

a first p-type layer overlying the first active region;

a first n-contact connected to the first n-type layer;

a first p-contact connected to the first p-type layer, wherein the first n-contact and the first p-contact are formed on the same side of the device;

a second light emitting device, comprising:

a second n-type layer overlying a second portion of the substrate;

a second active region overlying the second n-type layer;

a second p-type layer overlying the second active region;

a second n-contact connected to the second n-type layer;

a second p-contact connected to the second p-type layer, wherein the second n-contact and the second p-contact are formed on the same side of the device;

one of a trench and an ion implanted region separating the first light emitting device and the second light emitting device; and

a first interconnect connecting one of the first n- and first p-contacts to one of the second n- and second p-contacts.

2. The array of claim **1** wherein the first and second n-type layers, the first and second active regions, and the first and second p-type layers comprise III-nitride layers.

3. The array of claim **1** wherein the substrate is selected from the group consisting of sapphire, SiC, and III-nitride materials.

4. The array of claim **1** wherein the first interconnect connects the first p-contact to the second n-contact, the array further comprising a second interconnect connecting the second p-contact to the first n-contact.

5. The array of claim **4** further comprising a layer of dielectric material underlying a portion of the first and second interconnects.

6. The array of claim **1** wherein the first light emitting device and the second light emitting device are connected in series.

7. The array of claim **1** wherein the first light emitting device and the second light emitting device are connected in parallel.

8. The array of claim **1** further comprising a layer of phosphor coating a surface of the first portion of the substrate opposite the first n-type layer.

9. The array of claim **1** further comprising an highly resistive layer under the first n-type layer and the second n-type layer, wherein the highly resistive layer forms the bottom of the trench.

10. The array of claim **1** further comprising:

a third light emitting device, comprising:

a third n-type layer overlying a third portion of the substrate;

a third active region overlying the third n-type layer;

a third p-type layer overlying the third active region;

a third n-contact connected to the third n-type layer;

a third p-contact connected to the third p-type layer, wherein the third n-contact and the third p-contact are formed on the same side of the device;

a fourth light emitting device, comprising:

a fourth n-type layer overlying a fourth portion of the substrate;

a fourth active region overlying the fourth n-type layer;

a fourth p-type layer overlying the fourth active region;

a fourth n-contact connected to the fourth n-type layer;

a fourth p-contact connected to the fourth p-type layer, wherein the fourth n-contact and the fourth p-contact are formed on the same side of the device;

a second interconnect connecting the first n-contact to the third p-contact;

a third interconnect connecting the second n-contact to the fourth p-contact; and

a fourth interconnect connecting the third n-contact to the fourth n-contact;

wherein said one of a trench and an ion implanted region separates each of the first, second, third, and fourth light emitting devices from each other; and

wherein said first interconnect connects the first p-contact to the second p-contact.

11. An array of III-nitride light emitting devices formed on an highly resistive substrate, the array comprising:

a layer of a first conductivity type overlying the substrate;

a plurality of active regions overlying the layer of first conductivity type, such that an area underlying each active region in the plurality is surrounded by a portion of the layer of first conductivity type and portions of the layer of first conductivity type interpose areas underlying each active region in the plurality of active regions;

a plurality of layers of second conductivity type, overlying the plurality of active regions;

a first contact connected to the layer of first conductivity type; and

a plurality of second contacts connected to the plurality of layers of second conductivity type.

12. The array of claim **11** wherein the first contact surrounds an area underlying each active region in the plurality of active regions.

13. The array of claim **11** wherein the layer of first conductivity type comprises GaN doped with Si.

14. The array of claim **11** wherein the plurality of layers of second conductivity type comprise AlGaN doped with Mg.

15. The array of claim **11** wherein the plurality of second contacts comprise silver.

16. The array of claim **11** wherein the first contact comprises Al.

17. The array of claim **11** wherein the first contact comprises Ag.

18. The array of claim **11** wherein the substrate is selected from the group consisting of sapphire, SiC, and III-nitride materials.

19. The array of claim **11** further comprising a layer of phosphor coating a portion of a surface of the substrate underlying one of the plurality of active regions, the surface being opposite the layer of first conductivity type.

20. The array of claim **1** wherein the first interconnect overlies the trench or ion implanted region.

21. The array of claim **1** wherein the array is a monolithic structure.

22. The array of claim **21** wherein the first interconnect is part of the monolithic structure.

23. The array of claim **1** further comprising a layer of phosphor coating a surface of the substrate opposite the first and second light emitting devices, wherein, after conversion by the phosphor coating, each of the first and second light emitting device emits substantially the same color light.

24. The array of claim **11** wherein at least one of the plurality of layers of second conductivity type comprises InGaN.

* * * * *

Exhibit D

US006590235B2

(12) **United States Patent**
Carey et al.

(10) **Patent No.: US 6,590,235 B2**
(45) **Date of Patent: *Jul. 8, 2003**

(54) **HIGH STABILITY OPTICAL ENCAPSULATION AND PACKAGING FOR LIGHT-EMITTING DIODES IN THE GREEN, BLUE, AND NEAR UV RANGE**

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(73) Assignee: **Lumileds Lighting, U.S., LLC**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 146 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/775,765**

(22) Filed: **Feb. 2, 2001**

(65) **Prior Publication Data**

US 2001/0010371 A1 Aug. 2, 2001

Related U.S. Application Data

(63) Continuation of application No. 09/187,357, filed on Nov. 6, 1998, now Pat. No. 6,204,523.

(51) **Int. Cl.**[7] **H01L 33/00**
(52) **U.S. Cl.** **257/98**
(58) **Field of Search** 257/98, 99, 100, 257/791, 502; 438/25, 26, 28

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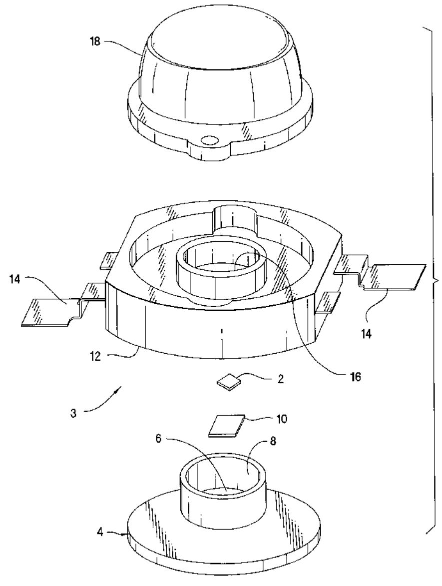
Primary Examiner—Craig Thompson
(74) *Attorney, Agent, or Firm*—Patent Law Group LLP; Rachel V. Leiterman

(57) **ABSTRACT**

An LED component is provided, with light emission in the green-to-near UV wavelength range. The light-emitting semiconductor die is encapsulated with one or more silicone compounds, including a hard outer shell, an interior gel or resilient layer, or both. The silicone material is stable over temperature and humidity ranges, and over exposure to ambient UV radiation. As a consequence, the LED component has an advantageously long lifetime, in which it is free of "yellowing" attenuation which would reduce the green-to-near UV light output.

17 Claims, 2 Drawing Sheets



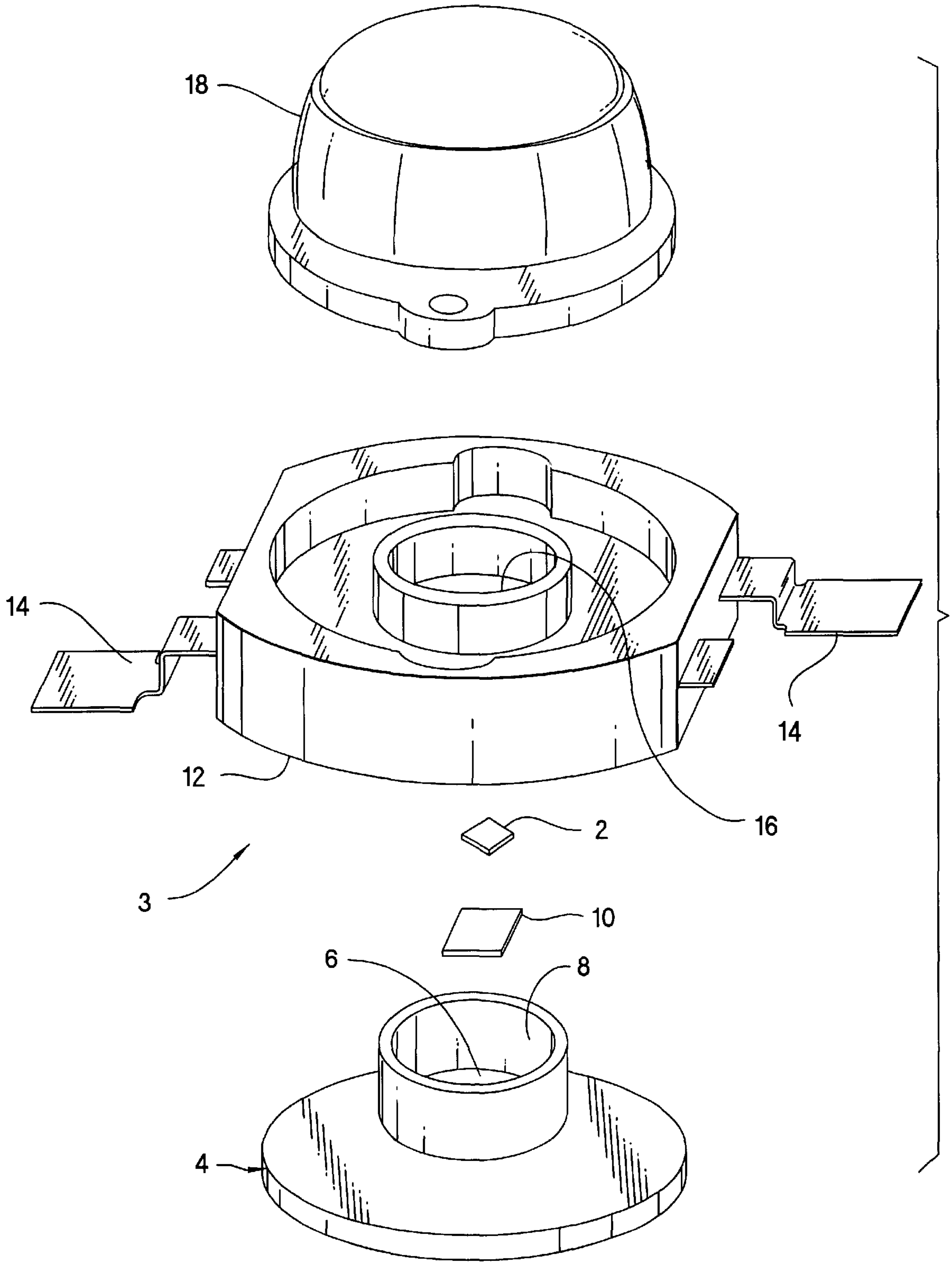


Fig. 1

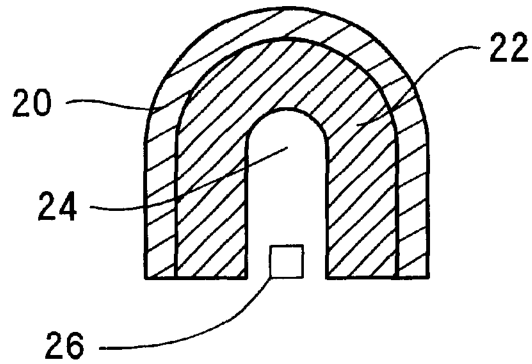


Fig. 2

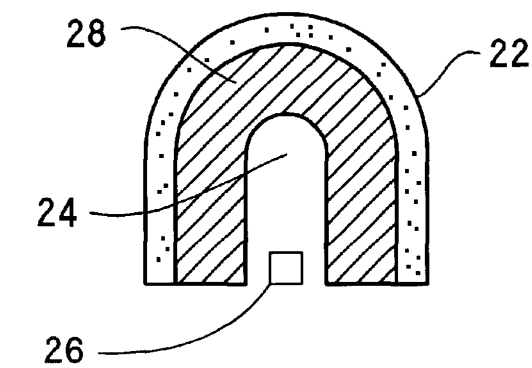


Fig. 3

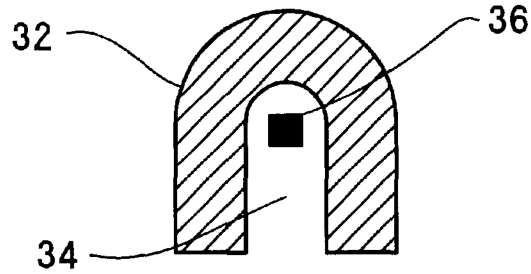


Fig. 4

HIGH STABILITY OPTICAL ENCAPSULATION AND PACKAGING FOR LIGHT-EMITTING DIODES IN THE GREEN, BLUE, AND NEAR UV RANGE

This application is a continuation of U.S. application Ser. No. 09/187,357, filed Nov. 6, 1998, now U.S. Pat. No. 6,204,523.

FIELD OF THE INVENTION

The invention generally relates to the field of Light-Emitting Diode (LED) technology. More specifically, the invention relates to LED packaging and encapsulation.

BACKGROUND OF THE INVENTION

An LED component essentially comprises an LED chip (a piece of semiconductor material with appropriate wire leads) and a package (typically a substantially transparent material, configured in a dome shape, the dome acting as a lens for the emitted light).

The package must be rigid enough, at least on its exterior, to make the LED component structurally sound. On its interior, however, the package must be soft or resilient enough in the vicinity of the LED chip, that mechanical stresses do not damage the LED chip or the wire leads. Throughout, the transparent material of the package must keep light attenuation as small as possible, and must not adversely affect the spectrum of light which is emitted from the LED component.

Conventionally, it has been necessary to compromise between these different objectives. Materials such as PMMA (polymethylmethacrylate: acrylic or "plexiglas"), glass, polycarbonate, optical nylon, transfer molded epoxy, and cast epoxy have been used for encapsulation.

However, these materials suffer from the drawback that their optical transmissive characteristics degrade over time. As the material degrades, light is absorbed ("attenuation") to an increasing degree. In particular, light with shorter wavelengths, from the UV through the yellow, is absorbed. The result is called "yellowing", because the eye perceives the light, tending more toward longer wavelengths, as yellowish.

Note, incidentally, that there is also degradation due to decreased light output from the LED die itself.

Different LED components are configured for particular wavelengths of light. For instance, Red (≧515 nm) and Yellow or Amber (~580–595 nm) LED technology are well-developed. By contrast, green through blue LEDs (400–570 nm) present design problems which have been more difficult to overcome.

Yellowing of the light-transmissive encapsulant material is not an issue for longer-wavelength Red, Amber, or Yellow LEDs. However, shorter-wavelength LEDs are particularly subject to attenuation because of yellowing.

Therefore, there is a need for an encapsulant for LEDs in the near UV, blue, and green range which avoids the drawbacks associated with yellowing and attenuation of the encapsulant material.

SUMMARY OF THE INVENTION

There is provided, in accordance with the invention, an LED component, for light of a wavelength in the green-to-near UV wavelength range, approximately 570 to 350 nm. The light-emitting semiconductor die is encapsulated with one or more silicone compounds, including a hard outer shell, an interior gel or resilient layer, or both. The silicone material is stable over temperature and humidity ranges, and over exposure to ambient UV radiation. As a consequence, the LED component has an advantageously long lifetime, in which it is free of "yellowing" attenuation which would reduce the green-to-near UV light output.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an exploded view of an LED according to the invention.

FIG. **2** is a cross-sectional view of an LED component according to a first embodiment of the invention.

FIG. **3** is a cross-sectional view of an LED component according to a second embodiment of the invention.

FIG. **4** is a cross-sectional view of an LED component according to a third embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Explanation of Terminology Used

In the discussion which follows, a naming convention will be used, in which the light-emitting semiconductor material itself is called an "LED chip" or an "LED die", and the overall packaged LED device, including the LED chip and the encapsulant, is called an "LED component."

Also, the verb "to encapsulate," and/or other forms of the word, including nouns, will be used in a broad, generic sense to refer to any way of enclosing the LED die, such that the enclosure protects and isolates the LED die from deleterious environmental effects, enhances light extraction from the LED die, and controls the external radiation patterns. An LED die may be encapsulated by placing a rigid cover over the die, by molding and curing a conformal material around the die into a predetermined shape, by a combination of the two, or by other techniques that would be known to persons skilled in the LED and the electrical component fields.

The optically transmissive cover will also be referred to as an "optic." The term "optic" broadly applies to any optically transmissive member. An optic may commonly be configured to refract light; that is, any lens may be referred to as an optic. However, an optic may also cause little or no refraction. For instance, a glass pane window is also an optic. The term "optic" applies to all embodiments of the optically transmissive cover presented herein, and to other embodiments of the invention which, given the present disclosure, a person skilled in the art would be aware of. In particular, the term "optic" applies to hard shell material, to softer, gel-type material, and to combinations of both.

It will be understood that optics are "optically transmissive." The term "optically transmissive" broadly covers transparency, translucency, transmissivity with dispersants, and other types of optical transmission.

LED Structure—FIG. 1

FIG. **1** is an exploded view of an LED component. An LED die **2** is driven by electrical current from wire leads (not shown). Responsive to current flow, the LED die **2** emits light.

The LED die **2** is enclosed in a package which generally includes a bed arrangement **3** upon which the LED die **2** rests, and an optically transmissive cover, generally including a lens. The structure shown in FIG. **1** is exemplary, and a wide variety of other structures would be known to persons skilled in LED technology.

The bed arrangement **3** supports the LED die **2** and its leads. As shown, the bed arrangement **3** includes a lower housing member **4** which has a die placement area **6**. The die placement area **6** may be substantially flat, or may be configured as a receptacle, as shown. A reflective surface **8** may be provided on the die placement area **6**, to direct emitted light outward. A substrate member **10** may be positioned inside the die placement area **6**, to support the die **2** itself.

The bed arrangement **3** also includes a lead support member **12**, which is positioned over the lower housing member **4**. Heavy leads **14**, provided on the exterior of the LED component for incorporating the LED component into circuits and systems, are coupled through the lead support member **12** to fine leads (not shown), which couple directly to the LED die **2**. The lead support member **12** includes an aperture **16**, through which light emitted by the die **2** passes.

The Optically Transmissive Cover of an LED Component

An optically transmissive cover **18** is positioned over the bed arrangement **3**, to cover and protect the LED die **2** and its leads. The cover **18** is made of one or more materials which are chosen for their light-transmissive properties, and for their stability over the environmental conditions under which the LED component is to operate. These environmental conditions include a wide range of temperatures (including Joule heating from operation) and ambient UV radiation. It is common practice to configure the cover **18** as a lens (generally in a convex shape) to direct the flow of light.

Conventionally, the optically transmissive cover **18** has been made of hard optical materials such as PMMA, glass, polycarbonate, optical nylon, transfer molded epoxy, and cyclic olefin copolymer.

For infrared (IR) (>940 nm) through Yellow-green (>560 nm) wavelength LED chips, silicone materials have been used to provide low stress junction coating during epoxy encapsulation, or used in conjunction with the above-listed hard optical materials.

For red monolithic display LEDs, silicone has also been used with no added hard materials in the optical path.

None of these conventional LED components, however, produced UV through Green light, so there was no need for overcoming the "yellowing" attenuation problem described above in connection with LED components of these wavelengths.

Statement of the Invention

In accordance with the invention, silicone is used in the optically transmissive cover of an LED component which produces light in the green through near UV range.

Aside from the general indications of hardness or softness given below, a discussion of specific silicone formulations will be omitted. Persons skilled in the art will be able to select silicone formulations suitable for their own needs based on known silicone formulations and properties. See, for instance, Jacqueline I. Kraschwitz, Herman F. Mark, et al., "Encyclopedia of Polymer Science and Engineering" (2d ed.), New York: Wiley & Sons, (1985), vol. 15. In that reference, the chapter "Silicone" provides information applicable to the relevent aspects of the invention.

In the illustration of FIG. **1**, the cover **18** is shown in simplified form. However, noteworthy features of covers such as the cover **18** will be described in detail below, in connection with embodiments of the invention. Most other details of the LED component structure, which are generally as described above, will be omitted from the illustrations of the embodiments of the invention.

The silicone encapsulant has advantageously stable optical transmission properties in the blue through green portion of the visible spectrum (400–570 nm). Because of the stability, light attenuation caused by changes in the material's light absorption properties is not a problem.

LED components according to the invention have been found to be stable over long lifetimes, greatly in excess of 1000 hours. Stability has been measured by exposure to low (−55° C.) through high temperatures (in excess of 100° C.), and low through high humidity (0–85% RH) operation. Stability also has been measured by exposure to high internal and external UV through green radiation, such as would be experienced during operation in outdoor environments.

Also, silicone has a high refractive index (~1.4 through 1.7), which makes silicone well-suited for optical refractive structures such as LED dome lenses.

First Embodiment—FIG. 2

FIG. **2** is a cross-sectional view of an LED optically transmissive cover structure, in accordance with a first embodiment of the invention.

Since it is common for LED covers to be shaped as lenses, the shape is given as a convex dome. Other shapes, however, will be known to those skilled in the art. Also, the position of the LED die is indicated, but it will be understood that leads and a suitable bed arrangement are also provided.

FIG. **2** shows an LED cover configured as per a first preferred embodiment of the invention. A hard outer shell **20** is suitably shaped, e.g., as a lens. The shell may be made of any suitable optically transmissive material, preferably a stable material such as cyclic-olefin copolymers or other optical plastics, glasses, ceramics, or other transparent materials such as Aluminum Oxide.

Inside the shell **20**, a quantity of softer, resilient material **22** is provided. In accordance with the invention, the material **22** is a silicone compound.

Inside the silicone material **22** is a space **24**, which may be a cavity or simply a region in the interior of the silicone material **22**. The space **24** is occupied by an LED die **26**. In accordance with the invention, the die produces light in the green through short UV range of wavelengths, and is therefore subject to light attenuation caused by any yellowing of the surrounding material. However, in accordance with the invention, the die **26** is surrounded by the silicone material **22**, rather than a material which is prone to yellowing. Therefore, yellowing does not take place, and the LED component of the invention advantageously does not suffer from attenuation.

Second Embodiment—FIG. 3

In the second embodiment of the invention, shown in FIG. **3**, an LED die **26** (in the green-to-near UV wavelength range) is disposed inside a space **24**, as before. Surrounding the LED die **26** is a structure including a hard outer shell and a softer interior. The interior is again a quantity of silicone material **28**, such as a gel, similar to the material **22** of FIG. **2**.

In this case, however, there is an outer shell **30** made of silicone material. Preferably, the outer shell **30** is a harder, more rigid silicone formulation than that of the material **28**, to give the desired rigidity and structural integrity to the LED component.

Since the optically transmissive cover of FIG. **2** is entirely silicone material, it provides further advantageous freedom from yellowing attenuation.

Third Embodiment—FIG. **4**

In yet another embodiment of the invention, the optically transmissive cover includes only a single layer of material.

As shown in FIG. **4**, a cover made of a single, thick layer **32** of silicone material surrounds a cavity **34**, in which an LED die **36** is disposed.

Other Embodiments of the Invention

From the description given above, persons skilled in the LED arts will foresee other embodiments that fall within the spirit and scope of the invention.

For instance, optical dispersants, such as scattering particles, may be embedded inside the optically transmissive cover, so that the LED component as a whole provides a more evenly balanced light. Such dispersants may be mixed into the silicone gel of FIGS. **2** and **3**, or formed within the hard shells of any of FIGS. **2**, **3**, and **4**.

Similarly, particles of light-emitting material, such as phosphor, may be embedded in the optically transmissive cover. Depending on the type of optically transmissive cover used (i.e., the various embodiments discussed above), the particles can be embedded either in the hard shell or in the softer interior silicone material. Responsive to excitation by radiation from the LED die, such particles emit light of a different wavelength from the radiation of the LED die.

In summary, the invention provides LED components in the green-to-near UV wavelength range, which are advantageously free of light attenuation due to yellowing or other forms of degradation of the optically transmissive lens and cover.

What is claimed is:

1. A light emitting diode (LED) component comprising:

an LED chip emitting light having a wavelength in a range of 200 to 570 nanometers; and

an optic encapsulating the LED chip, the optic comprising:

an outer optically transmissive shell of rigid material; and

a quantity of resilient, optically transmissive material inside the shell.

2. The LED component of claim **1** wherein the rigid material is selected from a group consisting of silicone, cyclic-olefin copolymer, optical plastic, glass, ceramic, and aluminum oxide.

3. The LED component of claim **1** further comprising an optical dispersant mixed into the resilient, optically transmissive material.

4. The LED component of claim **1** further comprising an optical dispersant formed within the rigid material.

5. The LED component of claim **1** further comprising particles of light-emitting material embedded in the resilient, optically transmissive material.

6. The LED component of claim **5** wherein the light-emitting material is a phosphor.

7. The LED component of claim **1** further comprising particles of light-emitting material embedded in the rigid material.

8. The LED component of claim **7** wherein the light-emitting material is a phosphor.

9. The LED component of claim **1** wherein the resilient, optically transmissive material comprises a silicone material being transmissive to light in the wavelength range from ultraviolet through green, wherein the silicone material maintains its transmissiveness when exposed to a temperature of 100° C.

10. The LED component of claim **1** further comprising: a die placement area having a reflective surface.

11. The LED component of claim **1** wherein the optic is configured as a lens.

12. The LED component of claim **11** wherein the lens has a convex shape.

13. A light emitting diode (LED) component comprising:

an LED chip emitting light having a wavelength in a range of 200 to 570 nanometers; and

an optic, configured as a lens, encapsulating the LED chip, the optic comprising:

an outer optically transmissive shell of rigid material; a quantity of resilient, optically transmissive material inside the shell, the resilient, optically transmissive material comprising a silicone material being transmissive to light in the wavelength range from ultraviolet through green, wherein the silicone material maintains its transmissiveness when exposed to a temperature of 100° C.; and

a die placement area having a reflective surface.

14. The LED component of claim **13** further comprising particles of light-emitting phosphor embedded in the silicone material.

15. The LED component of claim **13** further comprising an optical dispersant mixed into the silicone material.

16. The LED component of claim **13** further comprising:

particles of light-emitting phosphor embedded in the silicone material; and an optical dispersant mixed into the silicone material.

17. The LED component of claim **13** wherein the rigid material is selected from a group consisting of silicone, cyclic-olefin copolymer, optical plastic, glass, ceramic, and aluminum oxide.

* * * * *

Exhibit E

US006717353B1

(12) **United States Patent**
Mueller et al.

(10) **Patent No.: US 6,717,353 B1**
(45) **Date of Patent: Apr. 6, 2004**

(54) **PHOSPHOR CONVERTED LIGHT EMITTING DEVICE**

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(73) Assignee: **Lumileds Lighting U.S., LLC**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/272,150**

(22) Filed: **Oct. 14, 2002**

(51) **Int. Cl.**[7] **H01J 1/62**

(52) **U.S. Cl.** .... **313/501**; 313/485; 313/486; 313/487; 313/502; 313/503; 252/301.4 R; 252/301.4 S

(58) **Field of Search** .... 313/501, 502, 313/503, 485, 486, 487; 252/301.4 R, 301.4 S

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U.S. PATENT DOCUMENTS

2003/0141506 A1 * 7/2003 Sano et al. 257/78

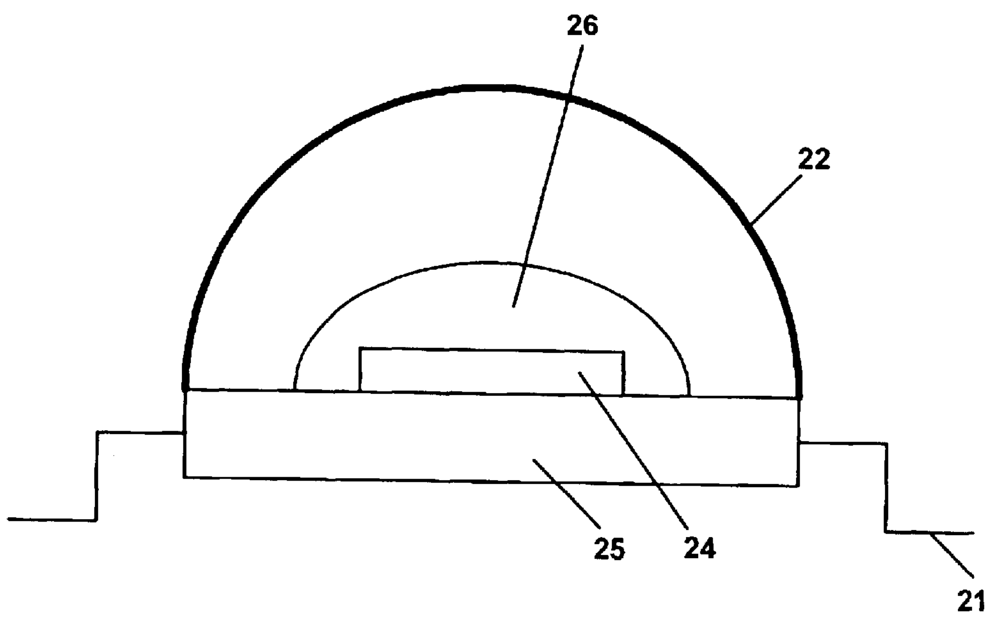
* cited by examiner

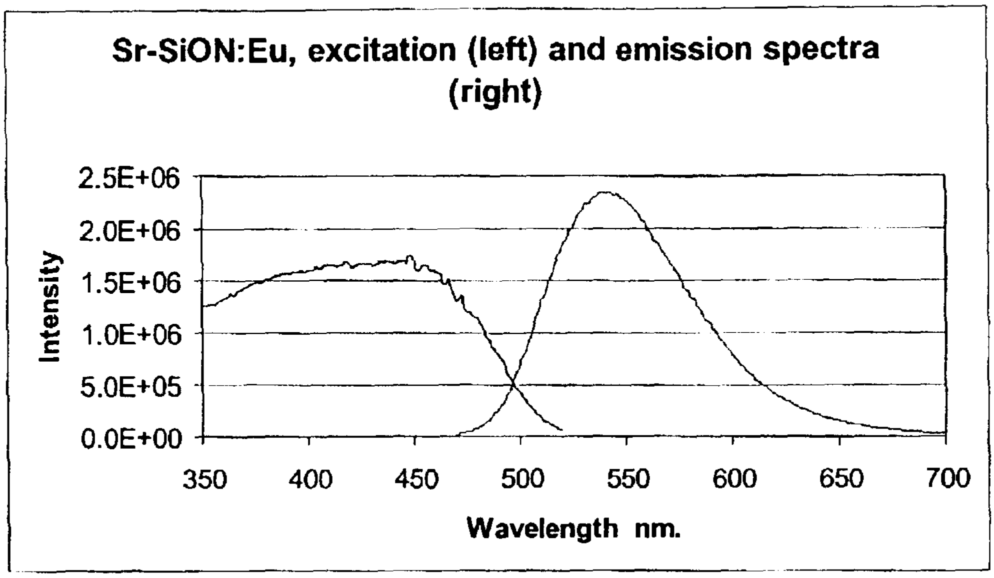
Primary Examiner—Vip Patel
Assistant Examiner—Holly Harper
(74) *Attorney, Agent, or Firm*—Patent Law Group LLP; Rachel V. Leiterman

(57) **ABSTRACT**

A device includes a semiconductor light emitting device and a wavelength-converting material comprising Sr—SiON:Eu^{2+}. The Sr—SiON:Eu^{2+} wavelength-converting material absorbs light emitted by the light emitting device and emits light of a longer wavelength. The Sr—SiON:Eu^{2+} wavelength-converting material may be combined with other wavelength-converting materials to make white light. In some embodiments, the Sr—SiON:Eu^{2+} wavelength-converting layer is combined with a red-emitting wavelength-converting layer and a blue light emitting device to generate emission in colors, which are not achievable by only mixing primary and secondary wavelengths. In some embodiments, the Sr—SiON:Eu^{2+} wavelength-converting layer is combined with a red-emitting wavelength-converting layer, a blue-emitting wavelength-converting layer, and a UV light emitting device.

23 Claims, 5 Drawing Sheets




Sr-SiON:Eu, excitation (left) and emission spectra (right)
Intensity
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2.0E+06
1.5E+06
1.0E+06
5.0E+05
0.0E+00
350
400
450
500
550
600
650
700
Wavelength nm.

Fig. 1

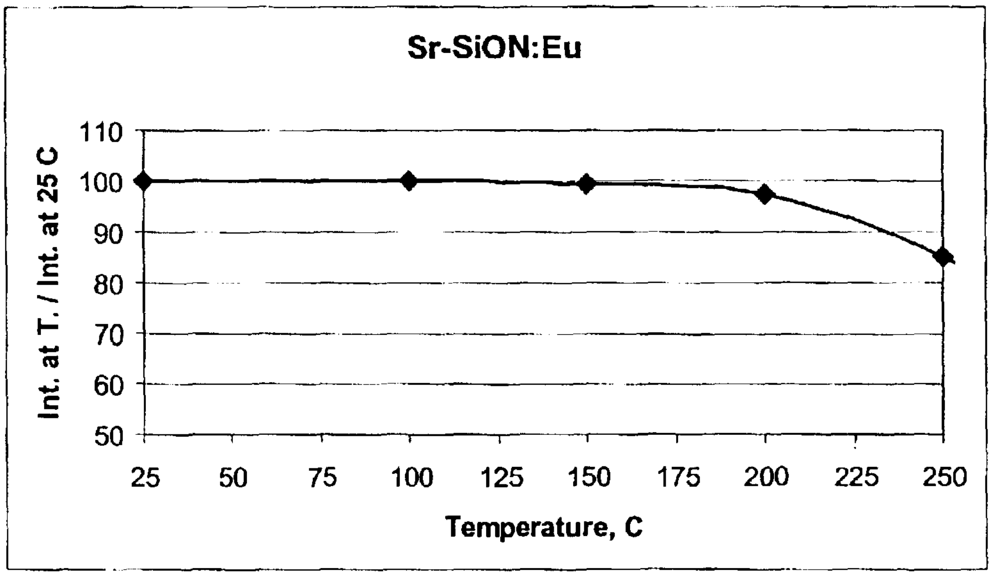

Sr-SiON:Eu
Int. at T. / Int. at 25 C
110
100
90
80
70
60
50
25
50
75
100
125
150
175
200
225
250
Temperature, C

Fig. 2

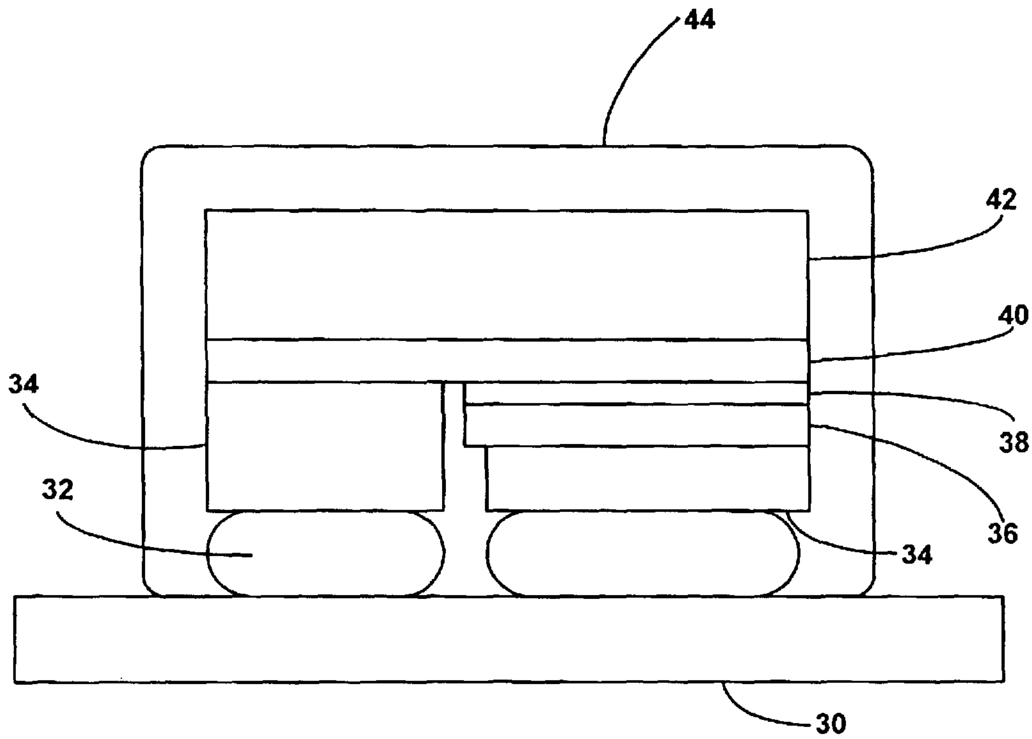


Fig. 3

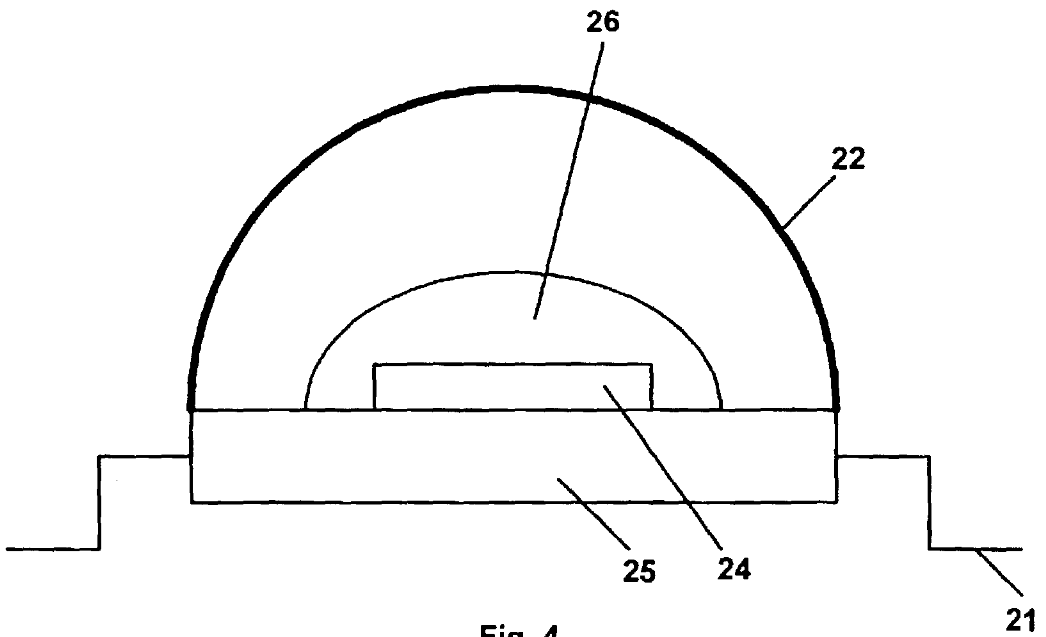
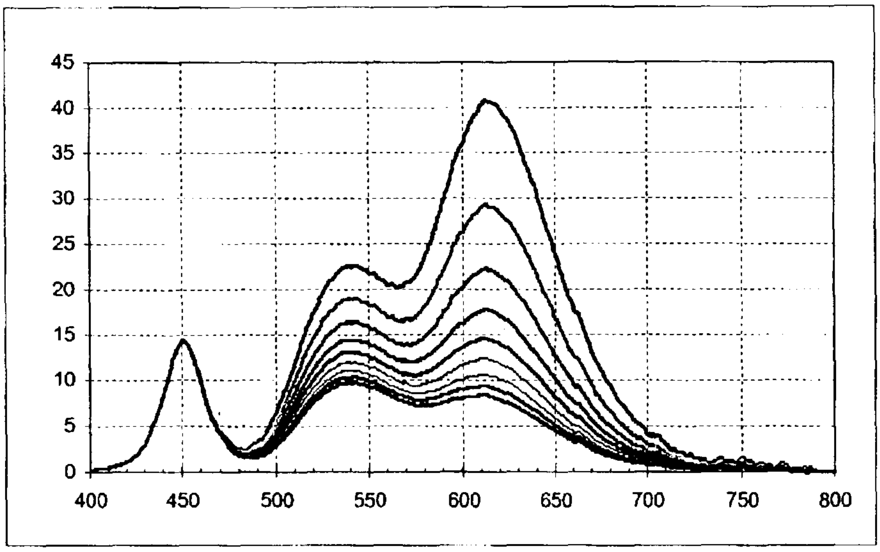


Fig. 4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35
30
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15
10
5
0
400
450
500
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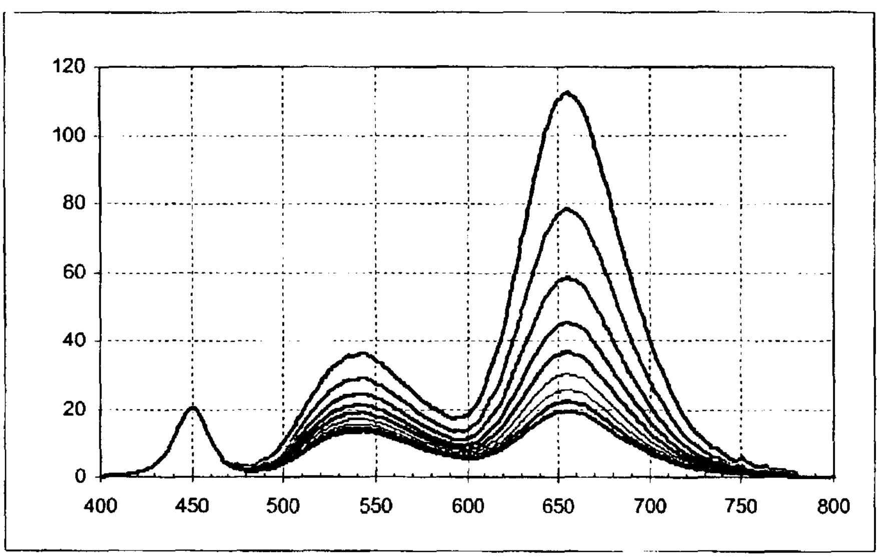
600
650
700
750
800

Fig. 5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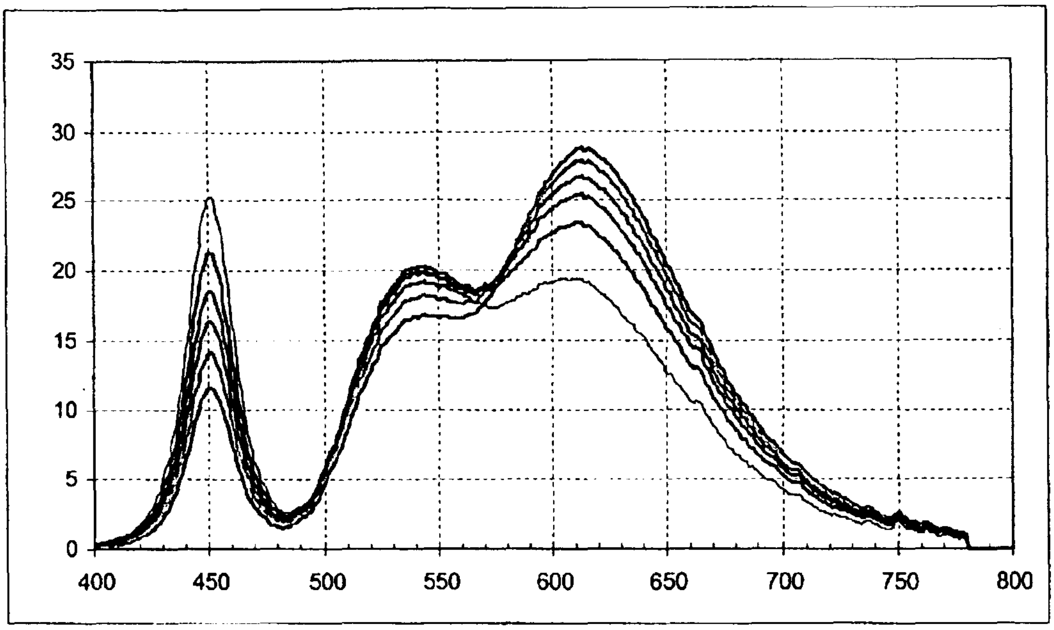
60
40
20
0
400
450
500
550
600
650
700
750
800

Fig. 6


35
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15
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5
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400
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550
600
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700
750
800

Fig. 7

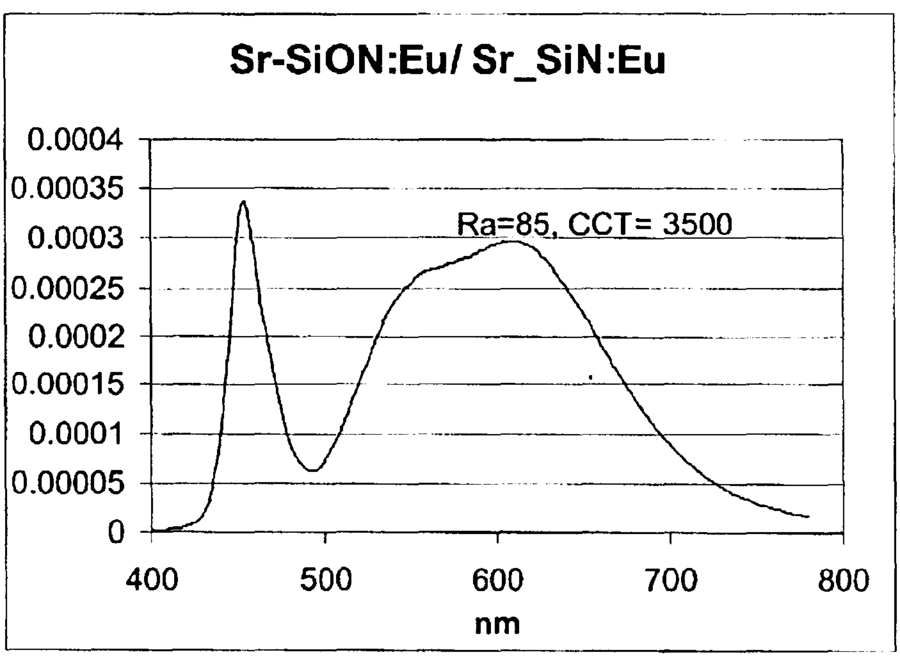
Sr-SiON:Eu/ Sr_SiN:Eu
Ra=85, CCT= 3500
0.0004
0.00035
0.0003
0.00025
0.0002
0.00015
0.0001
0.00005
0
400
500
600
700
800
nm

Fig. 8

PHOSPHOR CONVERTED LIGHT EMITTING DEVICE

BACKGROUND

1. Field of Invention

The invention relates generally to wavelength-converted light emitting devices.

2. Description of Related Art

Light emitting devices including light emitting diodes are well known solid state devices that can generate light having a peak wavelength in a specific region of the light spectrum. LEDs are typically used as illuminators, indicators, and displays. LEDs based on the III-nitride materials system have been developed that can efficiently emit light in a relatively narrow band around a peak wavelength in the blue to UV range of the spectrum. Since blue-UV light has a higher photo energy relative to other colors of visible light, such light generated by III-nitride LEDs can be readily converted to produce light having a longer wavelength. It is well known in the art that light having a first peak wavelength ("primary light") can be converted into light having a longer peak wavelength ("secondary light") using a process known as luminescence. The luminescence process involves absorbing the primary light by a photoluminescent phosphor material, which excites the atoms of the phosphor material, and emits the secondary light. The peak wavelength and the band of wavelengths around it (in short wavelength) of the secondary light will depend on the phosphor material. The type of phosphor material can be chosen to yield secondary light having a particular peak wavelength. Needed in the art are wavelength-converting materials (wavelength converters) that efficiently convert light in desired wavelength ranges and can withstand the same operating temperatures as the III-nitride light emitting devices.

SUMMARY

In accordance with embodiments of the invention, a device includes a semiconductor light emitting device and a wavelength-converting material comprising Sr—SiON:Eu^{2+}. The Sr—SiON:Eu^{2+} wavelength-converting material absorbs light emitted by the light emitting device and emits light of a longer wavelength. In some embodiments, the Sr—SiON:Eu^{2+} wavelength-converting material is combined with a red-emitting wavelength-converting material and a blue light emitting device. In some embodiments, the Sr—SiON:Eu^{2+} wavelength-converter is combined with a red-emitting wavelength-converter, a blue-emitting wavelength-converter, and a UV light emitting device.

The use of Sr—SiON:Eu^{2+} as a green wavelength-converting material offers several advantages including high chemical and thermal stability, enhanced color rendering in white devices due to a relatively wide emission band, and potentially inexpensive synthesis.

The designator Sr—SiON:Eu^{2+} is used here and in the following for materials of the general formula $(Sr_{1-a-b}Ca_bBa_c)Si_xN_yO_z:Eu_a$ (a=0.002–0.2, b=0.0–0.25, c=0.0–0.25, x=1.5–2.5, y=1.5–2.5, z=1.5–2.5).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates the excitation and emission spectra of Sr—SiON:Eu^{2+}.

FIG. **2** illustrates the emission intensity as a function of temperature for Sr—SiON:Eu^{2+}, relative to the intensity at room temperature.

FIG. **3** illustrates an embodiment of a light emitting device incorporating a light emitting diode and Sr—SiON:Eu^{2+}.

FIG. **4** illustrates an alternative embodiment of a light emitting device incorporating a light emitting diode and Sr—SiON:Eu^{2+}.

FIGS. **5–7** illustrate calculated emission spectra of several white devices including SiON:Eu^{2+}, showing emission in arbitrary units versus wavelength in nanometers.

FIG. **8** illustrates an observed emission spectrum of a white device including a blue light emitting diode, Sr—SiON:Eu^{2+} and $Sr_2Si_5N_8:Eu^{2+}$.

DETAILED DESCRIPTION

In accordance with embodiments of the invention, a light source includes a luminescent material for emitting green light. The luminescent material is Eu^{2+} activated Sr—SiON having the formula $(S_{1-a-b}Ca_bBa_c)Si_xN_yO_z:Eu_a$ (a=0.002–0.2, b=0.0–0.25, c=0.0–0.25, x=1.5–2.5, y=1.5–2.5, z=1.5–2.5) and excitable by light with a wavelengt ranging from UV through blue. FIG. **1** illustrates the emission and excitation spectrum of Sr—SiON:Eu^{2+}.

Sr—SiON:Eu^{2+} has several advantages. Sr—SiON:Eu^{2+} has low thermal quenching and is stable at high temperatures, permitting its use with light sources that operate at high temperatures. For example, at 170° C. Sr—SiON:Eu^{2+} still exhibits nearly 100% of the room temperature emission intensity. In contrast, other green phosphors are quenched to 50% of the room temperature emission intensity at 170° C. FIG. **2** illustrates the emission intensity (normalized to room temperature emission intensity) as a function of temperature for Sr—SiON:Eu^{2+}. Sr—SiON:Eu^{2+} also has excellent chemical stability and is potentially inexpensive to synthesize. In addition, in white light applications, Sr—SiON:Eu^{2+} has a relatively wide emission band which enhances color rendering. The lumen equivalent is about 550 lm/W and leads to high overall luminous conversion efficiency of the respective devices. The parity-allowed radiative transition in the Eu^{2+} ion is fast decaying (decay time less than 1 microsecond, which is advantageous for many applications.

The Sr—SiON:Eu^{2+} material is suitable for use with any light source emitting light having a wavelength capable of exciting the Sr—SiON:Eu material, including, for example, discharge lamps and blue- and UV-emitting semiconductor light emitting devices such as light emitting diodes and laser diodes. FIG. **3** illustrates a first embodiment of a device incorporating a Sr—SiON:Eu^{2+} material. Sr—SiON:Eu^{2+} layer **44** covers a light emitting diode including an n-type region **40**, and active region **38**, and a p-type region **36** formed over a substrate **42**. Contacts **34** are formed on the n- and p-type regions, then the light emitting diode is flipped over and electrically and physically connected to a submount **30** by interconnects **32**. Sr—SiON:Eu^{2+} layer **44** may be deposited by, for example, electrophoretic deposition, stenciling, or screen printing. Stenciling is described in "Stenciling Phosphor Coatings On Flip Chip Phosphor-LED Devices," U.S. application Ser. No. 09/688,053, and electrophoretic deposition is described in "Using Electrophoresis To Produce A Conformally Coated Phosphor-Converted Light Emitting Semiconductor Structure," U.S. application Ser. No. 09/879,627. Both applications are incorporated herein by reference. The light emitting device need not be a flip chip and may be oriented such that light is extracted from the device through the semiconductor device layers, rather than through the substrate.

FIG. **4** illustrates a second embodiment of a device incorporating a Sr—SiON:Eu^{2+} material. The device of FIG. **4** is a packaged light emitting diode including a light emitting diode **24** optionally mounted on a submount (not shown), supported by a base **25**, and electrically connected to leads **21**. A lens **22** protects light emitting diode **24**. Sr—SiON:Eu^{2+} may be dispersed in an encapsulant material **26** that is injected in a space between lens **22** and light emitting diode **24**. The encapsulant may be, for example, silicone, epoxy, or any other organic or inorganic material, which is suitable for incorporating the light converter(s) and adheres to the primary light emitting device.

In some embodiments of the devices illustrated in FIGS. **3** and **4**, the Sr—SiON:Eu^{2+} material is the only wavelength-converting material. The amount of unconverted light from the light emitting diode mixing with the light emitted by the Sr—SiON:Eu^{2+} is determined by the characteristics, such as thickness and amount of Sr—SiON:Eu^{2+}, of the layer containing the Sr—SiON:Eu^{2+}. In some embodiments, a filter material such as a dye may be incorporated into the device for filtering out any light unconverted by the Sr—SiON:Eu^{2+}. The use of a filter material is described in more detail in Application Serial No. 10/260,090, titled "Selective Filtering of Wavelength-converted Semiconductor Light Emitting Devices," filed Sep. 27, 2002, and incorporated herein by reference. For a blue-emitting light emitting diode, the light may range from bluish-green (some unconverted light from the light emitting diode allowed to escape) to green (no unconverted light allowed to escape). Such devices may be useful for applications requiring green light, such as, for example, green traffic lights or a backlight for a display. In one embodiment, the device is designed to generate green light of a centroid wavelength of 556 nm.

In some embodiments of the devices illustrated in FIGS. **3** and **4**, the Sr—SiON:Eu^{2+} is mixed with one or more additional wavelength-converting materials. Such devices may be used to create white light or to create light of a color that is difficult to achieve with a single wavelength-converting material. Each wavelength-converting material may be pumped by either light emitted by the light emitting diode or by light emitted by one of the other wavelength-converting materials. In some embodiments, Sr—SiON:Eu^{2+} may be used in combination with a red-emitting phosphor and a blue light emitting diode to produce white light. Examples of suitable red-emitting phosphors include nitride silicate phosphors and sulfide phosphors such as $(Sr_{1-a-b-c}Ba_bCa_c)_2Si_5N_8:Eu_a$ (a=0.002–0.2, b=0.0–1.0, c=0.0–1.0); $(Ca_{1-x-a}Sr_x)S:Eu_a$ (a=0.0005 . . . 0.01, x=0.0–1.0); $Ca_{1-a}SiN_2:Eu_a$ (a=0.002–0.2) and $(B_{1-x-a}Ca_x)Si_7N_{10}:Eu_a$ (a=0.002–0.2, x=0.0–0.25).

FIGS. **5**–**7** illustrate calculated emission spectra of white light emitting devices that combine a blue light emitting diode, Sr—SiON:Eu^{2+}, and a red-emitting phosphor. Each figure is accompanied by a table listing, for each spectrum, the color temperature CCT, the average color rendering index Ra, and the x and y coordinates on a chromaticity diagram. In each of

FIGS. **5**–**7**, the top most spectrum corresponds to the lowest color temperature and the bottom most spectrum corresponds to the highest color temperature.

FIG. **5** illustrates emission spectra of white light emitting devices with SrS:Eu^{2+} as the red emitting phosphor. The devices illustrated in FIG. **5** exhibit no tint and have very high color rendering indices, for example between **85** and **90**, at low color temperature. The table below lists CCT, Ra, and x and y for each of the spectra illustrated in FIG. **5**:

x	y	CCT,K	Ra
0.4599	0.4107	2709	90
0.4369	0.4042	3001	89
0.4171	0.3964	3301	88
0.3999	0.3882	3601	86
0.3850	0.3798	3900	85
0.3721	0.3716	4200	84
0.3609	0.3639	4498	84
0.3511	0.3566	4797	83
0.3425	0.3499	5096	82

FIG. **6** illustrates emission spectra of white light emitting devices with CaS:Eu^{2+} as the red emitting phosphor. The devices illustrated in FIG. **6** also exhibit no tint, but have significantly lower color rendering indices, for example between 62 and 72, at low color temperature. The table below lists CCT, Ra, and x and y for each of the spectra illustrated in FIG. **6**:

x	y	CCT,K	Ra
0.4599	0.4107	2709	62
0.4369	0.4042	3001	66
0.4171	0.3964	3300	68
0.3999	0.3881	3600	70
0.3850	0.3798	3900	72
0.3721	0.3716	4199	74
0.3609	0.3639	4499	75
0.3511	0.3566	4797	76
0.3424	0.3498	5097	77

The use of (Sr,Ca)S:Eu^{2+} as the red emitting phosphor is expected to offer better color rendering than CaS:Eu^{2+} devices illustrated in FIG. **6** and worse color rendering than SrS:Eu^{2+} devices illustrated in FIG. **5**.

FIG. **7** illustrates emission spectra of white light emitting devices with $Sr_2Si_5N_8:Eu^{2+}$ as the red emitting phosphor. The devices illustrated in FIG. **7** exhibit no tint and have color rendering indices comparable to those of the SrS:Eu^{2+} devices discussed above in reference to FIG. **5**. In some devices, $Sr_2Si_5N_8:Eu^{2+}$ is favored as the red emitting phosphor due to its favorable chemical properties. The table below lists CCT, Ra, and x and y for each of the spectra illustrated in FIG. **7**:

x	y	CCT,K	Ra
0.4599	0.4107	2709	87
0.4442	0.4065	2901	86
0.4300	0.4017	3101	86
0.4171	0.3964	3300	85
0.3999	0.3881	3600	84
0.3721	0.3717	4200	82

FIG. **8** illustrates an observed emission spectrum for a device including a blue light emitting diode, Sr—SiON:Eu^{2+} and $Sr_2Si_5N_8:Eu^{2+}$.

In some embodiments, Sr—SiON:Eu^{2+} may be used in combination with a red-emitting phosphor, a blue-emitting phosphor, and a UV light emitting diode to produce white light. Examples of suitable blue-emitting phosphors are $(Sr_{1-x-a}Ba_x)_3MgSi_2O_8:Eu_a$ (a=0.002–0.2, x=0.0–1.0); $(Sr_{1-x-a}Ba_x)P_2O_7:Eu_a$ (a=0.002–0.2, x=0.0–1.0); $(Sr_{1-x-a}Ba_x)_4Al_{14}O_{25}:Eu_a$ (a=0.002–0.2, x=0.0–1.0);

$La_{1-a}Si_3N_5$:Ce_a (a=0.002–0.5); $(Y_{1-a})_2SiO_5$:Ce_a (a=0.002–0.5); and $(Ba_{1-x-a}Sr_x)$ $MgAl_{10}O_{17}$:Eu_a (a=0.01–0.5, x=0.0–0.5). The amounts of Sr—SiON:Eu2+, red-emitting phosphor, and blue-emitting phosphor are adjusted to create white light and to minimize the amount of UV light escaping unconverted from the device. In embodiments with multiple wavelength-converting materials, the Sr—SiON:Eu^{2+} and other wavelength-converting materials may be separate layers formed one over the other or may be mixed in a single wavelength-converting material layer. For example, in a UV device according to FIG. **3** with red-, green-, and blue-emitting phosphors, the different phosphors may be mixed and deposited in a single layer, or may be deposited in three separate layers, usually blue adjacent to the light emitting diode, then green, then red. In a device according to FIG. **4**, the phosphors may be mixed in a single encapsulant layer, or three layers of encapsulant, each containing a different phosphor, may be deposited over the light emitting diode. The Sr—SiON:Eu^{2+} and any other wavelength-converting material may also be deposited as a thin film on at least one of the surfaces of the light emitting device.

In one example, Sr—SiON:Eu^{2+} may be synthesized as follows: 208.98 g (1.415 mol) $SrCO_3$ is mixed with 12.3 g (0.059 mol) EuF_3 and 206.8 g (4.423 mol) $SiN_{4/3}$ (min. 98% purity) in dry ethanol under argon. The ethanol is removed in a stream of argon and the dried powder mixture is then fired at 1400° C. for 1 hr in an H_2/N_2 atmosphere over charcoal in a tungsten boat. After milling, the powder is fired at 1500° C. for 1 hr in an H_2/N_2 atmosphere, then milled and washed with water several times.

leaving described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

What is being claimed is:

1. A device comprising:

a semiconductor light emitting device capable of emitting light of a first wavelength; and

a first wavelength-converting material comprising Sr—SiON:Eu^{2+}, the first wavelength-converting material disposed to absorb light of the first wavelength;

wherein the first wavelength-converting material absorbs light of the first wavelength and emits light of a second wavelength longer than the first wavelength.

2. The device of claim **1** wherein the first wavelength ranges from blue to UV.

3. The device of claim **1** wherein the second wavelength is green.

4. The device of claim **1** further comprising a second wavelength-converting material, wherein the second wavelength-converting material absorbs light of one of the first wavelength and the second wavelength, and emits light of a third wavelength longer than the second wavelength.

5. The device of claim **4** wherein the third wavelength is red.

6. The device of claim **4** wherein the second wavelength-converting material is selected from the group consisting of $(Sr_{1-a-b-c}Ba_bCa_c)_2Si_5N_8$:$Eu_a$ (a=0.002–0.2, b=0.0–1.0, c=0.0–1.0); $(Ca_{1-x-a}Sr_x)S$:Eu_a (a=0.0005 . . . 0.01, x=0.0–1.0); $Ca_{1-a}SiN_2$:Eu_a (a0.002–0.2); and $(Ba_{1-x-a}Ca_x)$ Si_7N_{10}:Eu_a (a=0.002–0.2, x=0.0–0.25).

7. The device of claim **4** wherein the first wavelength is blue.

8. The device of claim **4** further comprising a third wavelength-converting material, wherein the third wavelength-converting material absorbs light of the first wavelength and emits light of a fourth wavelength longer than the first wavelength and shorter than the second wavelength.

9. The device of claim **8** wherein the first wavelength is UV, the second wavelength is green, the third wavelength is red, and the fourth wavelength is blue.

10. The device of claim **8** wherein the third wavelength-converting material is selected from the group consisting of $(Sr_{1-x-a}Ba_x)_3MgSi_2O_8$:$Eu_a$ (a=0.002–0.2, x=0.0–1.0); $(Sr_{1-x-a}Ba_x)_2P_2O_7$:Eu_a (a=0.002–0.2, x=0.0–1.0); $(Sr_{1-x'a}Ba_x)_4Al_{14}O_{25}$; Eu_a (a=0.002–0.2, x=0.0–1.0); La_{1-a} Si_3N_5:Ce_a (a=0.002–0.5); $(Y_{1-a})_2SiO_5$:Ce_a (a=0.002–0.5); and $(Ba_{1-x-a}Sr_x)MgAl_{10}O_{17}$:$Eu_a$ (a=0.01–0.5, x=0.0–0.5).

11. The device of claim **8** wherein the amounts of first wavelength-converting material, second wavelength-converting material, and third wavelength-converting material are selected to prevent light of the first wavelength from escaping the device.

12. The device of claim **1** further comprising a filter material capable of absorbing light of the first wavelength.

13. The device of claim **1** wherein the second wavelength comprises a centroid wavelength of 556 nm.

14. The device of claim **1** wherein the light emitting device is a III-nitride light emitting diode.

15. The device of claim **1** wherein the first wavelength-converting material is coated on a top surface and a side surface of the light emitting device.

16. The device of claim **1** further comprising:

a pair of leads electrically connected to the light emitting device; and

a lens disposed over the light emitting device.

17. The device of claim **16** wherein the first wavelength-converting material is dispersed in an encapsulant disposed between the light emitting device and the lens.

18. The device of claim **16** wherein the light emitting device is mounted such that light is extracted from the light emitting device through a transparent substrate.

19. A device comprising:

a III-nitride light emitting diode;

a green emitting phosphor comprising Sr—SiON:Eu^{2+}; and

a red emitting phosphor;

wherein the green emitting phosphor and the red emitting phosphor are disposed over the III-nitride light emitting diode.

20. The device of claim **19** wherein the red emitting phosphor is selected from the group consisting of $(Sr_{1-a-b-c}Ba_bCa_c)_2Si_5N_8$:$Eu_a$ (a=0.002–0.2, b=0.0–1.0, c=0.0 –1.0); $(Ca_{1-x-a}Sr_x)S$:Eu_a (a=0.0005 . . . 0.01, x=0.0–1.0); $Ca_{1-a}SiN_2$:Eu_a (a=0.002–0.2); and $(Ba_{1-x-a}Ca_x)$ Si_7N_{10}:Eu_a (a=0.002–0.2, x=0.0–0.25).

21. The device of claim **19** further comprising a blue emitting phosphor disposed over the III-nitride light emitting diode.

22. The device of claim **21** wherein the blue emitting phosphor is selected from the group consisting of $(Sr_{1-x-a}Ba_x)_3MgSi_2O_8$:$Eu_a$ (a=0.002–0.2, x=0.0–1.0); $(Sr_{1-x-a}Sr_x)_2P_2O_7$:Eu_a (a=0.002–0.2, x=0.0–1.0); $(Sr_{1-x-a}Ba_x)_4Al_{14}O_{25}$:$Eu_a$ (a=0.002–0.2, x=0.0–1.0); $La_{1-a}Si_3N_5$:Ce_a (a=0.002–0.5); $(Y_{1-a})_2SiO_5$:Ce_a (a=0.002–0.5); and $(Ba_{1-x-a}Sr_x)$ $MgAl_{10}O_{17}$:Eu_a (a=0.01–0.5, x=0.0–0.5).

23. The device of claim **19** wherein the green emitting phosphor absorbs light emitted by the blue emitting phosphor and emits green light.

* * * * *

Exhibit F

United States Patent [19]
Gerard et al.

[11] **Patent Number: 5,075,742**
[45] **Date of Patent: Dec. 24, 1991**

[54] **SEMICONDUCTOR STRUCTURE FOR OPTOELECTRONIC COMPONENTS WITH INCLUSIONS**

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[73] Assignee: **French State represented by the Minister of the Post, Telecommunications and Space**, Issy-Les-Moulineaux, France

[21] Appl. No.: **639,530**

[22] Filed: **Jan. 10, 1991**

[30] **Foreign Application Priority Data**

Jan. 10, 1990 [FR] France 90 00229

[51] **Int. Cl.**[5] **H01L 33/00**
[52] **U.S. Cl.** **357/17**; 372/48; 372/43; 372/45; 357/16
[58] **Field of Search** 357/16, 17; 372/43, 372/44, 45, 46, 47, 48, 49, 50

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Primary Examiner—William Mintel
Attorney, Agent, or Firm—Fleit, Jacobson, Cohn, Price, Holman & Stern

[57] **ABSTRACT**

The object of the invention is to reduce the influence of dislocations on the functioning of structures for optoelectronic component, such as laser, made from semiconductor materials. Accordingly, one of the lasers of such a structure comprises three-dimensional inclusions in a semiconductor material with a thinner forbidden band than the forbidden band of the layer material. The inclusions are e.g. distributed over several planes of the active layer of a laser, and may be in InAs introduced into a layer in GaAs.

5 Claims, 3 Drawing Sheets

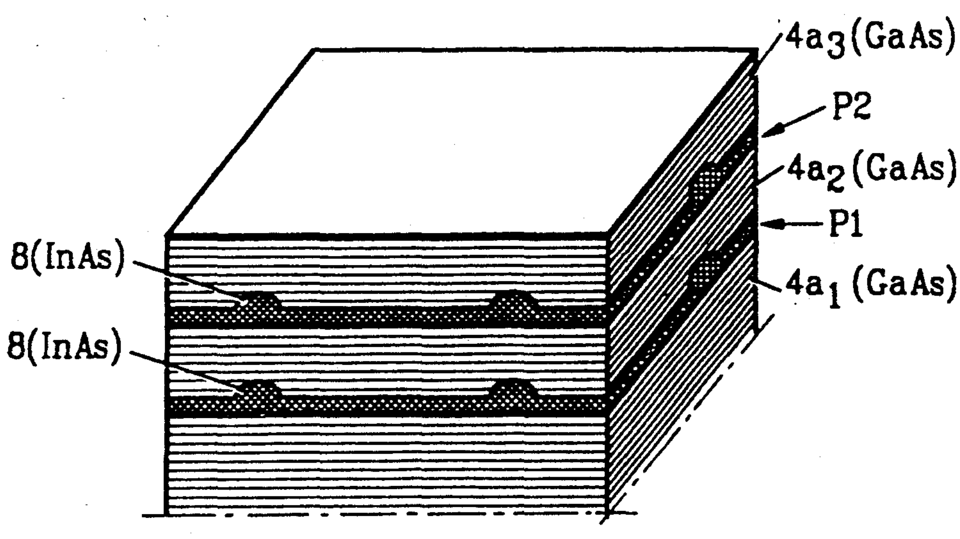
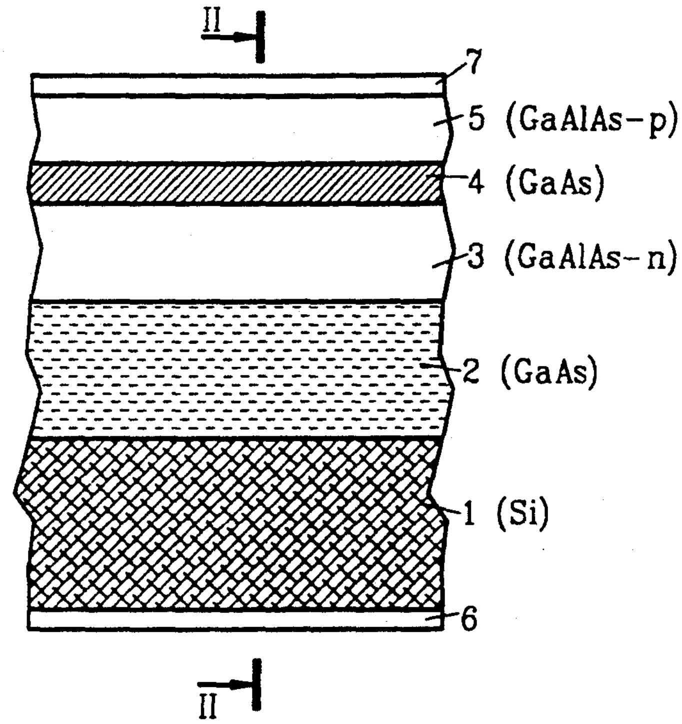


FIG. 1 (PRIOR ART)



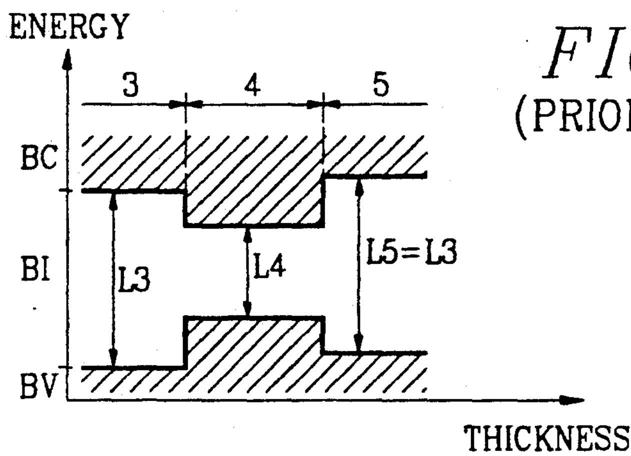


FIG. 2 (PRIOR ART)

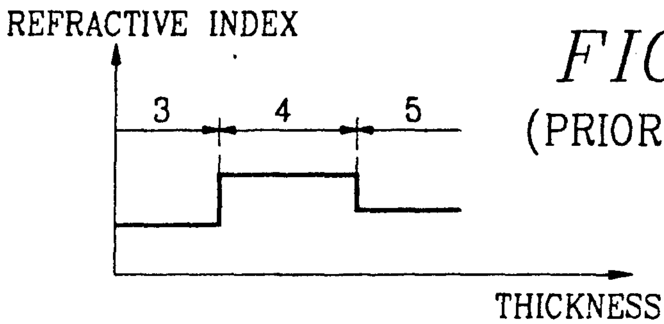


FIG. 3 (PRIOR ART)

FIG. 4

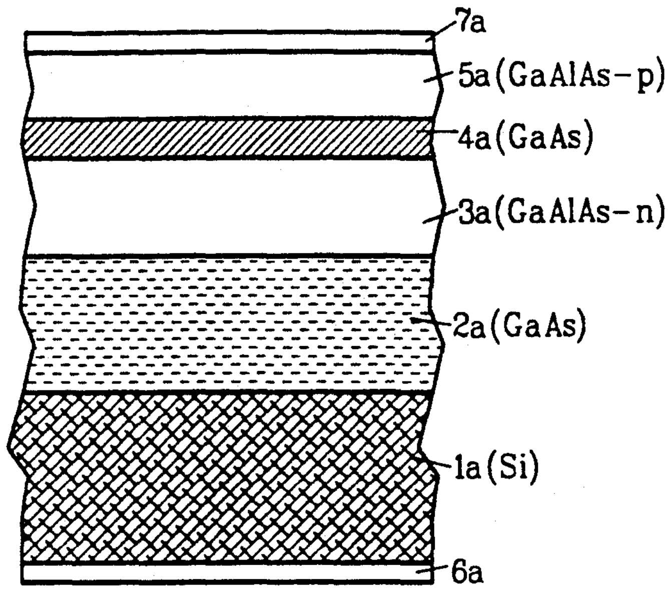


FIG. 5

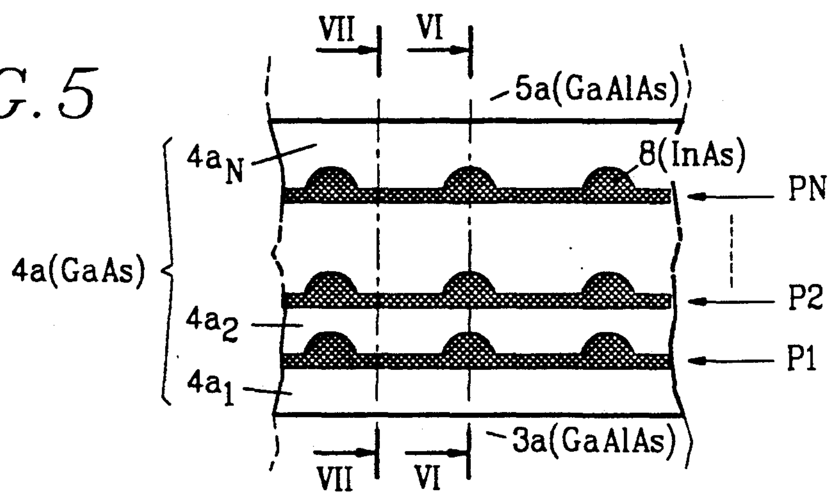


FIG. 6

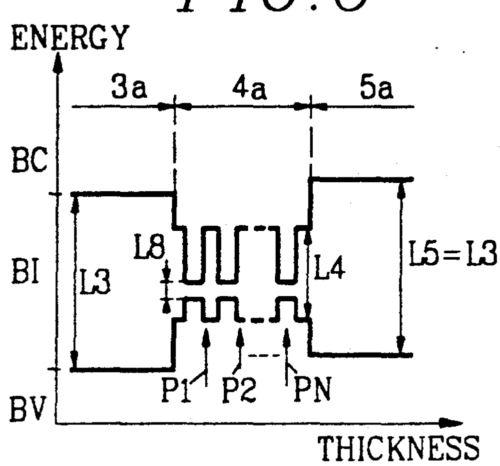


FIG. 7

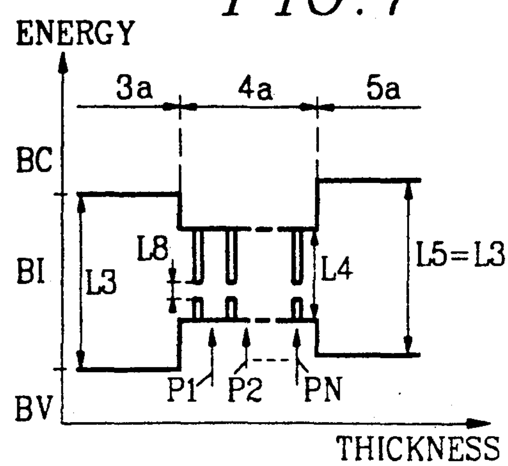


FIG. 8

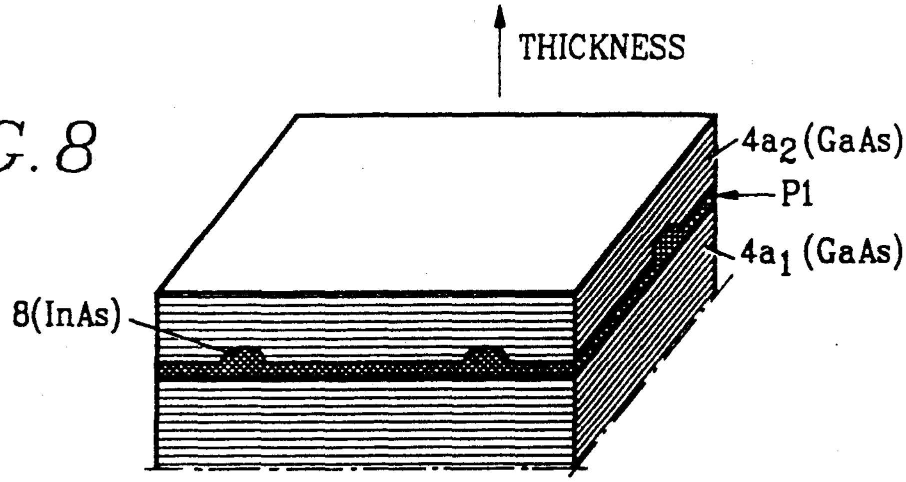


FIG. 9

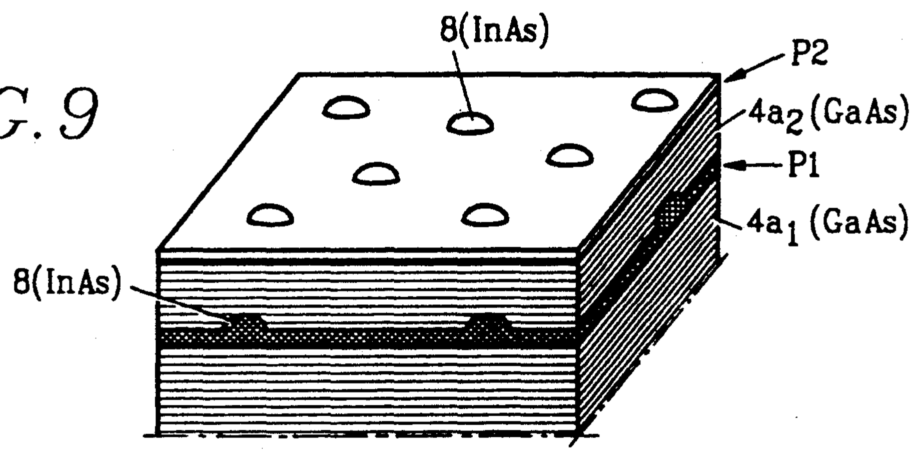
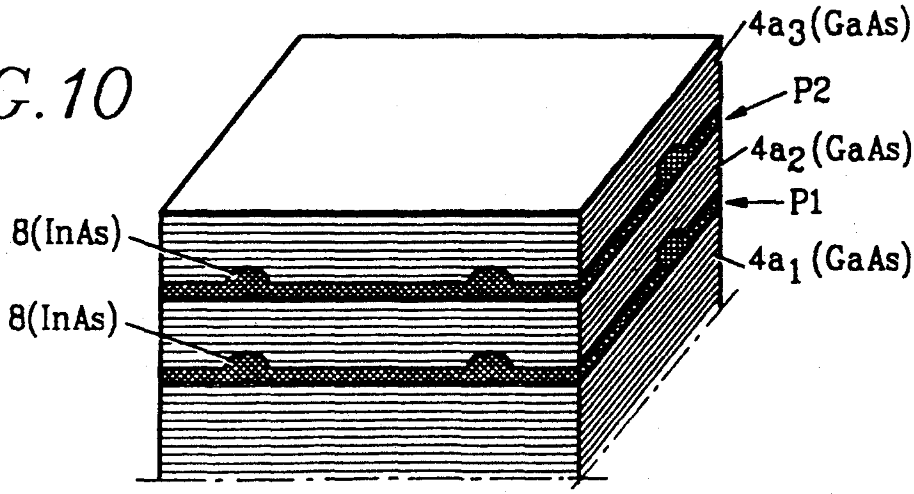


FIG. 10



SEMICONDUCTOR STRUCTURE FOR OPTOELECTRONIC COMPONENTS WITH INCLUSIONS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a multilayer structure in semiconductor material, especially for a solid state laser. More generally, the invention has applications in optoelectronics, and monolithic integration in opto- and microelectronics.

2. State of the Prior Art

Silicon Si and gallium arsenide GaAs are currently the most widely used semiconductor materials. Although a very high scale of integration has been obtained in microelectronics using silicon, optoelectronics has developed from heterostructure lasers with semiconductor materials from groups III and V of the Mendeleevian classification, such as GaAs/GaAlAs on GaAs substrate and such as GaInAs/AlInAs or GaInAs/InP on InP substrate. The integration on a common substrate of optoelectronic and microelectronic devices with complementary functions produced from different materials, e.g. material from groups III and V and silicon, is a particularly appealing perspective which has given rise to intensive research work in recent years.

A silicon substrate has numerous advantages: solidity, perfection, high thermal conductivity, low cost, etc. It is mainly the deposition of III-V compounds on silicon that has mainly been studied. Much progress has been achieved concerning this type of epitaxial growth and has enabled the obstacles encountered to be partially overcome: the difficulty in depositing a polar material such as III-V semiconductors on a non-polar material such as silicon, and the major lattice parameter difference between these, e.g. 4% for GaAs on silicon.

In particular, this mismatch implies the presence of a very high quantity of dislocations in the first tens of nanometers of the epitaxially deposited material. These dislocations can be due to the preparation of the state of the surface upon which the epitaxial growth is carried out, and/or to a degradation over time of the crystallographic quality of the epitaxial semiconductor. Whatever their origin, these dislocations beget local inhomgeneities and can develop.

For instance, when the crystalline lattice parameter of a layer is lower than that of a second layer, the first layer is subjected to tension and dislocations occur in the layer interface. If the first layer is the active layer of a laser component, the performances of the laser component are highly dependent on the number of dislocations present. These defects do, of course, affect the threshold current of this component with minority carriers, but also affect its ageing. When the component is operating, the presence of an electric field, and of high photon and carrier densities also help the displacement of existing defects and assist the generation of new defects.

For conventional optoelectronics applications, optoelectronic components are produced from III-V semiconductor heterostructures, such as GaAs/GaAlAs on GaAs substrate and such as GaInAs/AlInAs or GaInAs/InP on InP substrate. The dislocation rates obtained during the growth of these structures by conventional techniques, like molecular beam epitaxy and vapor phase epitaxy from organometallic compounds, are in the region of $10^4/cm^2$. The rates are compatible with proper functioning of these optoelectronic components, as witnessed by the large-scale commercial use of some of these, such as GaAs/GaAlAs laser diodes with 0.85-μm wavelength; however, in certain cases, the displacement and multiplication of the dislocations during operating of the components have been observed and correlated with lifetime problems of these components. The dislocation-related problems, latent in this instance, become crucial if these defects are more numerous in the material used.

In the case of the growth of a III-V material on silicon, it is therefore primordial to seek as low a dislocation rate as possible in the structure. The dislocation rates in the superficial layer of the material remain in the region of 10^6 to 10^7 dislocations per cm^2. The number of dislocations tends to decrease with the thickness of the deposit, but depositions cannot exceed 4 to 5 microns of material. Beyond that, the very major difference in coefficients of expansion between the silicon and the III-V material entails the formation of numerous cracks in the epitaxial layer when the growth temperature, in the region of 500° to 600° C., drops to room temperature. This failure of the attempts to reduce the number of dislocations is charged with consequences as regards the stability of laser components fabricated on silicon substrates.

To illustrate the results obtained, consideration is directed to the case of a GaAs structure on Si, which is the case that has been studied most intensely. No instance of room-temperature continuous-emission operation has been observed to date for double heterostructure lasers, as the component degrades below the laser threshold. On the other hand, a room-temperature operation in the pulsed mode, then in the continuous mode for short periods in the region of one minute has been observed for quantum well lasers, i.e., structures with confinement separated by index gradient. The reduction of the dimensions of the active layer is therefore clearly beneficial for the operating of the optoelectronic component. This result is related to several favourable factors. The use of the separate confinement concept brings about a reduction of the threshold current of the component, and therefore an increased stability of the latter. Moreover, there is a reduction in the size of the active layer which is the only region of the structure in which the two types of carriers are simultaneously present: the diffusion of the carriers before recombination then occurs in a plane and the dislocations no longer occur in the carrier capture except by their line fragment intersecting the active layer. However, even with these quantum well structures, the components obtained are not very stable, and have lifetime-related problems.

OBJECT OF THE INVENTION

The main object of this invention is to reduce the influence of dislocations on the operating of structures for optoelectronic components, such as lasers, fabricated from semiconductor materials.

SUMMARY OF THE INVENTION

Accordingly, there is provided a structure having plural layers in semiconductor material wherein one of the layers comprises three-dimensional inclusions in a semiconductor material having a narrower forbidden band (bandgap) than the forbidden band of the material of said layer.

Preferably, the layer comprising the inclusions constitutes the active layer of an optoelectronic component, such as a laser. The inclusions ensure a function of traps for the carriers, thereby avoiding diffusion of the latter towards the core of the dislocations and the associated nonradiative centers. The inclusions are the site of the radiative recombination between electrons and trapped holes leading to the laser gain.

The inclusions are inserted during growth, by using the three-dimensional nucleation mode observed during the epitaxy of III-V materials that are highly mismatched with regard to the substrate used. Accordingly, a method for fabricating a multilayer structure embodying the invention comprises the two following successive steps during the growth of the material constituting one of said layers:

interrupting at least once said growth, and

depositing a thin layer of the semiconductor material having a narrower forbidden band than the forbidden band of the material of said layer thereby constituting three-dimensional inclusions.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the invention will be apparent from the following particular description of several preferred embodiments of this invention as illustrated in the corresponding accompanying drawings in which:

FIG. 1 is a schematic transverse cross-sectional view of a laser structure according to the prior art;

FIG. 2 is a thickness - quantum energy diagram of the structure according to FIG. 1, in correspondence with the line II—II in FIG. 1;

FIG. 3 is a thickness - refractive index diagram of the structure shown in FIG. 1, according to the line II—II;

FIG. 4 is a schematic transverse cross-sectional view of a multilayer structure in semiconductor material embodying the invention, of a similar type to that of FIG. 1;

FIG. 5 is a schematic detailed view of the active layer in the structure shown in FIG. 4;

FIGS. 6 and 7 are thickness - quantum energy diagrams of the structure shown in FIG. 4, in correspondence with lines VI—VI and VII—VII in FIG. 5, respectively; and

FIGS. 8, 9 and 10 are schematic views in perspective of the structure in FIG. 4 for illustrating the state of the active layer in FIG. 5 before and after deposition of inclusions in a plane and after deposition of a sublayer of active layer on the inclusions, respectively.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As appears by comparison of FIGS. 1 to 4, a structure of a semiconductor laser according to the invention is similar to a known solid-state laser structure. The known structure comprises a semiconductor substrate 1 and a stacking of three or four layers in semiconductor material 2, 3, 4 and 5 placed on a major side of the substrate 1.

In the structure illustrated in FIG. 1, four layers 2 to 5 are provided and constitute a double heterostructure. The layers 2 to 4 are in semiconductor material offering narrow forbidden bands (bandgap) BI between valence band BV and conduction band BC, and high refractive indexes; the semiconductor material of the layers 2 and 4 can be GaAs. The two other layers 3 and 5 are in semiconductor material with forbidden band widths L3 and L5 that are larger than the width of the forbidden band L4 of the layer 4, as shown in FIGS. 2 and 3, and low refractive indexes. The narrowness of the forbidden bands of the layers 2 and 4 is defined here in relation to largeness of the forbidden bands of the layers 3 and 5. Under these conditions, the layers 3 and 5 confine, as is known, a laser beam propagating itself in the active layer 4 intermediate between the layers 3 and 5.

According to a preferred embodiment, the stacking of layers 2 to 5 constitutes a double heterostructure GaAs/GaAlAs formed on a substrate in silicon Si.

The layer 2 is of the monolayer or multilayer type and is epitaxially deposited directly on said major side of the substrate 1 and is in GaAs. The layer 2 constitutes a buffer layer as un-dislocated as possible whose sole purpose constituted by the layers 3, 4 and 5. According to certain embodiments, the layer 2 can be omitted.

The active layer 4 is also in GaAs, and is interposed between the thick layers 3 and 5 and is thinner than layers 3 and 5.

The layers 3 and 5 are in ternary alloy GaAlAs with a lower refractive index than that of the active layer 4 interposed between the layers 3 and 5. The layers 3 and 5 are doped with opposite conductivity impurities, respectively of type n and p. The injected electrons and holes are thus confined and recombine in the active layer 4 which ensures the confinement of the optical wave. In the layer 4 which constitutes the active region of the laser, energy is transferred to the electromagnetic wave by the recombination of the carriers.

To be complete, it should be noted that the invention may apply to any type of known structure in semiconductor materials for laser or optoelectronic components such as optical modulators or optical switches. In particular, the confining layers 3 and 5 may each be constituted by several layers of the same material but with different doping concentrations, and the upper layer 5 may be covered with other layers in semiconductor material that is different and/or of different conductivity, or even with an insulating layer such as SiO_2 or Si_3N_4. Two thin metallic layers 6 and 7 forming electrodes are, of course, provided on both sides of the stack of layers.

Turning to FIG. 4, the semiconductor laser structure embodying the invention comprises a substrate 1*a*, and superposed layers 2*a*, 3*a*, 4*a* and 5*a* as well as electrodes 6*a* and 7*a* which are arranged in relation to one another in the same way as the substrate 1, the layers 2 to 5 and the electrodes 6 and 7 in the known structure shown in FIG. 1. All the layers, with the exception of the layer 4*a*, are identical to the corresponding layers in the known structure.

According to the invention, the active layer 4*a* is modified by comparison with the previous layer 4, by punctual inclusions 8 in a semiconductor material, such as indium arsenide InAs having, as shown in FIG. 6, a smaller width of forbidden band L8 than that L4 of the semiconductor material of the active layer 4*a*, such as gallium arsenide GaAs. As shown in detail and schematically in FIG. 5, the inclusions 8 of InAs form islands substantially of a semi-spherical cap shape which are spread over the layer 4*a*, with a substantially uniform density, in several planes parallel to the confinement layers 3*a* and 5*a*. To avoid overloading of FIG. 5, only three planes P1, P2, PN of inclusions 8 have been illustrated in it.

The fabrication of the semiconductor laser embodying the invention is analogous to that of a laser of the same type according to the prior art, with the exception of the formation step of the active layer **4***a*. The entire laser structure is produced by the same growth technique, e.g. molecular beam epitaxy MBE, or by vapor phase epitaxy in another embodiment.

The growth by molecular beam epitaxy of the material GaAs constituting the layer **4***a* begins at the end of the formation of the confinement layer **3***a*. When the thickness of this layer **4***a* reaches each of the planes **P1** to PN, the growth is interrupted at this point of the structure, as shown in FIG. **8** for the plane **P2**. A thin layer of InAs is deposited on the surface of the "sub-layer" thus formed $4a_1$, $4a_2$, . . . of the active layer **4***a*. The material, InAs, has a lattice that is highly mismatched with GaAs, in the region of 7%, which strongly influences the InAs growth mode. The first molecular layer **P1** of InAs, in practice having a thickness of approximately 0.3 nm, elastically accommodates this lattice parameter difference. However, from the second monolayer on, corresponding to the plane **P2**, a transition to a three-dimensional growth mode is observed at the usual growth temperature of 500° to 550° C. Islands **8** of indium arsenide InAs form at the surface. During an observation of these islands with a Scanning Transmission Electron Microscope (STEM), the size of the InAs islands is seen to be fairly homogeneous, and the distribution of the islands is relatively uniform on the surface of the sample, as shown at the level of the second active sub-layer $4a_2$ in FIG. **9**. In practice, each inclusion is inscribed in a small paving with a size of $5\times5\times2$ nm^3 approximately, and the inclusions are spread over one or plural planes, such as the planes **P1**, **P2** and PN illustrated in FIG. **5**. After each deposition of inclusions in a plane, the epitaxial growth of GaAs is again performed so as to form another active sub-layer. The inclusions **8** are thus buried inside the active layer **4***a*. Constrained within the GaAs lattice, the inclusions do not however contain any dislocation.

As shown in FIGS. **6** and **7**, the indium arsenide InAs has a smaller forbidden band energy (bandgap energy) than that of gallium arsenide GaAs. The inclusions **8** are therefore more attractive for the electrons and the holes. A photoluminescence study of InAs structures in GaAs shows that the trapping of carriers by the inclusions is very efficient, which is translated by a very intense luminescence due to the inclusions, and a very small contribution of the GaAs lattice, and that the optical quality of these structures is very good. A transmission study of these structures shows that this luminescence is intrinsic, i.e., linked to the presence of a high density of states in conjunction with the luminescence energy. Finally, the size of the inclusions and consequently the position of the associated luminescence line depend on the quantity of InAs deposited after the transition to a three-dimensional growth mode.

Furthermore, the density of the InAs inclusions **8** in a plane **P1** to PN is very high, approximately 10^{12}/cm^2, and is particularly high compared with the number of dislocations in known GaAs structures on Si, typically in the region of 10^6/cm^2. The inclusions **8** situated near a dislocation therefore only represent a tiny fraction of their population. The injected carriers therefore have a very high probability of being trapped by an inclusion rather than by a dislocation, and by an intact inclusion rather than by an inclusion perturbed by the proximity of a dislocation. Finally, the presence of highly constrained areas in the structure around the InAs inclusions can inhibit the propagation of existing dislocations.

The confinement factor Γ which is defined as the fraction of the optical wave lying in the active layer **4***a*, is low for the structure embodying the invention, though it is close to 1 in the double heterostructure as shown in FIG. **1**. For a plane of inclusions **P1** to PN, the confinement factor is close to that of a structure with an 0.6-nm wide quantum mono-well. On the other hand, the gain per unit of volume of the active medium g_v increases very significantly for such a laser with quantum boxes. To obtain the same amplification of the optical wave in the cavity, the modal gain $\Gamma.g_v$ must be the same for the two structures. It is then necessary to multiply the inclusion planes in the structure in order to increase the factor of optical confinement. This requirement is met e.g. by forming N=10 to 40 planes **P1** to PN of InAs inclusions **8** in a GaAs cavity having a thickness of 200 nm.

Though the above description refers to a GaAs/-GaAlAs heterostructure, it is possible according to the invention to introduce inclusions in the active layer of other known heterostructures. Among the semiconductor alloy heterostructures of III-V compounds, mention can be made of the laser structures (InGa)As/(InAl)As or (InGa)As/InP on highly mismatched Si or GaAs substrate. InAs inclusions can be fabricated here according to the method embodying the invention. A quaternary alloy such as GaInAsP or InGaAlAs can be provided instead of a binary or ternary alloy. The method embodying the invention is also implemented in matched structures when the commercially available substrate used is of insufficient quality, i.e., when it has a high dislocation rate.

The invention also applies to laser structures usually used for optimizing the optical confinement factor and the collection of carriers, such as heterostructures with separate confinement, with confinement separated by index gradient, etc.

It is possible to apply the invention within the framework of other growth techniques for which a transition to a three-dimensional growth mode has been observed. The fabrication of a GaAs laser structure on Si with InAs inclusions is, for instance, also possible in vapor phase epitaxy from organometallic compounds.

Generally speaking, the present invention makes it possible to reduce the degradation of performances of optoelectronic components when this degradation is due to dislocations, whether it is a question of the increase of their number or their propagation, since the influence of dislocations is reduced. This aspect is important for the power application of laser components.

What we claim is:

1. A structure having plural layers in semiconductor material, one of said layers comprising plural substantially parallel sub-layers deposited successively during growth of said one layer, each of said sub-layers having three-dimensional inclusions in a semiconductor material and a narrower forbidden band gap than a forbidden band gap of said one layer.

2. The structure claimed in claim **1**, wherein the size of each of said inclusions is in the neighborhood of 50 nm^3.

3. The structure claimed in claim **1**, wherein said layer comprising said inclusions is an active layer of an optoelectronic component.

4. The structure claimed in claim **1**, wherein said inclusions comprise indium arsenide.

5. The structure claimed in claim **1**, wherein said layer comprising said inclusions comprises one of the following semiconductor materials: InGaAs, GaAs, GaInAsP, InGaAlAs.

* * * * *

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

I (a) PLAINTIFFS (Check box if you are representing yourself ☐)

Koninklijke Philips Electronics N.V.; and
Philips Lumileds Lighting Company LLC

DEFENDANTS

Seoul Semiconductor Company, Ltd.; and
Seoul Semiconductor, Inc.

(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.)

Edward D. Johnson (SBN 189475)
Mayer Brown LLP
Tel: (650) 331-2000

Two Palo Alto Square, Suite 300
3000 El Camino Real
Palo Alto, CA 94306

Attorneys (If Known)

BY FAX

II. BASIS OF JURISDICTION (Place an X in one box only.)

☐ 1 U.S. Government Plaintiff
☑ 3 Federal Question (U.S. Government Not a Party)
☐ 2 U.S. Government Defendant
☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES - For Diversity Cases Only
(Place an X in one box for plaintiff and one for defendant.)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business in this State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business in Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. ORIGIN (Place an X in one box only.)

☑ 1 Original Proceeding
☐ 2 Removed from State Court
☐ 3 Remanded from Appellate Court
☐ 4 Reinstated or Reopened
☐ 5 Transferred from another district (specify):
☐ 6 Multi-District Litigation
☐ 7 Appeal to District Judge from Magistrate Judge

V. REQUESTED IN COMPLAINT: JURY DEMAND: ☑ Yes ☐ No (Check 'Yes' only if demanded in complaint.)

CLASS ACTION under F.R.C.P. 23: ☐ Yes ☑ No

☑ **MONEY DEMANDED IN COMPLAINT: $** Not yet determined

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write a brief statement of cause. Do not cite jurisdictional statutes unless diversity.)

Patent Infringement under 35 U.S.C. §§ 1, et seq.; Declaratory Judgment under 28 U.S.C. §§ 2201, et seq., and 35 U.S.C. §§ 1, et seq.

VII. NATURE OF SUIT (Place an X in one box only.)

OTHER STATUTES
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce/ICC Rates/etc.
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced and Corrupt Organizations
- ☐ 480 Consumer Credit
- ☐ 490 Cable/Sat TV
- ☐ 810 Selective Service
- ☐ 850 Securities/Commodities/ Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 890 Other Statutory Actions
- ☐ 891 Agricultural Act
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of Info. Act
- ☐ 900 Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loan (Excl. Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability
- ☐ 196 Franchise

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

TORTS PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Fed. Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury
- ☐ 362 Personal Injury-Med Malpractice
- ☐ 365 Personal Injury-Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

IMMIGRATION
- ☐ 462 Naturalization Application
- ☐ 463 Habeas Corpus-Alien Detainee
- ☐ 465 Other Immigration Actions

TORTS PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

CIVIL RIGHTS
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/Accommodations
- ☐ 444 Welfare
- ☐ 445 American with Disabilities - Employment
- ☐ 446 American with Disabilities - Other
- ☐ 440 Other Civil Rights

PRISONER PETITIONS
- ☐ 510 Motions to Vacate Sentence Habeas Corpus
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus/ Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

FORFEITURE/ PENALTY
- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 R.R. & Truck
- ☐ 650 Airline Regs
- ☐ 660 Occupational Safety /Health
- ☐ 690 Other

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt. Relations
- ☐ 730 Labor/Mgmt. Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl. Ret. Inc. Security Act

PROPERTY RIGHTS
- ☐ 820 Copyrights
- ☑ 830 Patent
- ☐ 840 Trademark

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS-Third Party 26 USC 7609

FOR OFFICE USE ONLY: Case Number: SACV11-00356 AG (RNBx)

AFTER COMPLETING THE FRONT SIDE OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED BELOW.

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has this action been previously filed in this court and dismissed, remanded or closed? ☑ No ☐ Yes
If yes, list case number(s): ______

VIII(b). RELATED CASES: Have any cases been previously filed in this court that are related to the present case? ☑ No ☐ Yes
If yes, list case number(s): ______

Civil cases are deemed related if a previously filed case and the present case:
(Check all boxes that apply) ☐ A. Arise from the same or closely related transactions, happenings, or events; or
☐ B. Call for determination of the same or substantially related or similar questions of law and fact; or
☐ C. For other reasons would entail substantial duplication of labor if heard by different judges; or
☐ D. Involve the same patent, trademark or copyright, and one of the factors identified above in a, b or c also is present.

IX. VENUE: (When completing the following information, use an additional sheet if necessary.)

(a) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named plaintiff resides.
☐ Check here if the government, its agencies or employees is a named plaintiff. If this box is checked, go to item (b).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
	Koninklijke Philips Electronics N.V. -- The Netherlands Philips Lumileds Lighting Company LLC -- Santa Clara County

(b) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named defendant resides.
☐ Check here if the government, its agencies or employees is a named defendant. If this box is checked, go to item (c).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Seoul Semiconductor, Inc. -- Orange County	Seoul Semiconductor Company, Ltd. -- Republic of Korea

(c) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** claim arose.
Note: In land condemnation cases, use the location of the tract of land involved.

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Orange County -- All claims	

*** Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, or San Luis Obispo Counties**
Note: In land condemnation cases, use the location of the tract of land involved

X. SIGNATURE OF ATTORNEY (OR PRO PER): ______ **Date** 3/4/2011

Notice to Counsel/Parties: The CV-71 (JS-44) Civil Cover Sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law. This form, approved by the Judicial Conference of the United States in September 1974, is required pursuant to Local Rule 3-1 is not filed but is used by the Clerk of the Court for the purpose of statistics, venue and initiating the civil docket sheet. (For more detailed instructions, see separate instructions sheet.)

Key to Statistical codes relating to Social Security Cases:

Nature of Suit Code	Abbreviation	Substantive Statement of Cause of Action
861	HIA	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405(g))
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405(g))
864	SSID	All claims for supplemental security income payments based upon disability filed under Title 16 of the Social Security Act, as amended.
865	RSI	All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended. (42 U.S.C. (g))

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

NOTICE OF ASSIGNMENT TO UNITED STATES MAGISTRATE JUDGE FOR DISCOVERY

This case has been assigned to District Judge Andrew Guilford and the assigned discovery Magistrate Judge is Robert N. Block.

The case number on all documents filed with the Court should read as follows:

SACV11- 356 AG (RNBx)

Pursuant to General Order 05-07 of the United States District Court for the Central District of California, the Magistrate Judge has been designated to hear discovery related motions.

All discovery related motions should be noticed on the calendar of the Magistrate Judge

---

NOTICE TO COUNSEL

A copy of this notice must be served with the summons and complaint on all defendants (if a removal action is filed, a copy of this notice must be served on all plaintiffs).

Subsequent documents must be filed at the following location:

[ ] **Western Division** **312 N. Spring St., Rm. G-8** **Los Angeles, CA 90012**	[X] **Southern Division** **411 West Fourth St., Rm. 1-053** **Santa Ana, CA 92701-4516**	[ ] **Eastern Division** **3470 Twelfth St., Rm. 134** **Riverside, CA 92501**

Failure to file at the proper location will result in your documents being returned to you.

FOR OFFICE USE ONLY

AO 440 (Rev. 12/09) Summons in a Civil Action

UNITED STATES DISTRICT COURT

for the

Central District of California

Koninklijke Philips Electronics N.V.; and Philips Lumileds Lighting Company LLC *Plaintiff* v. Seoul Semiconductor Company, Ltd.; and Seoul Semiconductor, Inc. *Defendant*	)	Civil Action No. **SACV11-00356 AG (RNBx)**

SUMMONS IN A CIVIL ACTION

To: *(Defendant's name and address)*

FOR OFFICE USE ONLY

A lawsuit has been filed against you.

Within 21 days after service of this summons on you (not counting the day you received it) — or 60 days if you are the United States or a United States agency, or an officer or employee of the United States described in Fed. R. Civ. P. 12 (a)(2) or (3) — you must serve on the plaintiff an answer to the attached complaint or a motion under Rule 12 of the Federal Rules of Civil Procedure. The answer or motion must be served on the plaintiff or plaintiff's attorney, whose name and address are:

Mayer Brown LLP
Edward D. Johnson (SBN 189475)
Two Palo Alto Square, Suite 300
3000 El Camino Real
Palo Alto, California 94306
P: 650-331-2000; F: 650-331-2060

If you fail to respond, judgment by default will be entered against you for the relief demanded in the complaint. You also must file your answer or motion with the court.

CLERK OF COURT

Date: MAR -4 2011

ROLLS ROYCE PASCHAL

Signature of Clerk or Deputy Clerk

1144

FOR OFFICE USE ONLY

AO 440 (Rev. 12/09) Summons in a Civil Action (Page 2)

Civil Action No.

PROOF OF SERVICE

(This section should not be filed with the court unless required by Fed. R. Civ. P. 4 (l))

This summons for *(name of individual and title, if any)* ______________________

was received by me on *(date)* ______________ .

❒ I personally served the summons on the individual at *(place)* ______________________

______________________ on *(date)* ______________ ; or

❒ I left the summons at the individual's residence or usual place of abode with *(name)* ______________

______________________ , a person of suitable age and discretion who resides there,

on *(date)* ______________ , and mailed a copy to the individual's last known address; or

❒ I served the summons on *(name of individual)* ______________________ , who is

designated by law to accept service of process on behalf of *(name of organization)* ______________

______________________ on *(date)* ______________ ; or

❒ I returned the summons unexecuted because ______________________ ; or

❒ Other *(specify)*:

FOR OFFICE USE ONLY

My fees are $ __________ for travel and $ __________ for services, for a total of $ 0.00 .

I declare under penalty of perjury that this information is true.

Date: ______________

____
Server's signature

____
Printed name and title

____
Server's address

Additional information regarding attempted service, etc:

Additional Documents Served:
Complaint for Patent Infringement and Declaratory Judgment of Patent Non-Infringement and Invalidity
Civil Cover Sheet
Certification and Notice of Interested Parties (Local Rule 7.1-1)
Report on the Filing or Determination of an Action Regarding a Patent or Trademark

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