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Attorneys for Plaintiff
HUGA OPTOTECH INC.

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

HUGA OPTOTECH INC.,

Plaintiff,

v.

BLUESTONE INNOVATIONS L.L.C.; BLUESTONE INNOVATIONS HOLDINGS L.P.; BLUESTONE INNOVATIONS FLORIDA, L.L.C.; and BLUESTONE INNOVATIONS TEXAS, L.L.C.,

Defendants.

Case No. CV 11 1576

COMPLAINT FOR DECLARATORY JUDGMENT

DEMAND FOR JURY TRIAL

Plaintiff Huga Optotech Inc. ("Huga") by way of its Complaint alleges the following against Defendants Bluestone Innovations L.L.C.; Bluestone Innovations Holdings L.P.; Bluestone Innovations Florida, L.L.C.; and Bluestone Innovations Texas, L.L.C. (collectively "Bluestone"):

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PARTIES

1. Huga is a foreign corporation organized and existing under the laws of Taiwan with a principal place of business located at No. 40, Industrial 34th Road, Taichung Industrial Park, Taichung, Taiwan, Republic of China.

2. On information and belief, Bluestone Innovations L.L.C. is a corporation organized and existing under the laws of the State of Virginia, having an established place of business at 123 Moncure Drive, Alexandria, Virginia 22314.

3. On information and belief, Bluestone Innovations Holdings L.P is a corporation organized and existing under the laws of the State of Virginia, having an established place of business at 123 Moncure Drive, Alexandria, Virginia 22314.

4. On information and belief, Bluestone Innovations Florida, L.L.C., is a corporation organized and existing under the laws of the State of Florida, having an established place of business at 1970 E. Osceola Parkway, Suite 10, Kissimmee, Florida 34743-8630.

5. On information and belief, Bluestone Innovations Texas, L.L.C., is a corporation organized and existing under the laws of the State of Texas, having an established place of business at 350 N. Saint Paul St., Suite 2900, Dallas, Texas 75201-4234.

JURISDICTION AND VENUE

6. This action arises under the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the Patent Laws of the United States, 35 U.S.C. §1 *et seq.*

7. This Court has subject matter jurisdiction in this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) in that it is a civil action arising out of the patent laws of the United States of America. This Court also has subject matter jurisdiction pursuant to 28 U.S.C. §§ 2201 and 2002 because, as shown below, a substantial controversy exists between Huga and Bluestone regarding non-infringement, invalidity, and unenforceability.

8. This Court has personal jurisdiction over Bluestone because it has engaged in numerous contacts and business dealings within the State of California, including in relation to their acquisition of rights to the patents-in-suit.

9. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400,

because a substantial part of the events giving rise to Huga's claims occurred in this district.

INTRADISTRICT ASSIGNMENT

10. Pursuant to Civil Local Rule 3-2(c), because this action is an intellectual property action, it is properly assigned to any of the divisions in this district.

GENERAL ALLEGATIONS

11. On information and belief, Bluestone owns by assignment U.S. Patent No. 5,977,612 ("the '612 patent") entitled "Semiconductor Devices Constructed from Crystallites," which was filed on December 20, 1996, and issued on November 12, 1999. The '612 patent lists as inventors David P. Bour, Fernando A. Ponce, G.A. Neville Connell, Ross D. Bringans, Noble M. Johnson, Werner K. Goetz, and Linda T. Romano, who, on information and belief, were all residents of the State of California at the time of the filing of the '612 patent. A true and correct copy of the '612 patent is attached hereto as Exhibit A.

12. On information and belief, Bluestone owns by assignment U.S. Patent No. 6,605,832 ("the '832 patent") entitled "Semiconductor Structures Having Reduced Contact Resistance," which was filed on July 31, 2001, and issued on August 12, 2003. The '832 patent lists as the inventor Christian G. Van De Wall, who, on information and belief, was a resident of the State of California at the time of the filing of the '832 patent. A true and correct copy of the '832 patent is attached hereto as Exhibit B.

13. On information and belief, Bluestone purchased its rights under the '612 and '832 patents from Xerox PARC, which has its principal place of business located at the Palo Alto Research Center, 333 Coyote Hill Road, Palo Alto, CA.

14. On May 26, 2010, Bluestone filed a complaint in the United States District Court for the Eastern District of Texas against Huga, among others, for patent infringement of a patent related to light emitting diodes ("LEDs"), which is the same subject matter of the patents-in-suit.

15. On February 10, 2011, during discussions regarding settlement of the litigation in the Eastern District of Texas, a Bluestone representative told Huga representatives and Huga's counsel that unless Huga settled the litigation in the Eastern District of Texas, Bluestone would sue Huga in Florida for infringement of the '612 and '832 patents. As such, Bluestone has demonstrated its

intent to assert the '612 and '832 patents against Huga and there is, as a consequence, a reasonable apprehension of imminent legal action by Bluestone against Huga.

16. To avoid legal uncertainty and to protect its substantial investment in its LED products, Huga has brought these claims for declaratory judgment against Bluestone. An actual justiciable controversy exists between the parties as to the infringement and validity of the '612 and '832 patents.

17. A judicial determination of the respective rights of the parties with respect to the infringement and validity of the claims of the ''612 and '832 patents is necessary and appropriate pursuant to 28 U.S.C. § 2201.

FIRST CAUSE OF ACTION

Declaratory Judgment of Non-Infringement and Invalidity of U.S. Patent No. 5,977,612

18. Huga realleges and incorporates by reference the allegations of paragraphs 1-17.

19. Huga does not directly or indirectly infringe any valid claim of the '612 patent.

20. The '612 patent is invalid for failure to meet one or more of the requirements of patentability under 35 U.S.C. § 101, *et seq.*, including but not limited to 35 U.S.C. §§102, 103, and 112.

SECOND CAUSE OF ACTION

Declaratory Judgment of Non-Infringement and Invalidity of U.S. Patent No. 6,605,832

21. Huga realleges and incorporates by reference the allegations of paragraphs 1-17.

22. Huga does not directly or indirectly infringe any valid claim of the '832 patent.

23. The '832 patent is invalid for failure to meet one or more of the requirements of patentability under 35 U.S.C. § 101, *et seq.*, including but not limited to 35 U.S.C. §§102, 103, and 112.

PRAYER FOR RELIEF

WHEREFORE, Huga respectfully requests that this Court enter a Judgment and Order in its favor against Bluestone:

1. Declaring that Huga has not infringed any valid claim of the '612 and '832 patents;

2. Declaring that all the claims of the '612 and '832 patents are invalid;

3. Declaring that this case is an exceptional case under 35 U.S.C. § 285 and awarding Huga its attorney's fees, costs, and expenses; and

4. Awarding Huga any further additional relief as the Court may deem just, proper and equitable.

DEMAND FOR JURY TRIAL

Huga hereby demands a trial by jury on all issues triable to a jury.

DATED: March 31, 2011

Respectfully submitted,

KILPATRICK TOWNSEND & STOCKTON LLP

By: _____
DAVID B. PERRY

Attorneys for Plaintiff
HUGA OPTOTECH INC.

63237471 v1

Exhibit A

US005977612A

United States Patent [19]

Bour et al.

[11] **Patent Number: 5,977,612**

[45] **Date of Patent: Nov. 2, 1999**

[54] **SEMICONDUCTOR DEVICES CONSTRUCTED FROM CRYSTALLITES**

[75] Inventors: **David P. Bour**, Cupertino; **Fernando A. Ponce**, Sunnyvale; **G. A. Neville Connell**; **Ross D. Bringans**, both of Cupertino; **Noble M. Johnson**, Menlo Park; **Werner K. Goetz**, Palo Alto; **Linda T. Romano**, Sunnyvale, all of Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **08/770,403**

[22] Filed: **Dec. 20, 1996**

[51] **Int. Cl.**[6] **H01L 29/06**

[52] **U.S. Cl.** **257/618**; 257/466; 257/103; 257/440

[58] **Field of Search** 257/466, 618, 257/94, 97, 103, 440, 499

[56] **References Cited**

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F. A. Ponce, D. P. Bour, and W. Götz, Palo Alto Research Center; P.J. Wright, Oxford Instruments, "Spatial distribution of the luminescence in GaN thin films," App. Phys. Lett. 68 (1), Jan. 1, 1996, pp. 57–59.

Shuji Nakamura, Masayuki Senoh, Shin–ichi Nagahama, Naruhito Iwasa, Takao Yamada, Toshio Matsushita, Hiroyuki Kiyoku and Yasunobu Sugimoto, "InGaN–Based Muli–Quantum–Well–Structure Laser Diodes," Jpn. J. Appl. Phys. vol. 35 (1996) pp. L74–L76.

Isamu Akasaki, Hiroshi Amano, Shigetoshi Sota, Hiromitsu Sakai, Toshiyuki Tanaka and Masayoshi Koike, "Stimulated Emission by Current Injection from an AlGaN/GaN/GaInN Quantum Well Device," Jpn. J. Appl. Phys. vol. 34 (1995) pp. L1517–L1519.

Shuji Nakamura, Masayuki Senoh, Shin–ichi Nagahama, Naruhito Iwasa, Takao Yamada, Toshio Matsushita, Hiroyuki Kiyoku, and Yasunobu Sugimoto, "Characteristics of InGaN multi–quantum–well–structure laser diodes," Appl. Phys. Lett. 68 (23, Jun. 3, 1996, pp. 3269–3271.

Shuji Nakamura, Masayuki Senoh, Shin–ichi Nagahama, Naruhito Iwasa, Takao Yamada, Toshio Matsushita, Hiroyuki Kiyoku and Yasunobu Sugimoto, "InGaN multi–quantum–well structure laser diodes grown on $MgAl_2O_4$ substrates," Appl. Phys. Lett. 68 (15), Apr. 8, 1996, pp. 2105–2107.

Shuji Nakamura, Masayuki Senoh, Shin–ichi Nagahama, Naruhito Iwasa, Takao Yamada, Toshio Matsushita, Hiroyuki Kiyoku and Yasunobu Sugimoto, "InGaN Multi–Quantum–Well–Structure Laser Diodes with Cleaved Mirror Cavity Facets," Jpn. J. Appl. Phys. vol. 35 (1995), pp. L217–L219.

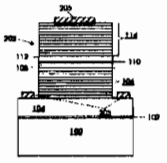
Shota Kitamura, Kazumasa Hiramatsu and Nobuhiko Sawaki, "Fabrication of GaN Hexagonal Pyramids on Dot–Patterned GaN/Sapphire Substrates via Selective Metalorganic Vapor Phase Epitaxy," Jpn. J.A. Appl. Phys. vol. 34 (1995) pp. L–1184—L1186.

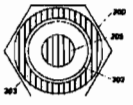
Primary Examiner—Nathan K. Kelley

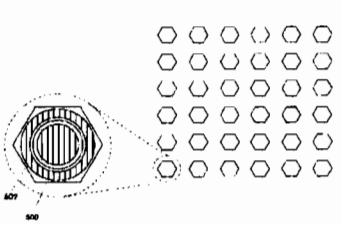
[57] **ABSTRACT**

The present invention relates to electronic devices formed in crystallites of III-V nitride materials. Specifically, the present invention simplifies the processing technology required for the fabrication of high-performance electronic devices in III-V nitride materials.

5 Claims, 14 Drawing Sheets







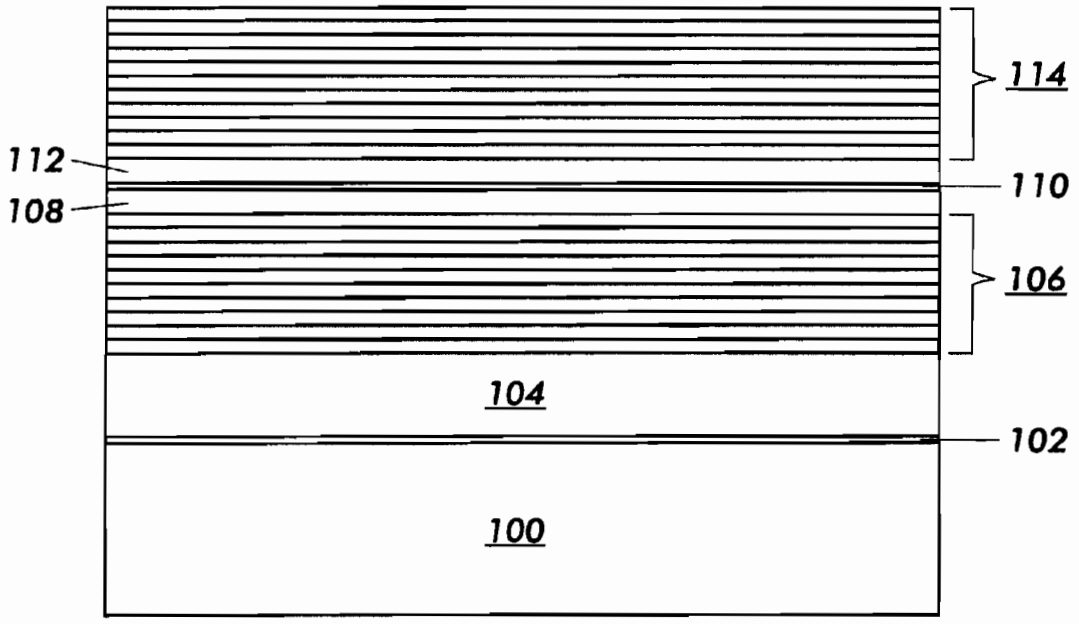


FIG. 1

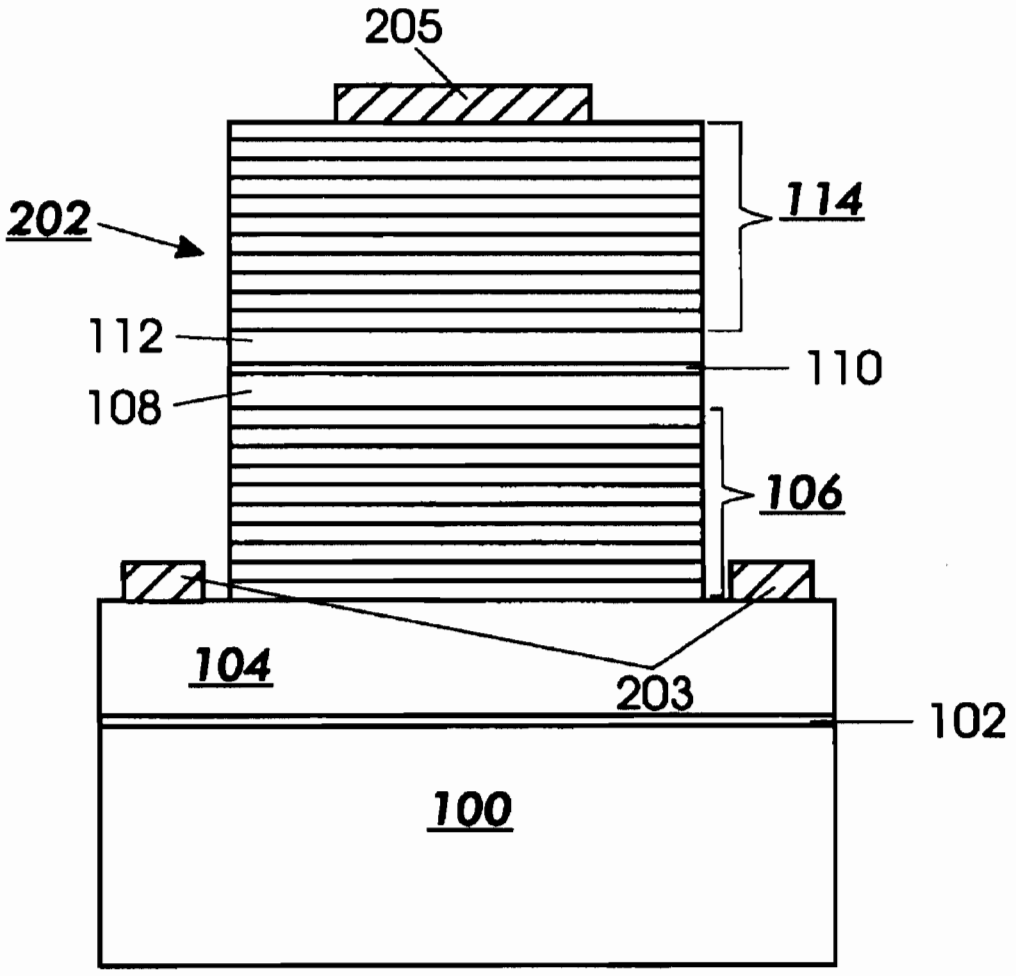


FIG. 2a

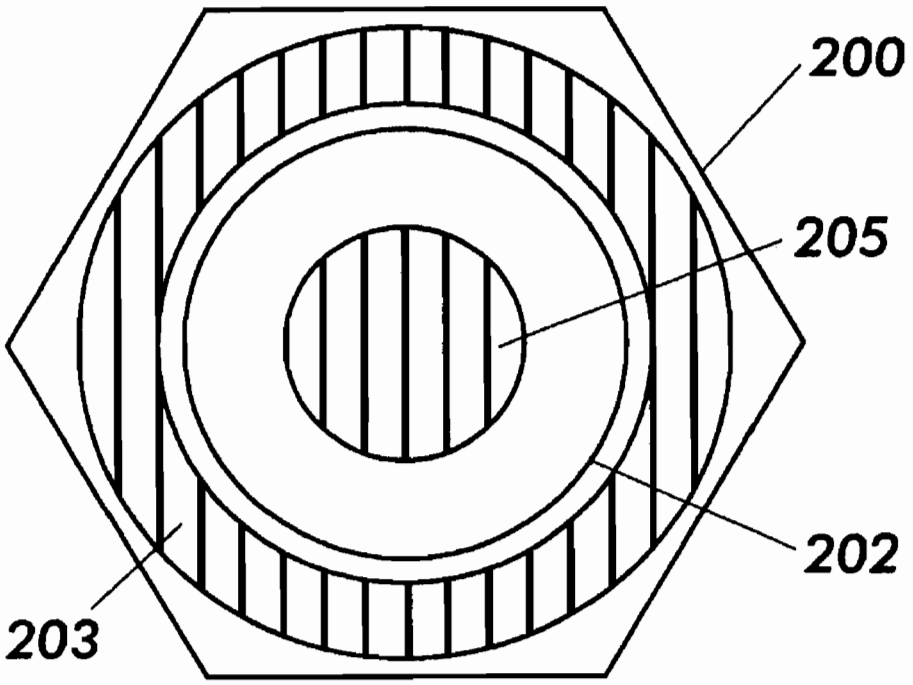


FIG. 2b

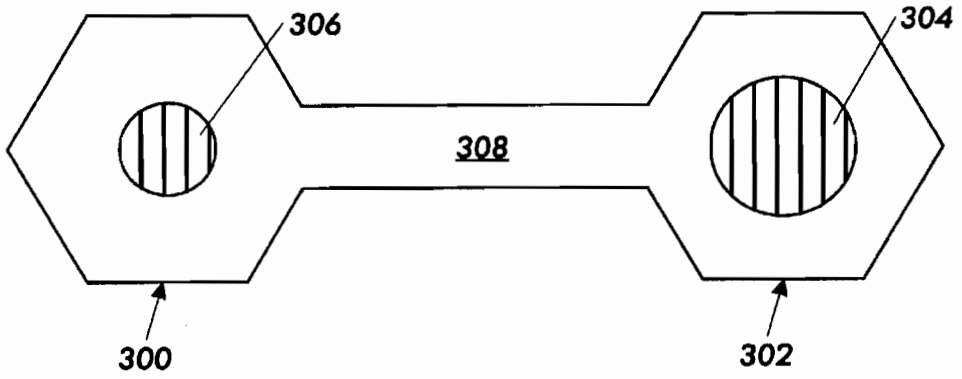


FIG. 3a

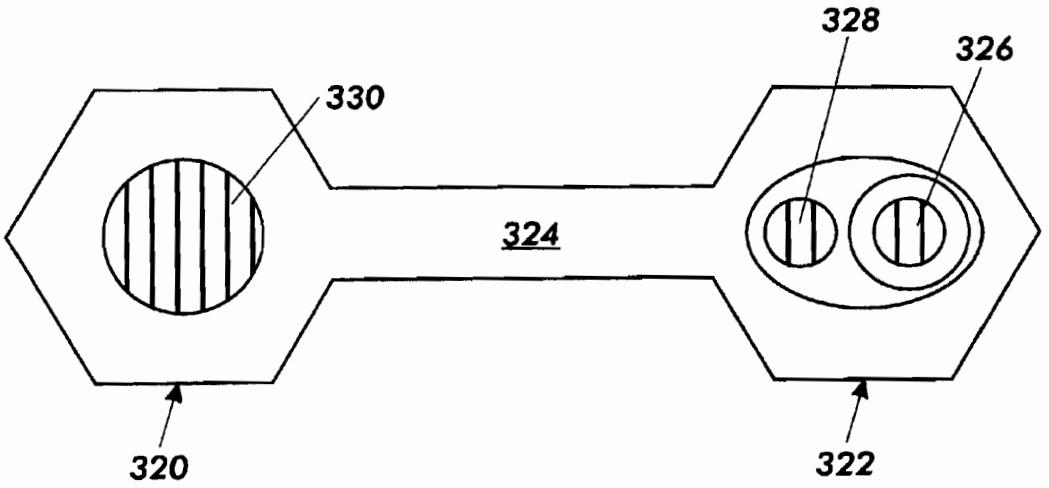


FIG. 3b

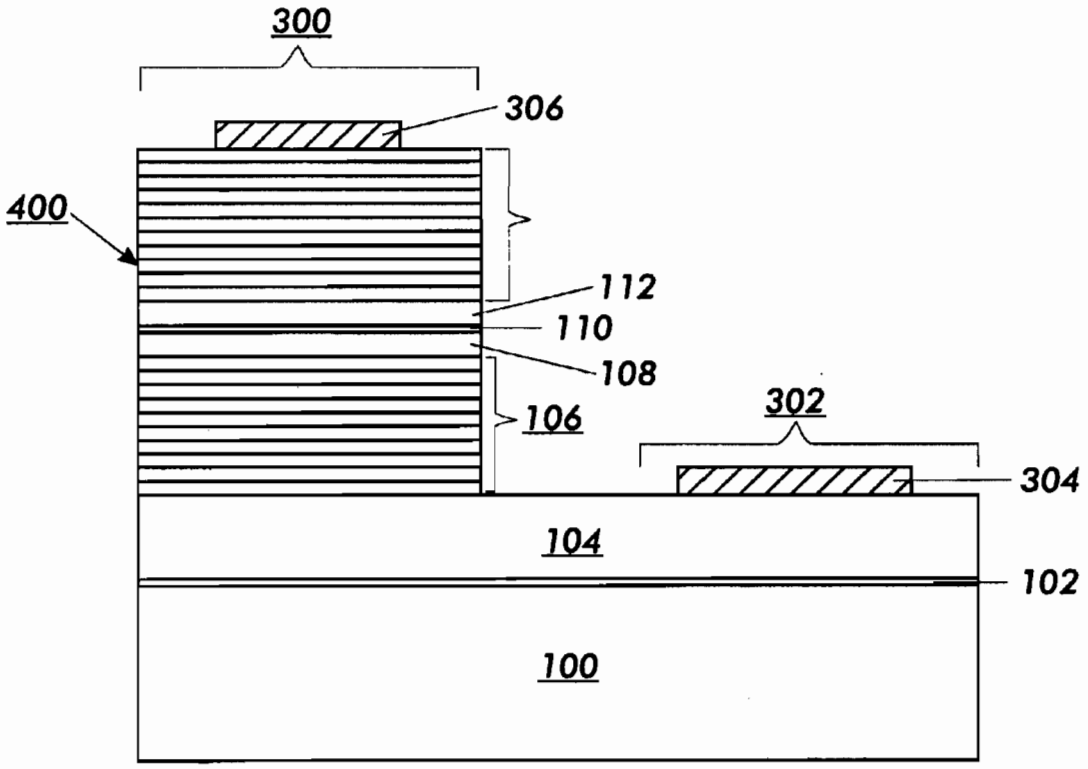


FIG. 4

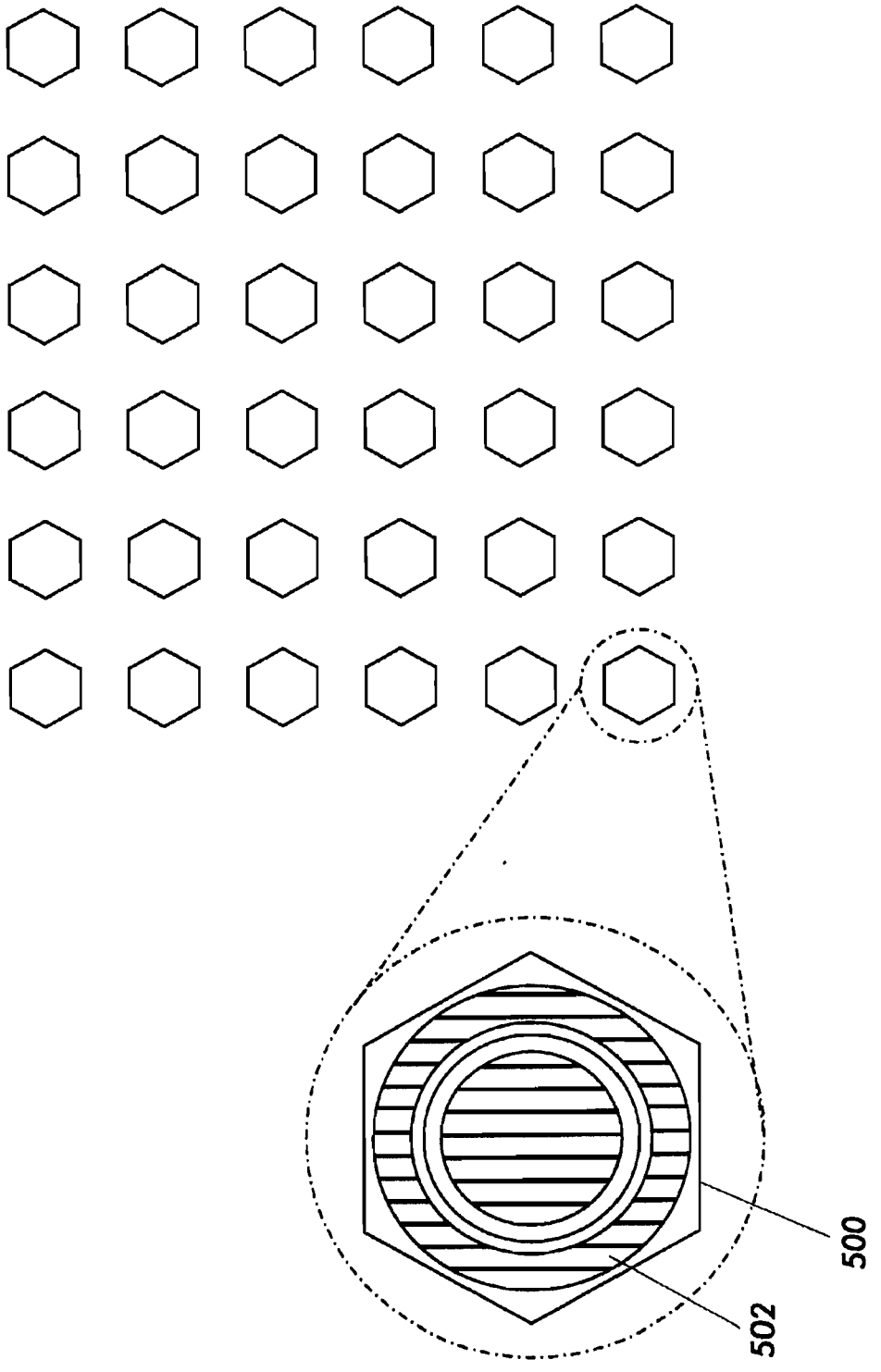


FIG. 5a

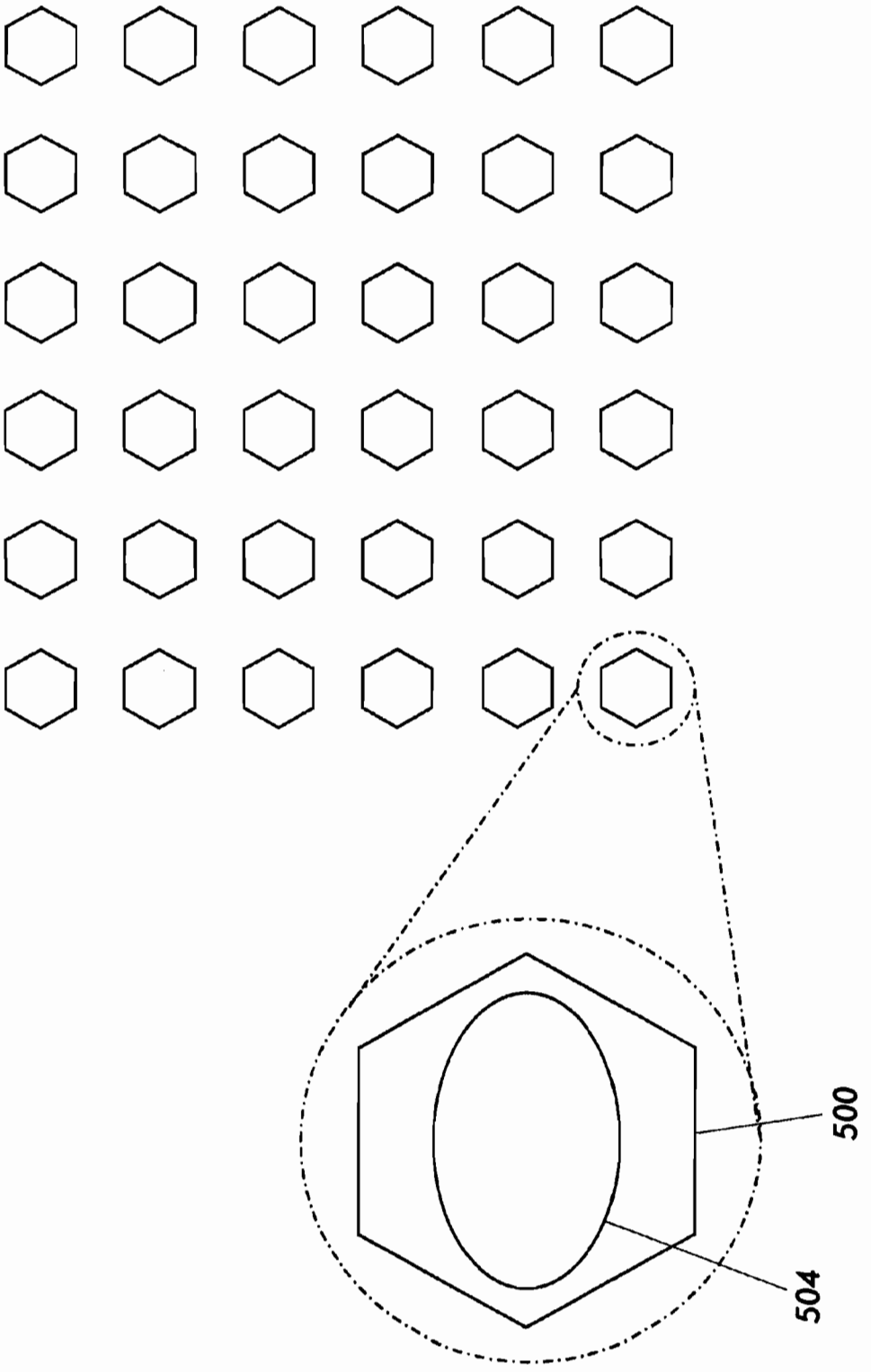


FIG. 5b

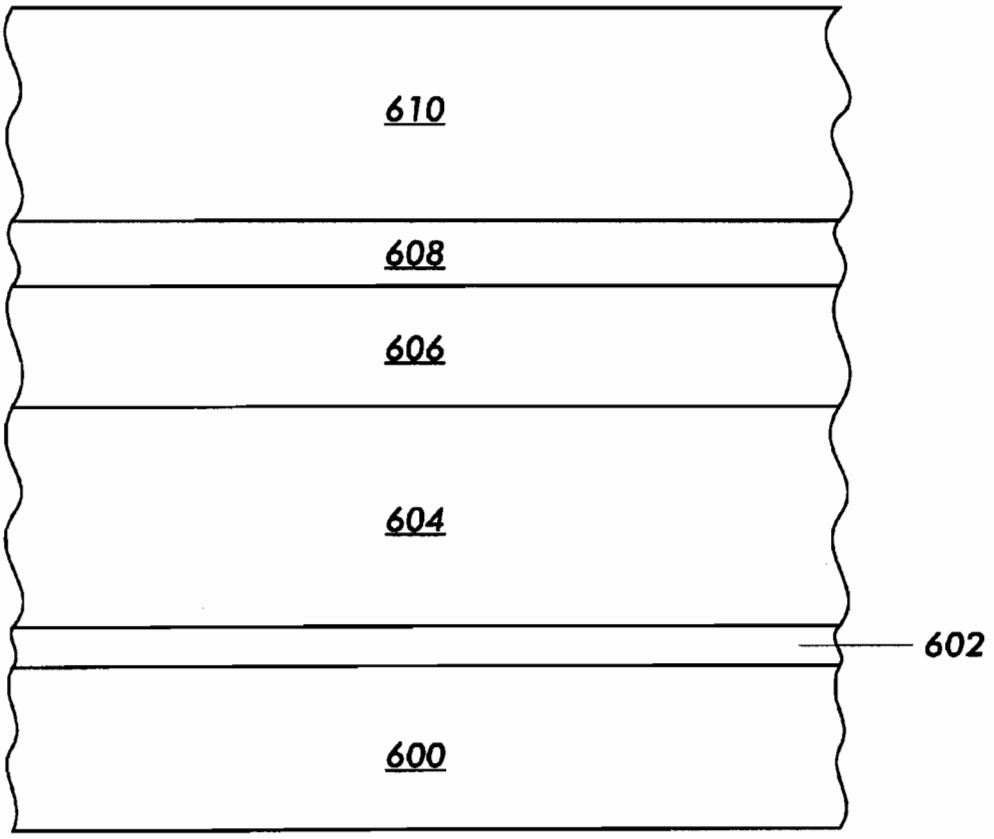


FIG. 6

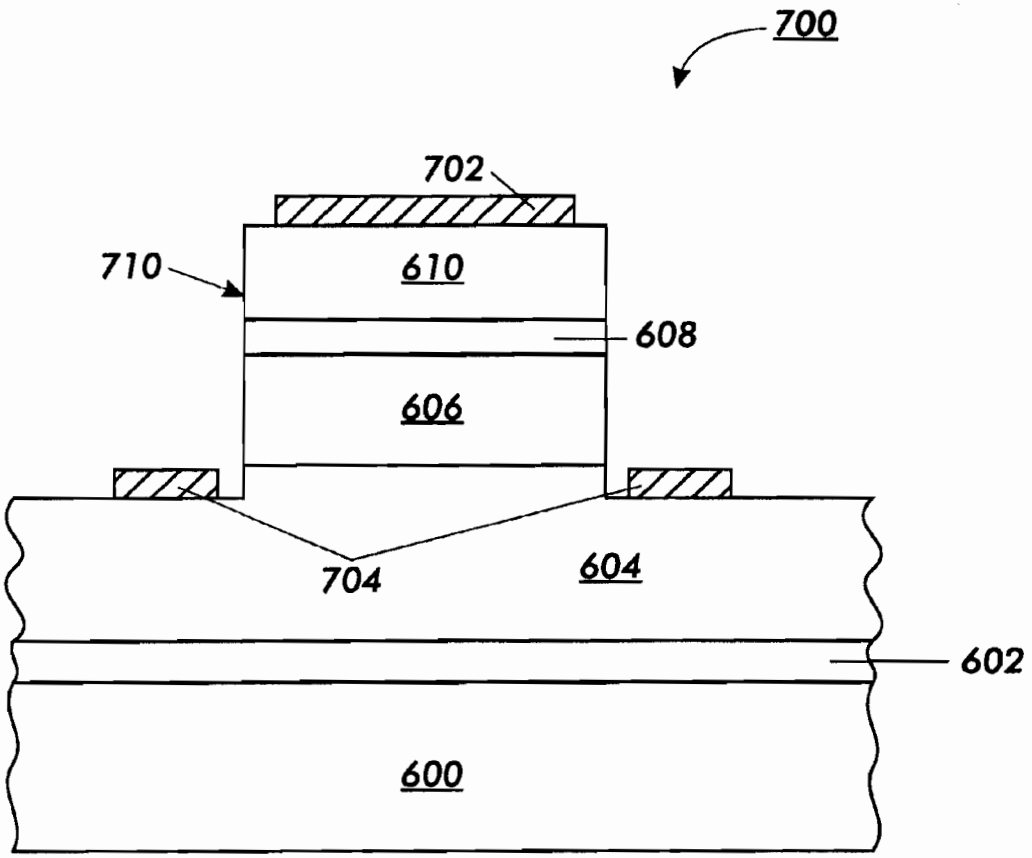


FIG. 7a

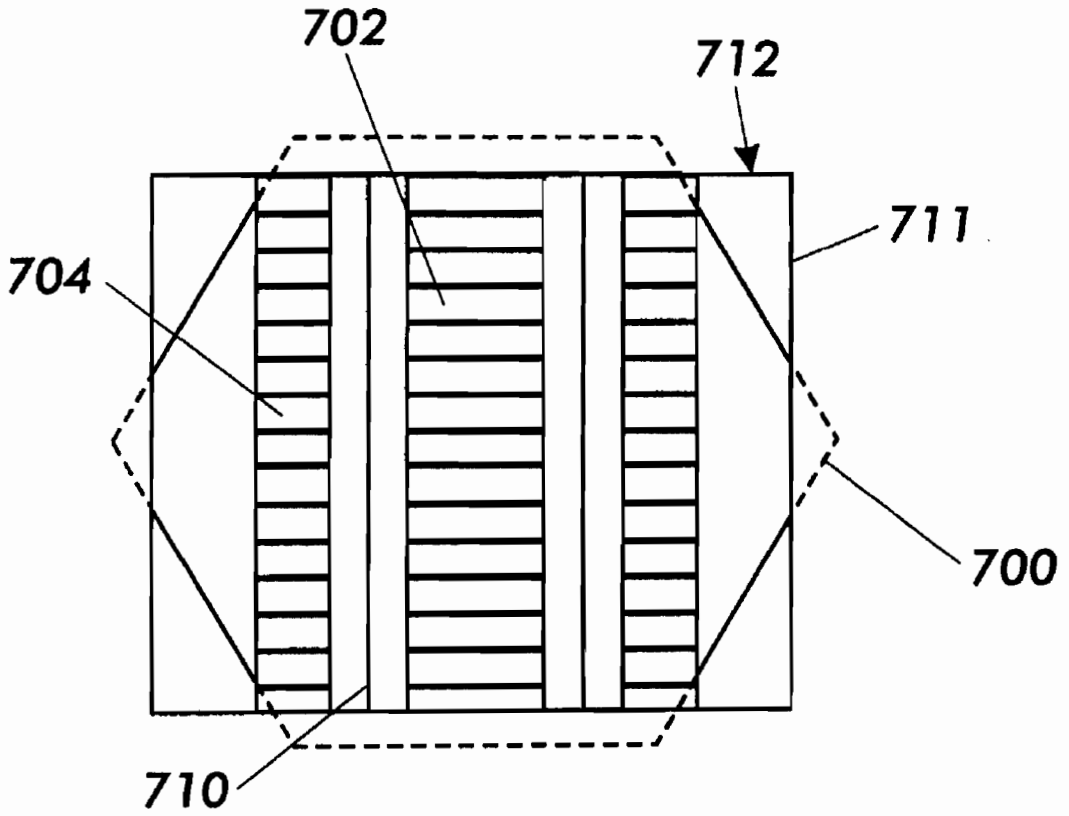


FIG. 7b

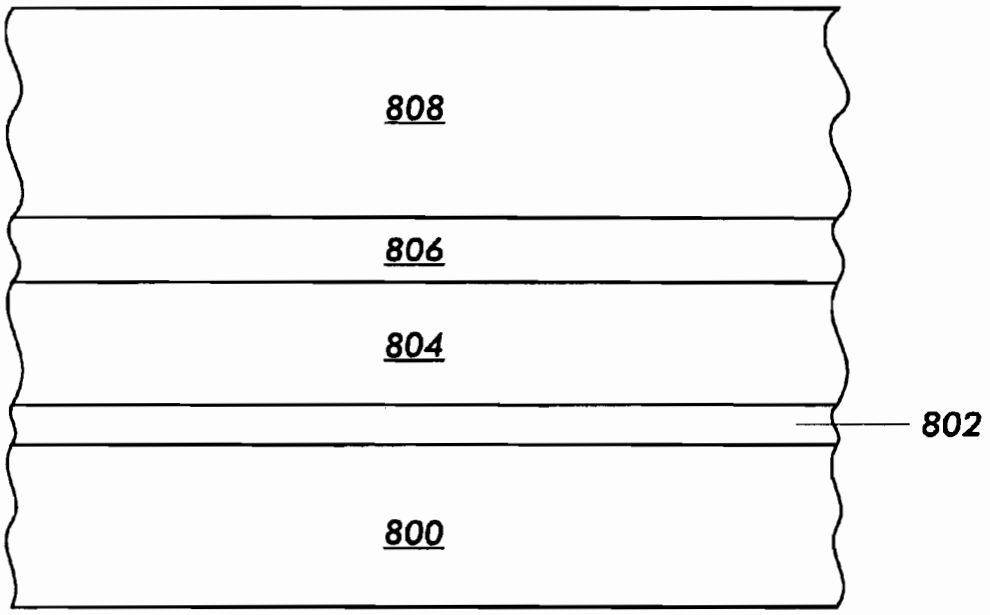


FIG. 8

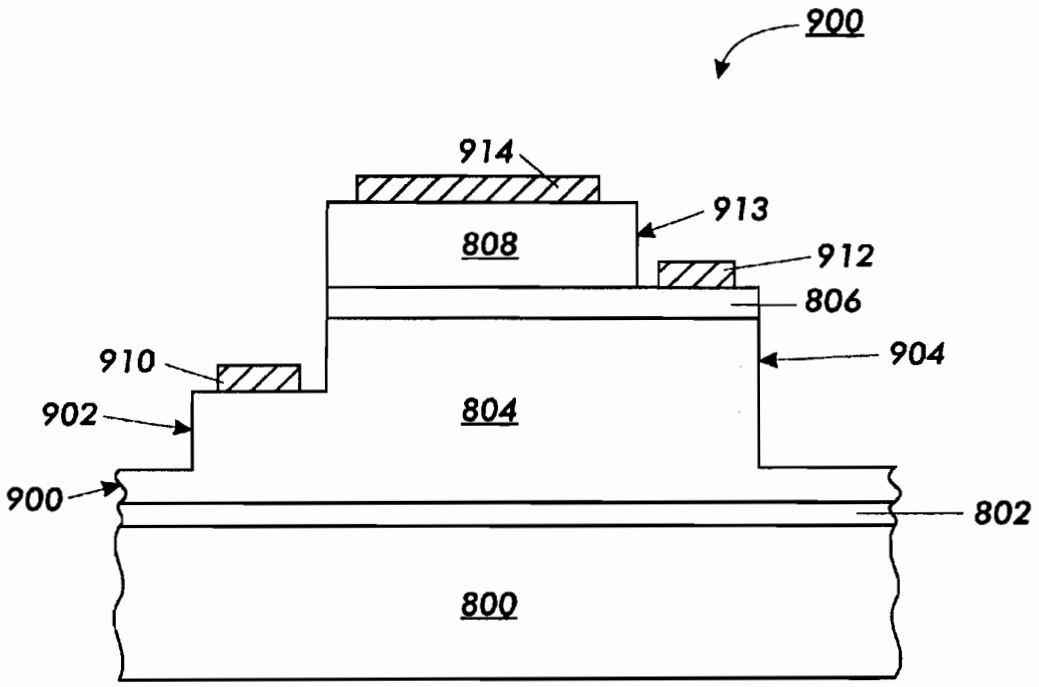


FIG. 9a

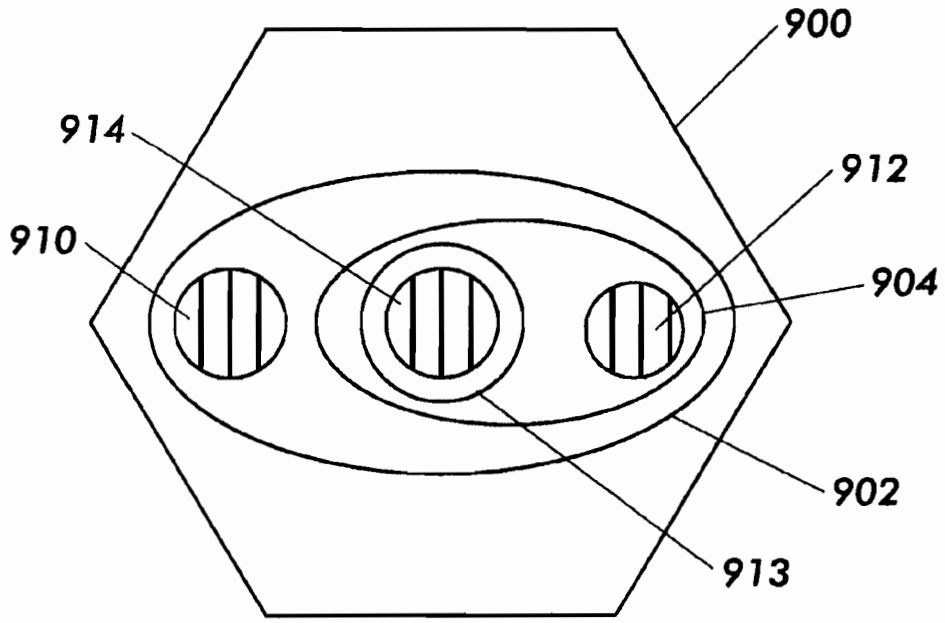


FIG. 9b

SEMICONDUCTOR DEVICES CONSTRUCTED FROM CRYSTALLITES

FIELD OF INVENTION

The present invention relates generally to solid state laser devices which emit short-wavelength radiation. More specifically, the invention relates to laser structures constructed from hexagonal crystallites.

BACKGROUND OF INVENTION

Solid state lasers made from Group III-V nitrides such as InAlGaN, have great potential in applications in many areas such as high-resolution full-color printing, high-density optical storage, advanced display systems, and optical communications. Since materials in the Group III-V nitride system have bandgaps that vary from 1.9 eV to 6.2 eV, a laser or light emitting diode ("LED") made from a Group III-V nitride may emit light at a wavelength ranging from 380 to 600 nanometers (nm). A laser made from GaN can emit light in the ultra-violet region of the spectrum whereas a laser made from InN can emit light in the red region. Therefore, the Group III-V nitride material system can produce lasers at wavelengths covering a wide range of the electromagnetic spectrum.

The lasers formed by materials in the Group III-V nitride system which produce emissions at short wavelength such as green or blue have particularly significant implications in high-resolution printing and high-density optical storage. For instance, substantial effort has been expended in developing a blue laser for high-resolution printing because of a blue laser's small fundamental spot size and superior depth of focus. The small spot size allows for higher "dpi" (dots per inch) printing, and therefore improved resolution. The superior depth of focus enables a blue laser to be easily focused, allowing for the use of relatively low cost optics even in a high resolution printing system.

Short-wavelength lasers also allow for high density optical storage of audio information, video information, and data. Conventional compact disc ("CD") players and CD-ROM drives use a infrared laser beam. Currently, a standard 12.7 cm CD can hold up to 650 megabytes of data. Blue lasers, at half the wavelength of red lasers, have much smaller spot sizes and can read and write in finer detail on optical discs, thereby substantially increasing their data capacity. They will allow audio CD's and CD-ROMS to store up to at least five times the information they currently hold.

As stated previously, in addition to producing short-wavelength lasers, the Group III-V nitride material system can produce lasers which emit light at a wavelength ranging from 380 to 600 nanometers (nm). The ability to produce lasers with large wavelength separation with a single material system is important in full-color xerographic printing. Generally, in xerographic printing, a full-color print is formed by superimposing an electrostatic image in black with an electrostatic image in each of the three primary colors (cyan, magenta, and yellow). In one architecture, to achieve high-speed single-pass printing, four laser beams are typically required, one for each color and black. The laser beams simultaneously strike a single raster output polygon mirror and a single set of scan optics. The beams are then separated by optical filters, and each beam is directed to a photoreceptor for printing a color. A similar application is to use red, green, and blue lasers to make full-color film printing for computer generated movies.

In order for the optical filters to effectively isolate each beam at a reasonable cost, the laser beams must typically

have a separation of at least 50 nanometers in their wavelengths. To make such a four-laser array on the same substrate, the use of two semiconductor material systems is generally required. For instance, the $Al_xGa_{1-x}As$ material system can produce lasers with wavelengths from approximately 750 nanometers to 850 nanometers whereas the AlGaInP material system can produce lasers from approximately 630 to 700 nanometers. In contrast, a laser array formed using materials in the Group III-V nitride system can achieve large wavelength separations without using a second material system.

Red, green, and blue lasers can also be used to produce brighter and more efficient projection displays. They can also be used for backlighting in direct view displays such as screens for laptop computers. Furthermore, due to the physical and electronic properties of materials in the Group III-V nitride system, devices formed using such materials can withstand higher temperatures, higher power densities, and harsher environmental conditions. Hence, the need for lasers formed using Group III-V nitrides crosses a wide spectrum of applications.

Unfortunately the development of lasers formed by Group III-V nitride materials has been hampered by numerous problems in the processing technology of such materials. For instance, the difficulties in forming high-quality single-crystalline Group III-V nitride materials over large areas are well known. Group III-V materials tend to form dislocations and cracks easily. They are also difficult to remove by etching. Due to the difficulty in etching III-V nitride materials, techniques to selectively deposit nitride materials over a smaller area have been developed. An example of such a selective deposition technique is described in "Fabrication of GaN Hexagonal Pyramids on Dot-Patterned GaN/Sapphire Substrate via Selective Metalorganic Vapor Phase Epitaxy" by Kitamura et al., Jpn. J. App. Phys. vol. 34(1995) pp. L1184–1186 (1995). However, such techniques often result in the formation of hexagonal pyramids, commonly known as "hillocks," which are a manifestation of the natural lattice structure of III-V nitride materials. These hillocks are often viewed as defects unsuitable for use in any application because of their topology and crystalline structures. However, high-quality crystallites with a topology suitable for device fabrication have been described in recent publications such as in "Spatial Distribution of the Luminescence in GaN Thin Films," by Ponce et al., Appl. Phys. Lett. 68(1), pp. 57–59 (1996).

BRIEF SUMMARY OF INVENTION

The present invention takes advantage of crystallites which are associated with natural lattice structures of III-V nitrides to form semiconductor devices. Each III-V nitride material has a natural lattice structure, and these crystallites are manifestations of natural lattice structures of the III-V nitride materials. The use of these crystallites alleviates the need to form single-crystalline nitride material over large areas since their sizes typically range from tens of microns to millimeters. These crystallites also have large flat surfaces, making device formation in them possible. Additionally, these crystallites have superior structural, optical, and electronic properties, allowing for the formation of high-performance semiconductor devices. For instance, it would allow for the manufacture of laser devices with high-efficiency and low threshold current. The present invention also simplifies the processing required to form an electronic device comprising of a patterned element such as a bipolar transistor or a field effect transistors in the III-V nitride material system. It also allows for the integration of electronic devices with optoelectronic devices.

One advantage of the present invention is that it greatly simplifies the processing required in the fabrication of short-wavelength lasers in the blue and green portion of the spectrum, which have wide applications in high-resolution printing and high-density optical storage systems. The present invention alleviates the need to grow high-quality planar epitaxial films over a large area.

A further advantage of the present invention is that it makes possible the formation of an array of electronic or optoelectronic devices on a single substrate. For instance, under the present invention, a substrate may be patterned so that a two-dimensional array of laser devices may be formed. Such two-dimensional arrays would allow for multiple-beam printing and help enable the manufacture of super high-speed printing devices.

The advantages and objects of the present invention will become apparent to those skilled in the art from the following detailed description of the invention, its preferred embodiments, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a cross-sectional view of a hexagonal crystallite structure with a plurality of semiconductor layers on a sapphire substrate. The hexagonal crystallite structure shown may be used to implement the preferred embodiment of the present invention.

FIG. **2**(*a*) illustrates a cross-sectional view of a vertical cavity surface emitting laser structure formed in a hexagonal crystallite structure with a plurality of semiconductor layers.

FIG. **2**(*b*) illustrates a top view of a vertical cavity surface emitting laser structure formed in a hexagonal crystallite structure with a plurality of semiconductor layers.

FIG. **3**(*a*) illustrates a top view of two adjacent hexagonal crystallites which are used to form a laser structure. The crystallites are connected by a bridge structure.

FIG. **3**(*b*) illustrates a top view of two adjacent hexagonal crystallites which are used to form a transistor. The crystallites are connected by a bridge structure.

FIG. **4** illustrates a cross-sectional view of a vertical cavity surface emitting laser structure formed in two separate hexagonal crystallites connected by a bridge.

FIG. **5**(*a*) illustrates a top view of a two-dimensional array of hexagonal crystallites formed in accordance to a pattern in the substrate. As illustrated, a laser device may be formed in each crystallite.

FIG. **5**(*b*) illustrates a top view of a two-dimensional array of hexagonal crystallites formed in accordance to a pattern in the substrate. As illustrated, a transistor may be formed in each crystallite.

FIG. **6** illustrates a cross-sectional view of a hexagonal crystallite structure with a plurality of semiconductor layers on a sapphire substrate. This hexagonal crystallite structure may be used for forming an edge emitting laser.

FIG. **7**(*a*) illustrates a cross-sectional view of an edge emitting laser formed in a hexagonal crystallite structure.

FIG. **7**(*b*) illustrates a top view of an edge emitting laser formed in a hexagonal crystallite structure.

FIG. **8** illustrates a cross-sectional view of a hexagonal crystallite structure with a plurality of semiconductor layers on a sapphire substrate. The hexagonal crystallite structure shown may be used for forming a heterojunction bipolar transistor.

FIG. **9**(*a*) illustrates a cross-sectional view of a heterojunction bipolar transistor formed in a hexagonal crystallite structure.

FIG. **9**(*b*) illustrates a top view of a heterojunction bipolar transistor formed in a hexagonal crystallite structure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **1** illustrates the layers of a hexagonal crystallite structure which is used to implement the preferred embodiment of the present invention. Under this embodiment, this structure is used to form a vertical cavity surface emitting laser ("VCSEL") in a single hexagonal crystallite. The laser structure uses a "C"-plane sapphire (Al_2O_3) substrate **100** with good surface quality. Other substrates known to those of ordinary skill in the art, such as "A"-plane sapphire, silicon carbide or spinel substrate ($MgAl_2O_4$) may also be used. Prior to any epitaxial process, the sample undergoes a nitridation process, during which it is exposed to ammonia gas at above 1000° C. momentarily. The duration of the exposure may not be critical in most circumstances. The duration of the exposure to ammonia gas may range from seconds to minutes. Typically, the sample is exposed to ammonia for about five to ten minutes. This nitridation process replaces the oxygen atoms on the surface of the substrate with nitrogen atoms, converting the aluminum oxide on the surface to aluminum nitride. Instead of ammonia, other nitrogen precursors which are sufficiently pyrolyzed above 500° C. such as hydrazine, phenylhydrazine, or other organic nitrogen molecules may also be used.

After the nitridation process, nitride layers are deposited on the sapphire substrate **100** by an epitaxial process known as metal-organic chemical vapor deposition ("MOCVD") at approximately 500 to 1100° C. Hydride vapor phase epitaxy ("VPE"), liquid phase epitaxy ("LPE"), molecular beam epitaxy ("MBE"), and other known crystal growth processes may also be used. As shown in FIG. **1**, a thin amorphous GaN layer **102** is first deposited on the substrate **100**. Other nitride materials such as AlN may also be used. This GaN layer **102** is typically deposited at a low temperature such as 550° C. to ensure that the resulting film will be amorphous. This amorphous film **102** should provide a good continuous coverage of the substrate, on which other epitaxial layers are formed. After the deposition process, the amorphous layer **102** is then heated up so that it undergoes a solid phase epitaxy process during which the film becomes crystalline. The thickness of the amorphous layer **102** must ordinarily be such that it will crystallize in a manner which is well-aligned to the atoms of the substrate material **100**. If the GaN layer **102** is too thin, the material may not completely cover the substrate **100**. If the GaN layer **102** is too thick, the film may crystallize through two different processes—"homogeneous crystallization" and "solid phase epitaxy." Homogeneous crystallization is the process by which the amorphous GaN film **102** crystallizes in accordance with the natural lattice structure of GaN. In contrast, solid phase epitaxy is the process by which the GaN film **102** crystallizes in accordance to the underlying substrate **100**. As a result, the crystallization process would produce randomly aligned crystallites embedded in the layer. Typically, the thickness of the GaN layer **102** ranges from 10 to 40 nanometers (nm).

Additionally, this amorphous GaN layer **102** serves to release the stress between the interface of the layers above the substrate **100** and the substrate **100**. This amorphous GaN layer **102** helps to accomodate the lattice mismatch that exists between the substrate and the epitaxial films. It also acts as a nucleation layer for the subsequently deposited epitaxial layers.

Above the amorphous GaN layer **102**, a thicker GaN layer **104** of three to five microns (μm) is deposited. This layer is

generally deposited at 1000–1100° C., producing a crystalline film. Under this embodiment, instead of a planar epitaxial film, the deposited layer tends to crystallize into hexagonal structures with flat top surfaces over the substrate. These crystallites on the substrate may be associated with the lattice structure of one of the deposited layers. The size of these hexagonal crystallites varies from microns to millimeters. Generally, thicker epitaxial layers tend to produce larger hexagonal crystallites and films of higher structural quality. A discussion of the quality of such films may be found in "Spatial Distribution of the Luminescence in GaN Thin Films," by Ponce et al., Appl. Phys. Lett. 68(1), pp. 57–59 (1996). However, as this GaN layer **104** becomes thicker, the throughput of the process may be of concern.

The doping of the GaN buffer layer **104** is generally silicon at a level of approximately $5\times10^{18}cm^{-3}$. Other n-type dopants such as selenium (Se), tellurium (Te), tin (Sn) or sulphur (S) may also be used. Under this embodiment, an even higher doping level in the GaN layer **104** is desired because the n-type contact to the laser structure would be formed on this layer. Higher doping generally produces lower contact resistance. However, it is well known that GaN films, which are highly-doped by silicon, are susceptible to "alloy hardening" effects which typically cause cracks in the epitaxial film. Dislocations and cracks in the GaN buffer layer **104** is a particularly serious problem in light of the relatively large lattice mismatch between an Al_2O_3 substrate and a GaN film.

Above the GaN buffer layer **104** is a superlattice structure for forming a lower distributed Bragg reflector ("DBR") **106** which provides the necessary internal reflection and outcoupling of light in a VCSEL structure. The lower DBR **106** is typically formed by multiple pairs of an AlGaN layer and a GaN layer, both of which are n-type. The number of pairs required depends upon the desired reflectivity. Typically, 20 to 50 pairs are used. To achieve high internal reflection, the reflectivity should be as close to 100% as possible. High reflectivity generally reduces the threshold current of a laser. However, if the DBR structure is also used to outcouple light, its reflectivity must be slightly below 100 percent. In this case, the reflectivity of the lower DBR **106** is typically 98% to 99% because it is used to outcouple the light.

The reflectivity of the lower DBR **106** is a function of the difference in the refractive index between the AlGaN layer and the GaN layer of the superlattice. The greater the difference in their refractive indices, the fewer number of pairs are required. Under this embodiment, the refractive index of the AlGaN layer in the DBR superlattice **106** is approximately 2.2 to 2.3, which corresponds to an aluminum content of approximately 20% to 40%. Presently, the correlation between aluminum mole fractions and the corresponding refractive indices is not yet well established. Factors other than reflectivity such as strain, current injection requirements, and the offset between the conduction band and the valence band also influence the aluminum content to be used in the AlGaN layers of the superlattice **106**. Generally, more strain in the film is created when higher aluminum content is used in the AlGaN layers of the DBR superlattice **106**. Interface problems as well as difficulties in doping tend to occur as higher aluminum content in the AlGaN layers of the superlattice **106** is used.

The thickness of the individual AlGaN or GaN layers of the DBR superlattice **106** depends upon the desired output wavelength of the laser as well as the refractive index of the material forming the active region of the laser structure. Typically, the thickness is one quarter of the output wavelength divided by the refractive index of the material. For instance, if the laser is designed to produce emission at 420 nm, the thickness of each layer should be 105 nanometers divided by the refractive index of the material which is about 2.5 for GaN, amounting to approximately 40 nanometers.

Immediately above the lower DBR structure is an InGaN or GaN layer **108**. The lower InGaN or GaN layer **108**, the active layer **110**, and the top InGaN or GaN layer **112** comprise the optical cavity or the so-called "spacer" between the two DBR's **106** and **114**. The total thickness of these three layers, **108**, **110**, and **112**, is an integer multiple of the desired output wavelength. This integer multiple is typically in the range of one to ten. For instance, assuming that the integer multiple is one, the weighted average refractive index is 2.5, and the desired output wavelength is 420 nm, the total thickness of all three layers, **108**, **110**, and **112**, should then be 168 nanometers. Above this InGaN layer **108** is the active layer **110** of the laser structure which is formed by a single InGaN quantum well or a multiple quantum well structure ("MQW"). A typical thickness of a quantum well structure is one to five nanometers. To achieve an output wavelength of 420 nanometers, the indium mole fraction is typically 15% to 20%. Nothing in this invention prevents the use of a thicker GaN or InGaN layer as the active layer **110**. The thickness of such a GaN or InGaN layer would be approximately one to ten nanometers.

Above the active layer **110** is an upper InGaN or GaN layer **112** whose thickness is essentially the same as the lower InGaN layer **108**. These two InGaN layers, **108** and **112**, along with the active layer **110** form the optical cavity in which the desired optical gain can be attained. Above the upper InGaN layer **112** is an upper DBR structure **114**, which is structurally similar to the lower DBR structure **106**. Since the lower DBR **106** is n-type, this upper DBR **108** is p-type. Instead of a p-type DBR, a material such as titanium dioxide (TiO_2)or aluminum dioxide (Al_2O_3), which is transparent to light at 420 nanometers, may also be used. The use of such an insulating DBR material would necessitate an alternative approach in forming the p-type contacts. A metal may also be used to reflect the light so long as the metal does not absorb light at the wavelength produced by the laser.

FIGS. **2** (*a*) and (*b*) illustrate a cross-sectional view and a top view of the preferred embodiment respectively. FIG. **2**(*a*) shows a cross-sectional view of a VCSEL formed in a hexagonal crystallite structure **200** with a plurality of semiconductor layers as shown in FIG. **1**. FIG. **2**(*b*) shows a top view of a VCSEL formed in a hexagonal crystallite. After the epitaxial layers **104** though **114** shown in FIG. **1** have been formed, the sample undergoes an etching step to produce the cylindrical mesa structure **202** shown in FIG. **2**. The depth of the mesa structure should be such that an n-type contact **203** to the VCSEL can be formed on the n-type GaN layer **104** as shown in FIG. **2**(*b*). The n-type contact **203** is in a donut shape as shown in FIG. **2**(*b*). After the n-type contact **203** has been formed, the sample is masked so that a circular p-contact **205** can be formed above the upper DBR structure **114**. As shown in FIG. **2**(*b*), the entire laser structure is formed in a single hexagonal crystallite **200**, portions of which have been removed by etching during the formation of the VCSEL.

The semiconductor structure shown in FIG. **1** may also be used to implement a second embodiment of the present invention. Under this alternative embodiment, two adjacent hexagonal crystallites, **300** and **302**, are used to form a single laser structure as shown in FIG. **3**(*a*). FIG. **3** shows a top view of two hexagonal crystallites **300** and **302** which are connected by a bridge **308**. To form such as structure, a silicon dioxide layer is first deposited on the substrate

material. Then, a pair of pin-holes a fixed distance apart is formed in the silicon dioxide layer using a mask. As previously stated, prior to the epitaxial process, the substrate first undergoes a nitridation process. The pin-holes in the substrate, along with the nitridation process, help the nucleation of hexagonal crystallite structures at the locations of the pin-holes.

Under this embodiment, one of the hexagonal crystallite **300** is for forming a VCSEL structure and its p-type contact **306**. The other hexagonal crystallite structure **302** is for forming the n-type contact **304** of the VCSEL. Such an approach is particularly useful if there is difficulty in achieving large crystallite structure. The bridge **308** is formed by removing the epitaxial materials surrounding the hexagonal crystallite structures **300** and **302** as well as the bridge region **308**. Likewise, a bipolar transistor can be formed in two adjacent hexagonal crystallites, **320** and **322**, as shown in FIG. **3**(*b*). The two crystallites **320** and **322** are connected by a bridge structure **324**. Under this approach, the emitter contact **326** and the base contact **328** are formed in one of the crystallites **322**. The collector contact **330** is formed in another crystallite **320**.

FIG. **4** shows a cross-sectional view of a VCSEL formed in two hexagonal crystallite structures. As shown in FIG. **4**, the epitaxial layers are etched so that a p-type contact **306** can be formed. The depth of the mesa structure **400** should be such that an n-type contact **304** can be formed on the n-type GaN layer **104**. Above the mesa structure **400**, a p-type contact **306** is formed.

The embodiment shown in FIG. **2**(*b*) is easily extendible to the formation of a two-dimensional array of hexagonal crystallites as shown in FIG. **5**(*a*) through the formation of an array of pin-holes in the substrate. The pin-holes are generally formed by a silicon dioxide mask defined by photolithography. FIG. **5**(*a*) shows a 6×6 crystallite array which can be used to form a two-dimensional array of devices. For instance, as shown in FIG. **5**(*a*), a laser structure **502** may be formed in each of the hexagonal crystallites **500**. Likewise, as shown in FIG. **5**(*b*), other semiconductor device comprises a patterned element such as a transistor structure may be formed in each of the hexagonal crystallites **500**. FIG. **5**(*b*) is intended to show a generic transistor, without any of its structural element, formed in a crystallite.

FIG. **6** illustrates a semiconductor structure which may be used to implement another embodiment of the present invention. It illustrates the layers of a hexagonal crystallite which may be used to form an edge emitting laser structure. As shown in FIG. **6**, the substrate is a "C"-plane sapphire (Al_2O_3) substrate **600** with good surface quality. As previously discussed, prior to any epitaxial process, the sample first undergoes a nitridation process, during which it is exposed to ammonia gas at above 1000° C. momentarily. After the nitridation process, nitride layers for forming an edge emitting laser structure are deposited by an epitaxial process known as metal-organic chemical vapor deposition (MOCVD) at approximately 700 to 1100° C. A thin amorphous GaN layer **602** is first deposited on the substrate **600** at a low temperature such as **550°** C. Other nitride materials such as AlN may also be used. A typical thickness of the amorphous GaN layer **602** is approximately 10 to 40 nanometers (nm).

Again, after the deposition process, the amorphous GaN layer **602** is then heated up so that it undergoes a solid phase epitaxy process during which the film becomes crystalline. Then, a thick GaN buffer layer **604** of three to five microns (μm) is deposited. This layer **604** is generally deposited at 1000–1100° C., producing a film which crystallizes into localized hexagonal structures with flat top surfaces. The quality and size of the hexagonal crystallite depends upon the thickness of the layer **604** and other subsequently deposited films. The doping of the GaN buffer layer **604** is silicon at a level of approximately $5\times10^{18}cm^{-3}$. Under this embodiment, an even higher doping level is desired in the GaN buffer layer **604** is desired because the n-type contact to the laser structure would be formed on this layer. However, as stated previously, higher doping generally produces "alloy hardening" effects which may cause cracks in the epitaxial film.

Above the GaN buffer layer **604** is an n-type AlGaN cladding layer **606**. The thickness of the layer is typically several hundred nanometers. The aluminum mole fraction ranges from 5 to 15 percent. A aluminum mole fraction of less than 5 percent may also be used. Above the lower AlGaN cladding layer **606** is the active layer **608** formed by a single InGaN quantum well or a multiple quantum well structure. The indium mole is approximately 15 to 40 percent, which should produce emissions at a wavelength of 380 to 450 nanometers. Above the active layer **608** is an upper AlGaN cladding layer **610**. This layer is p-type with an aluminum mole fraction which ranges from 5 to 15 percent.

After the formation of the layers shown in FIG. **6**, a ridge mesa **710** is formed by an etching process as shown in FIG. **7**(*a*). The depth of the mesa structure **710** should reach the n-type GaN layer **604** so that the n-type contact **704** to the laser structure may be formed. The n-type contact may be formed by using a titanium/gold alloy. FIG. **7**(*a*) shows a cross-sectional view of an edge emitting laser under the present invention. FIG. **7**(*b*) shows a top view of an edge emitting laser under the present invention. After the ridge mesa **710** is etched, a rectangular n-type contact **704** is formed on the GaN layer **604**. Similarly, a p-type contact **702** is formed on the p-type AlGaN layer **610**. The p-contact **702** is typically formed with a metal such as a nickel/gold alloy. The rectangle in FIG. **7**(*b*) shows the laser chip. The dotted line in FIG. **7**(*b*) shows the hexagonal crystallite structure **700**. Before forming the facets **712**, the laser structure is etched or mechanically cut to form the edges **711**. Then, the laser structure is cleaved or etched along crystalline planes to form side facets **712**. In order to form side facets **712** for this laser structure, the size of the hexagonal crystallite **700** should be relatively large so that the side facets **712** may be formed by a cleaving or etching process.

FIG. **8** illustrates a semiconductor structure which may be used to implement another embodiment of the present invention. It illustrates layers of a hexagonal crystallite for forming a heterojunction bipolar transistor. The substrate used is again a "C"-plane sapphire (Al_2O_3) substrate **800**. After a nitridation process as described previously, epitaxial layers are then deposited by a process known as MOCVD at approximately 500 to 1100° C. As shown in FIG. **8**, a thin amorphous GaN layer **802** of approximately 10 to 40 nanometers is first deposited on the substrate **800** at a low temperature such as 550° C. Other nitride materials such as AlN may also be used. Then, the amorphous layer **802** is subsequently heated up so that it undergoes a solid phase epitaxy process during which the film becomes crystalline. Above the amorphous GaN layer **802**, a thicker GaN collector layer **804** of three to five microns (μm) is then deposited. This GaN collector layer **804** is generally deposited at 1000–1100° C., producing a film which crystallizes into hexagonal crystallite structures with flat top surfaces.

The quality and size of the hexagonal crystallites depends upon the thickness of the GaN collector layer **804** as well as the thickness of other subsequently deposited films. Generally, thicker epitaxial layers produce a film of higher quality.

The doping of the GaN collector layer **804** is generally silicon at a level of approximately $5\times10^{18}cm^{-3}$. Its thickness is typically three to five microns. Above the GaN collector layer **804** is a p-type GaN base layer **806** for forming the base of a heterojunction bipolar transistor. The doping and thickness of the p-type GaN layer is typically 50 to 500 nanometers and 1 to 2×10^{18} cm^{-3}. The base layer **806** should generally be as thin as possible to reduce the base transit time of the bipolar transistor. Above the p-type GaN base layer **806** is an n-type AlGaN emitter layer **808** for forming the emitter of the bipolar transistor. The aluminum mole fraction of the n-type emitter layer **808** typically ranges from 0 to 20 percent. Its doping and thickness are typically 0.5 to 5×10^{18} cm^{-3} and 0.1 to 2 microns respectively.

FIG. **9**(*a*) shows a cross-sectional view of a heterojunction bipolar transistor under the present invention. FIG. **9**(*b*) shows a top-view of a heterojunction bipolar transistor under the present invention. After the formation of the layers shown in FIG. **8**, a cylindrical mesa structure **902** shown in FIG. **9**(*b*) is formed by etching. The depth of this mesa structure **902** should reach the GaN collector layer **804** so that the n-type collector contact **910** may be formed on it. Then, a second cylindrical mesa structure **904** is formed so that a p-type base contact **912** may be formed on the GaN base layer **912** as shown in FIG. **9**(*a*). Then, a third cylindrical mesa structure **913** is formed so that an n-type emitter contact **914** can be formed on the AlGaN emitter layer **808**. The entire heterojunction bipolar structure is formed in a single hexagonal crystallite **900** as shown in FIG. **9**(*b*).

The composition, dopants, doping levels, and dimensions given above are exemplary only, and variations in these parameters are permissible. Additionally, other layers in addition to the ones shown in the figures may also be included. Variations in experimental conditions are also permitted. Lastly, instead of GaN and GaAlN, other semiconductor materials or other III-V alloys may also be used.

While the invention has been described in conjunction with specific embodiments, it is evident to those skilled in the art that many alternatives, modifications, and variations will be apparent in light of the foregoing description. Any other semiconductor device comprises a patterned element may also be formed in a crystallite. Accordingly, the invention is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the appended claims.

What is claimed is:

1. A structure in which may be formed a semiconductor device, the structure comprising:

an aluminum-containing substrate having a nitrided region formed therein with a generally planar upper surface upon which material layers may be formed, said nitrided region having a single crystal structure;

a gallium nitride nucleation region in physical contact with said upper surface; and

a localized crystallite structure formed over and in physical contact with said nucleation region such that said localized crystallite structure forms epitaxially with said upper surface of said region, said localized crystallite structure having a substantially planar upper surface generally parallel to said generally planar upper surface of said nitrided region.

2. The structure of claim **1**, wherein said nitrided region is a region of single-crystal aluminum nitride formed in said aluminum-containing substrate.

3. The structure of claim **2**, wherein said aluminum containing substrate is Al_2O_3.

4. A structure in which may be formed a semiconductor device, the structure comprising:

a substrate formed of Al_2O_3 and having a region formed therein with a generally planar upper surface upon which material layers may be formed, said region being comprised of aluminum nitride and having a single crystal structure; and

a localized crystallite structure formed over and in physical contact with said upper surface of said region such that said localized crystallite structure forms epitaxially with said upper surface of said region, said localized crystallite structure having a substantially planar upper surface generally parallel to said planar upper surface of said region.

5. A structure in which may be formed a semiconductor device, the structure comprising:

a substrate formed of Al_2O_3 and having a region formed therein with a generally planar upper surface upon which material layers may be formed, said region comprising aluminum nitride and having a single crystal structure;

a gallium nitride nucleation region in physical contact with said upper surface; and

a localized crystallite structure formed over and in physical contact with said nucleation region such that said localized crystallite structure forms epitaxially with said upper surface of said region, said localized crystallite structure having a substantially planar upper surface generally parallel to said generally planar upper surface of said region.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,977,612
APPLICATION NO. : 08/770403
DATED : November 2, 1999
INVENTOR(S) : David P. Bour et al.

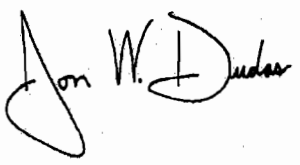
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 3, insert as a new paragraph:

This invention was made with Government support under Agreement No. 70NANB2H1241 awarded by the Department of Commerce and under Agreement No. MDA972-95-3-0008 awarded by ARPA. The Government has certain rights in this invention.

Signed and Sealed this

First Day of August, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

Exhibit B

US006605832B2

(12) **United States Patent**
Van De Walle

(10) **Patent No.: US 6,605,832 B2**
(45) **Date of Patent: Aug. 12, 2003**

(54) **SEMICONDUCTOR STRUCTURES HAVING REDUCED CONTACT RESISTANCE**

(75) Inventor: **Christian G. Van De Walle**, Sunnyvale, CA (US)

(73) Assignee: **Xerox Corporation**, Stamford, CT (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/682,174**

(22) Filed: **Jul. 31, 2001**

(65) **Prior Publication Data**

US 2003/0025113 A1 Feb. 6, 2003

(51) **Int. Cl.**[7] **H01L 21/8249**
(52) **U.S. Cl.** **257/200**; 257/184; 257/189
(58) **Field of Search** 257/184, 189, 257/200; 438/22, 46, 47

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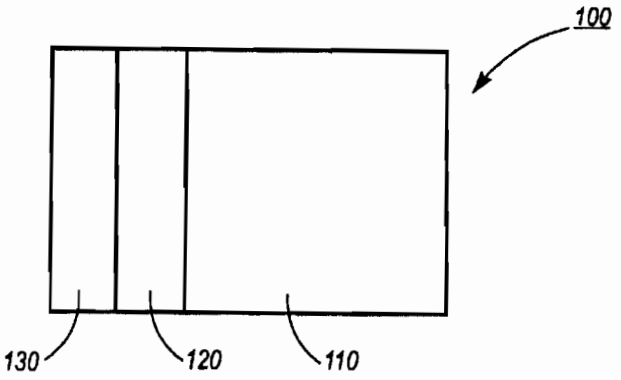
* cited by examiner

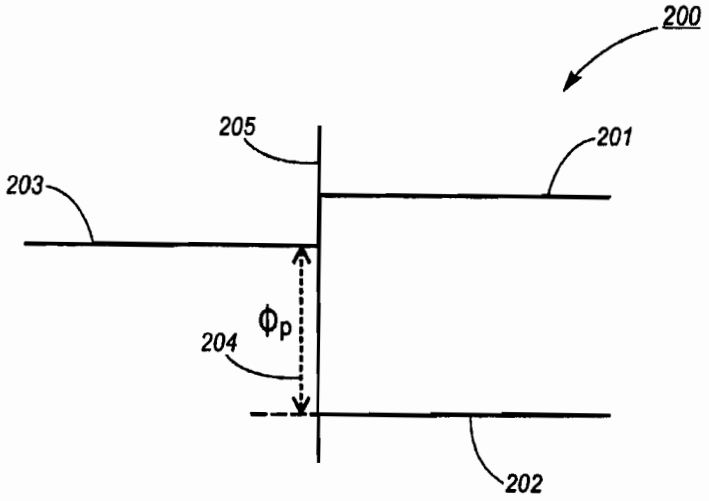
Primary Examiner—Long Pham
(74) *Attorney, Agent, or Firm*—Oliff & Berridge, PLC.

(57) **ABSTRACT**

The performance of nitride based diodes is currently limited by the resistivity of the ohmic contacts to the p-type GaN. The large value of the contact resistance contributes to a large voltage for device operation. This in turn causes device heating, making cw operation difficult and limiting the device lifetime. A layer of GaP or GaNP alloy between the GaN and the metal contact layer serves to bridge the energetic barrier between the GaN valence band and the metal Fermi level, thus enhancing the hole injection and reducing the contact resistance.

20 Claims, 4 Drawing Sheets





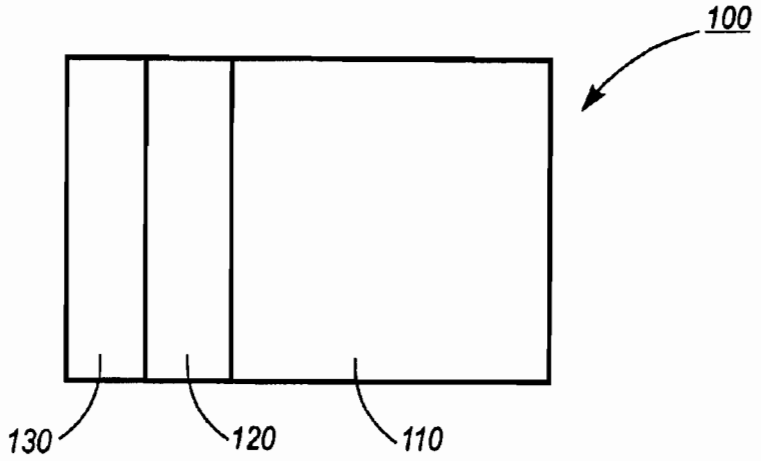


FIG. 1

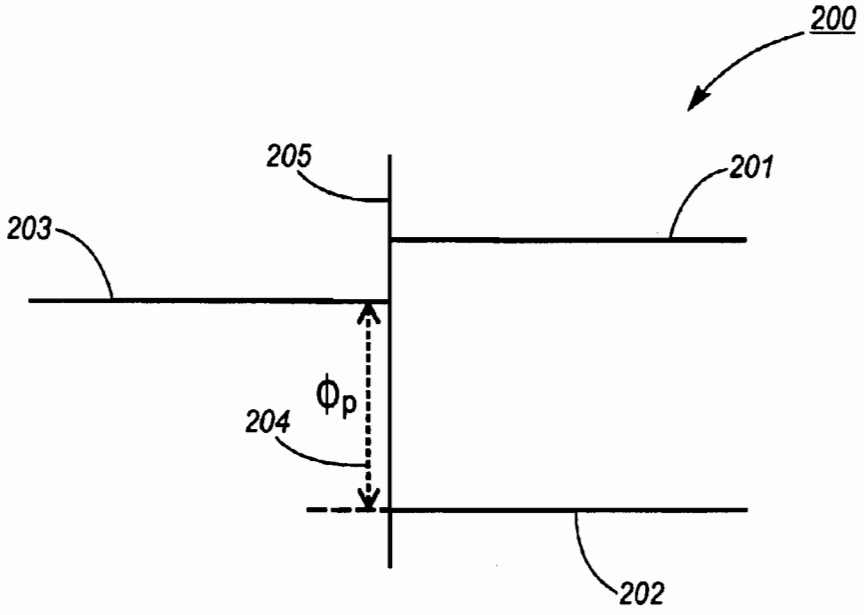


FIG. 2

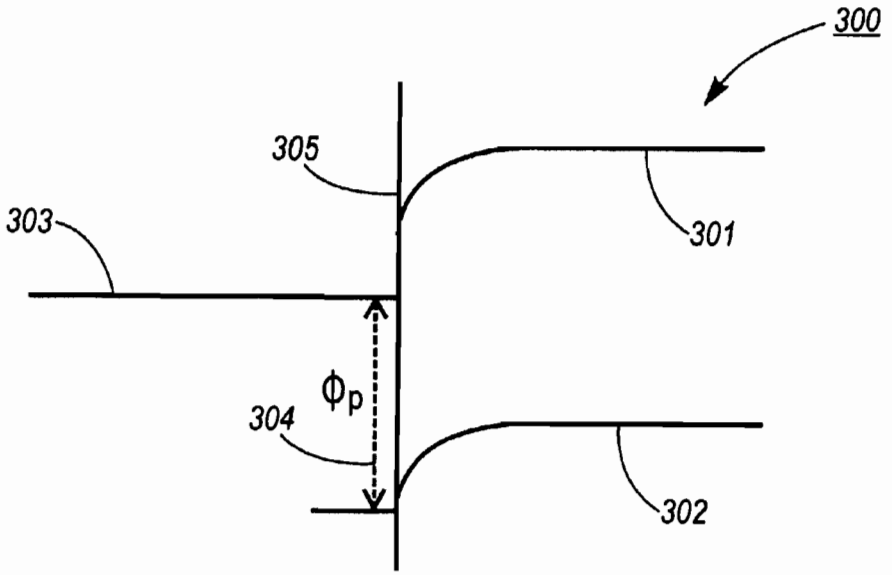

300
305
303
301
ϕ_p
304
302

FIG. 3

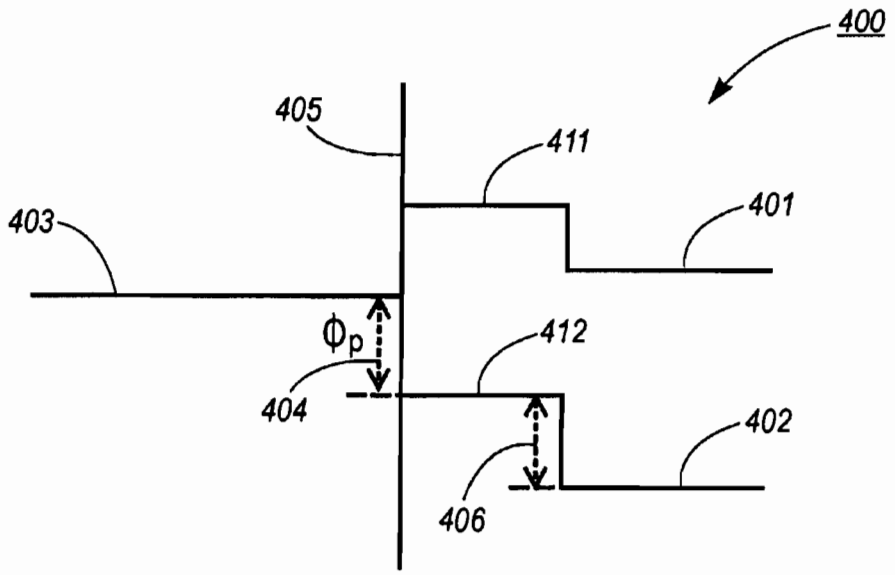

400
405
411
403
401
ϕ_p
412
404
402
406

FIG. 4

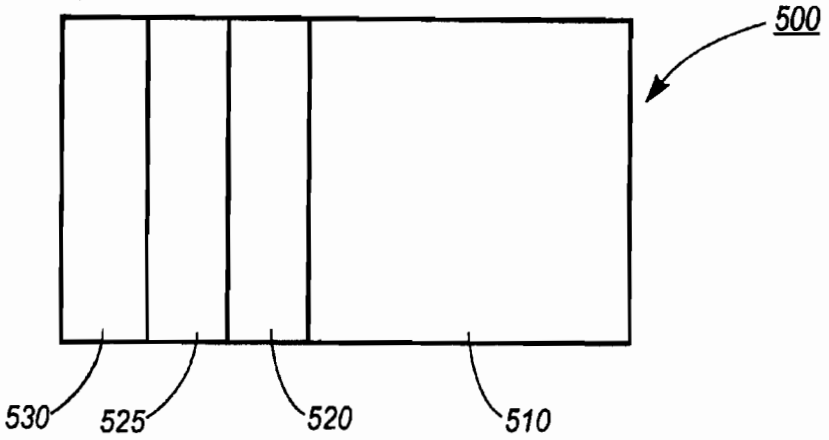

500
530
525
520
510

FIG. 5

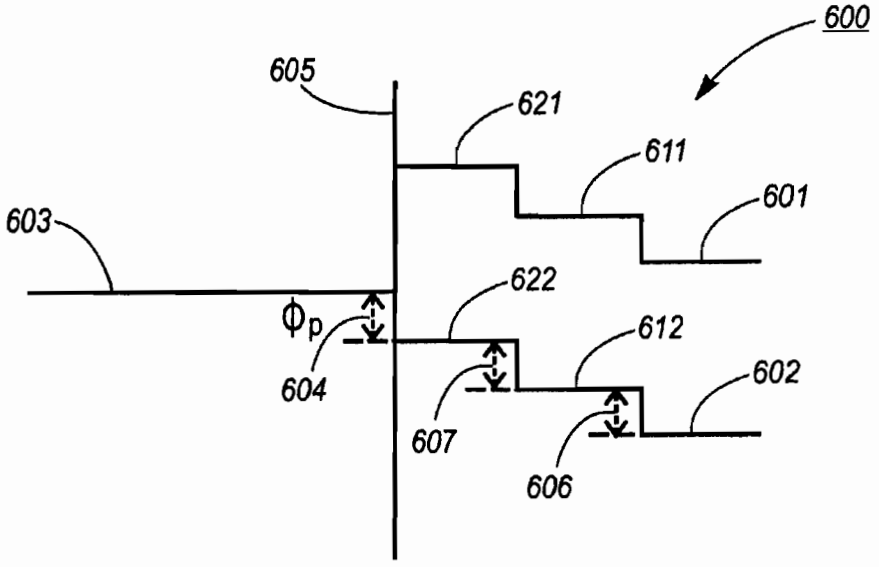

600
605
621
611
601
603
622
612
602
ϕ_p
604
607
606

FIG. 6

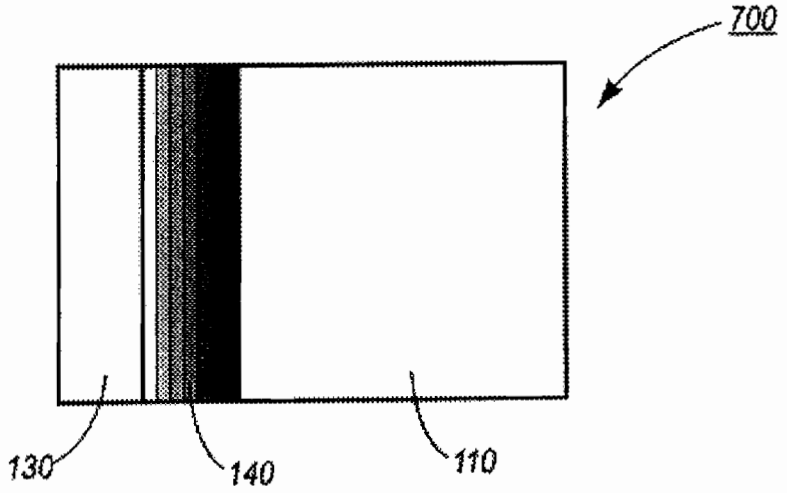


FIG. 7

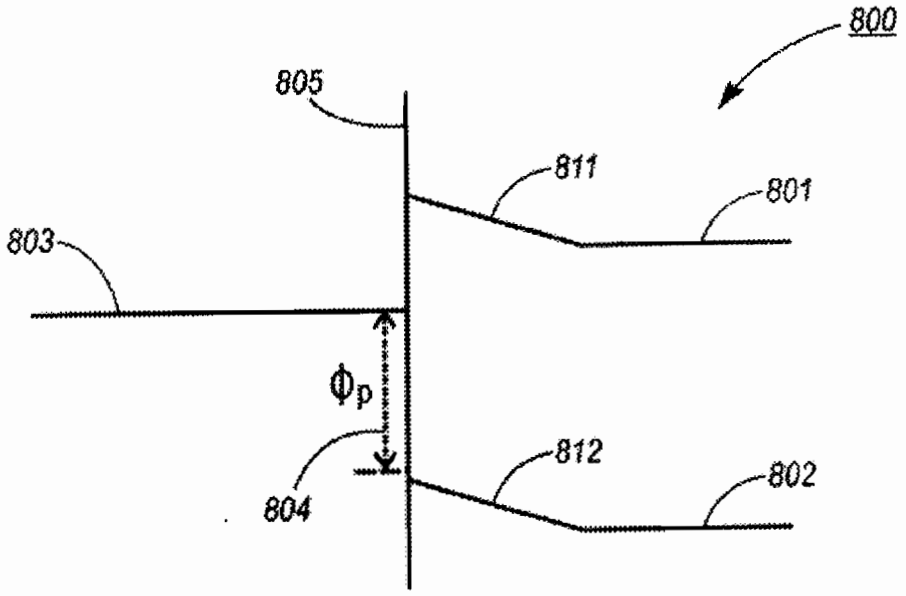


FIG. 8

SEMICONDUCTOR STRUCTURES HAVING REDUCED CONTACT RESISTANCE

BACKGROUND OF THE INVENTION

1. Field of Invention

The invention is directed to group III–V nitride semiconductor devices.

2. Description of Related Art

III–V semiconductors are compound semiconductors containing a group III element and a group V element. Gallium nitride (GaN) is one such semiconductor, with gallium from group III and nitrogen from group V. GaN is useful in laser diodes, and is especially useful in emitting light in the blue or UV region of the electromagnetic spectrum. GaN is able to emit in this region due to its large band gap. The large band gap of GaN allows emission of light with a large energy and short wavelength, which are characteristics of the blue or UV part of the electromagnetic spectrum.

Nevertheless, the large band gap present in many nitride-based group III–V semiconductors creates a large p-type contact resistance between the semiconductor structures and the metal contacts used in such group III–V semiconductor devices. This large contact resistance arises because of the difference between the energy level of the valence band in the group III–V material and the Fermi level of the metal used to form the metal contacts. The large contact resistance contributes to the large voltage required to drive these group III–V semiconductor devices, which leads to greater power use, can cause device heating and operational difficulties, and can cause device degradation and limited device life.

As a possible solution, high p-doping of GaN may allow carriers to tunnel through the barrier between the metal contacts and the semiconductor structures. However, obtaining such high p-dopant levels may itself be difficult for other reasons.

SUMMARY OF THE INVENTION

Forming high quality ohmic contacts to group III–V semiconductor materials, such as, for example, p-type gallium nitride, is an outstanding problem in nitride device design. The lineup between the gallium nitride valence band and the Fermi level of most metals is such that a large offset exists. That is, a large p-type Schottky barrier height, ϕ_p, occurs. This large Schottky barrier height ϕ_p makes it difficult to inject holes into the gallium nitride valence band. Even metals with large values for the work function, such as gold, nickel, palladium and platinum, having work function values of 5.1 to 5.5 eV, 5.1 to 5.4 eV, 5.1 to 5.6 eV, and 5.7 eV, respectively, fail to produce a Schottky barrier height ϕ_p that is sufficiently small to facilitate hole injection, because of the low energetic position of the gallium nitride valence band.

This invention provides methods for forming group III–V semiconductor devices having contact interlayers between the metal contact layer and the active group III–V semiconductor structure.

This invention separately provides a semiconductor device having a variable group III–V contact interlayer between a first group III–V material and a metal contact layer.

This invention further provides a variable group III–V contact interlayer that has a plurality of homogenous sublayers, each homogeneous sublayer having a different composition.

This invention alternatively further provides a variable group III–V contact interlayer that has at least one heterogeneous layer, each heterogeneous layer having a varying composition.

In various exemplary embodiments of a semiconductor device according to this invention, a gallium phosphide or gallium nitride phosphide interlayer is used to achieve contact formation on p-type gallium nitride. In the various exemplary embodiments, gallium phosphide is used because the energetic position of its valence band is about 1.3 eV above the valence band of the gallium nitride. This higher valence band position makes it much easier to form a p-type ohmic contact between gallium phosphide and the metal contact layers. An interlayer of gallium phosphide or of gallium nitride phosphide between the metal contact layer and the p-doped gallium nitride semiconductor structure therefore facilitates hole injection into the p-doped gallium nitride.

In various exemplary embodiments, a gallium phosphide interlayer or a gallium nitride phosphide interlayer can be used to divide the large energy difference between the metal contact layer and the gallium nitride semiconductor structure. In various other exemplary embodiments, multiple layers with varying concentrations of phosphide or nitride phosphide may also be used to divide the large energy difference between the metal contact layer and the gallium nitride semiconductor structure. In still other various exemplary embodiments, grading the composition of a $GaN_{1-x}P_x$ interlayer from pure gallium nitride towards an increasingly higher proportion of phosphide can be used to divide the large energy difference between the metal contact layer and the gallium nitride semiconductor structure. It should also be appreciated that two or more such heterogeneous composition interlayers would also be used.

The structure of this invention is not limited to forming an ohmic contact to gallium nitride, but also applies to contacts to other nitrides, InN, AlN or nitride alloys (InGaN, AlGaN, AlInN).

These and other features and advantages of this invention are described in, or are apparent from, the following detailed description of various exemplary embodiments of the systems and methods according to this invention.

BRIEF DESCRIPTION OF DRAWINGS

Various exemplary embodiments of this invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** shows the general structure of a first exemplary embodiment of a semiconductor device having a semiconductor contact interlayer according to this invention;

FIG. **2** schematically illustrates the band lineup between different materials under flat band conditions;

FIG. **3** schematically illustrates the band lineup between different materials including the effect of band bending;

FIG. **4** schematically illustrates the band lineup at the junctions between the metal and the semiconductor layer in the semiconductor structure shown on FIG. **1**;

FIG. **5** shows the structure of a second exemplary embodiment of a semiconductor device having a plurality of semiconductor contact interlayers according to this invention;

FIG. **6** schematically illustrates the band lineup at the junctions between the metal contact layer, the semiconductor contact interlayers and the group III–V semiconductor layer in the semiconductor structure shown in FIG. **5**;

FIG. **7** shows the structure of a third exemplary embodiment of a semiconductor device having at least one variable

semiconductor contact interlayer between the metal contact layer and the group III–V semiconductor structure according to this invention; and

FIG. **8** schematically illustrates the band lineup at the junctions between the metal contact layer, the variable semiconductor contact layer and the group III–V semiconductor layer in the semiconductor structure shown in FIG. **7**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The following detailed description of this invention is focused on GaP and GaPN contact interlayers between a metal contact layer and p-type doped GaN semiconductor layer. However, it should be appreciated that this invention is not limited to such materials, for either the base semiconductor layer or for the contact interlayers. In general, this invention can be used with any group III–V semiconductor layer to which a metal contact is desired, but for which the contact resistance will be larger than desired. Likewise, any group III–V semiconductor materials having an appropriate relationship according to this invention with the valence level and the work function values of the base semiconductor material and the metal used in the contact can be used in the systems and methods according to this invention.

In particular, the semiconductor materials usable in this invention are not limited to gallium nitride, but also includes other nitrides, such as InN or AlN, or nitride alloys, such as InGaN, AlGaN, or AlInN. Thus, it should be appreciated that the following exemplary embodiments are illustrative only, and are not intended to limit the literal or equivalence scope of the appended claims.

FIG. **1** shows the structure of a first exemplary embodiment of a semiconductor device **100** according to this invention. As shown in FIG. **1**, the semiconductor device **100** includes a first group III–V layer **110**. A second group III–V layer **120** is formed on or over the first group III–V layer **110**. A metal layer **130** is formed on or over the second group III–V layer **120**. In various exemplary embodiments, the first group III–V layer **110** is a gallium nitride layer. However, it should be appreciated that any known or later-developed group III–V type semiconductor material that has an undesirably large energy difference with the metal used in the metal layer **130** can be used in the first semiconductor layer **110** according to this invention.

When the group III–V layer **110** is formed of gallium nitride, the group III–V layer **110** is doped with a suitable acceptor, such as magnesium.

FIG. **2** schematically illustrates the band lineup between different materials under flat band conditions. In particular, a first material, such as a metal, has a Fermi level **203** that is offset from the valence band **202** of a second material, such as a semiconductor. In flat-band conditions, the conduction band **201** and the valence band **202** of the semiconductor material are parallel with the Fermi level **203** of the metal. The difference between the Fermi level **203** of the metal and the valence band **202** of the semiconductor is the p-type Schottky barrier height ϕ_p **204** which occurs at the metal semiconductor junction **205**.

FIG. **3** schematically illustrates the band lineup between different materials when the effect of band bending is included. In particular, a first material, such as a metal, has a Fermi level **303** that is offset from the valence band **302** of the second material, such as a semiconductor that is doped. The conduction band **301** and the valence band **302** of the doped semiconductor material are bent near the metal-doped semiconductor junction **305**. The Fermi level **303** of the metal and the Fermi level of the doped semiconductor (not shown) must align in equilibrium. However, it should be appreciated that the Schottky barrier height ϕ_p**304** is the same as the Schottky barrier height ϕ_p **204**.

FIG. **4** schematically illustrates the band lineup at the junction between the metal layer **130** and the first and second semiconductor layers **110** and **120** of the semiconductor structure **100** shown in FIG. **1**. The band bending that generally occurs in the semiconductor structure **100** at the end near the metal semiconductor junction **405** is not shown for simplicity. In particular, the addition of the second group III–V layer **120** between the first group III–V layer **110** and the metal layer **130** creates a step in the band structure **400**. The valence band **412** and the conduction band **411** of the second group III–V semiconductor material **120** are both offset from the valence band **402** and conduction band **401** of the first group III–V semiconductor material **110**.

The valence-band offset **406** is the energy difference between the valence band of the second group III–V semiconductor material **120** and the valence band of the first group III–V semiconductor **110**. If the first semiconductor **110** is GaN and the second semiconductor **120** is GaP, the valence-band offset **406** is about 1.3 eV. As shown in FIG. **4**, the Schottky barrier height ϕ_p **404** between the valence band of the second semiconductor layer **120** and the Fermi level **403** of the metal of the metal layer **130** is decreased accordingly.

It should also be appreciated that the contact resistance depends exponentially on the Schottky barrier height ϕ_p **404**. Likewise, the interlayer resistance between the first and second semiconductor layers **110** and **120** is an exponential function of the band offset **406**. Thus, the contact resistance between the metal layer **130** and the second semiconductor layer **120** is reduced relative to an undivided contact resistance that would occur if the metal layer **130** were formed on the first semiconductor layer **110**. Additionally, the overall resistance (i.e., the sum of the contact resistance and the interlayer resistance) is less than the undivided contact resistance. In a realistic structure, band bending effects occur that bring the Fermi levels of the semiconductors and the metal in alignment, but they would not change the arguments made above for the flat-band conditions.

FIG. **5** shows the structure of a second exemplary embodiment of the semiconductor device **500** according to this invention. As shown in FIG. **5**, in this second exemplary embodiment, the semiconductor device **500** includes the first group III–V layer **110**, the second group III–V layer **120** formed on or over the first group III–V layer **110**, and a third group III–V layer **125** formed on or over the second group III–V layer **120**. The metal layer **130** is formed on or over the third group III–V layer **125**.

In various exemplary embodiments, the first group III–V layer **110** is a gallium nitride layer. However, it should be appreciated that any known or later-developed group III–V type semiconductor material that has an undesirably large energy difference with the metal layer **130** can be used in the first semiconductor layer **110** according to this invention. Again, when the group III–V layer **110** is formed of gallium nitride, the group III–V layer **110** is doped with a suitable acceptor, such as magnesium.

The first and second separate interlayers **120** and **125** have a valence band that is higher than that of the first group III–V semiconductor layer **110**. For instance, the third group III–V layer **125** may be a layer of gallium phosphide. In contrast, the second group III–V layer **120** may be a layer of gallium nitride phosphide. Moreover, it should be appreciated that,

in other various exemplary embodiments, there may be additional contact interlayers, beyond the second and third group III–V layers **120** and **125**, between the first group III–V semiconductor layers **110** and the metal layer **130**. Each group III–V semiconductor contact interlayer, such as the second and third group III–V layers **120** and **125** may have varying ratios of nitrogen and/or phosphorous or other appropriate elements. It should be noted that, although a mixture of phosphorous and nitrogen is used in the disclosed exemplary embodiment, any known or later-developed group III–V type semiconductor material that has a valence band that is higher than the first group III–V semiconductor layer **110** may be used as a contact interlayer between the first group III–V semiconductor **110** and the metal layer **130** in the second exemplary embodiment of the semiconductor structure **100** according to this invention.

FIG. **6** schematically illustrates the band lineup at the junctions between the metal layer **130** and the group III–V semiconductor layers **110**,**120** and **125** in the semiconductor structure **500** shown in FIG. **5**. As in FIG. **4**, the band bending at the metal-group III–V semiconductor junction **605** is again not shown for simplicity. As shown in the band diagram **600**, there are multiple stair-like structures in the band structure of the semiconductor device between the valence bands **602**, **612** and **622**, and the conduction bands **601**, **611** and **621**, respectively. This particular band structure is created by using a plurality of group III–V semiconductor contact interlayers between the first group III–V semiconductor layer **110** and the metal layer **130**. In this example, the semiconductor contact interlayer **125** closest to the metal semiconductor junction **605** may be a layer of gallium phosphide, while the semiconductor contact interlayer **120** between the gallium phosphide layer **125** and the first group III–V semiconductor layer **110** may be gallium nitride phosphide.

The valence-band offset **606** is the energy difference between the valence band **602** of the first group III–V semiconductor layer **110** and the valence band **612** of the first semiconductor contact interlayer **120**. The valence-band offset **607** is the energy difference between the valence band **612** of the first semiconductor contact interlayer **120** and the valence band **622** of the second semiconductor contact interlayer. The Schottky barrier height ϕ_p **604** is the energy difference between the metal Fermi level **603** and the valence band **622** of the second semiconductor contact interlayer **125**. It should be appreciated that the original Schottky barrier height ϕ_p **204** shown in FIG. **2** is further divided between the Schottky barrier height ϕ_p **604** and the two valence-band offsets **606** and **607** (or more if additional semiconductor contact interlayers were present). Additionally, it should be appreciated that there may be three or more semiconductor contact interlayers, each having, for example, a different ratio of phosphide to nitride.

FIG. **7** shows the structure of a third exemplary embodiment of semiconductor device **700** according to this invention. As shown in FIG. **7**, the semiconductor device **700** includes the group III–V layer **110**, a second group III–V layer **140** formed on or over the first group III–V layer **110** and the metal layer **130** formed on or over the second group III–V layer **140**. In particular, in this third exemplary embodiment, the second group III–V layer **140** has a varying concentration of two or more group V materials. For example, if the second group III–V layer **140** included nitrogen and phosphorous as the group V materials, the concentration of the group V materials could vary according to the formula $GaN_{1-x}P_x$, where the phosphorous concentration x increases with depth in the second group III–V layer **140** from a surface closest to the first group III–V layer.

That is, the group III–V material of the portion of the second group III–V layer **140** that is closest to the first group III–V semiconductor layer **110** might be gallium nitride. At the same time, the group III–V material of the portion of the second group III–V layer **140** that is closest to the metal layer **130** may be gallium nitride phosphide $GaN_{1-x}P_x$ with a given alloy concentration x. In particular, the portion of the second group III–V layer **140** that is closest to the metal layer **130** could be pure GaP, where x is equal to 1. In this structure, the composition of the gallium nitride phosphide in the middle of the group III–V layer **140** varies between these two extremes.

In various exemplary embodiments, the concentration of the group V materials varies linearly within the second group III–V layer **140**. However, it should be appreciated that, in various exemplary embodiments, the group V material that varies across the thickness of the second group III–V layer **720** can vary according to any desired continuous or non-continuous function. However, it should be appreciated that the actual concentrations will vary depending on various factors, including deposition method, temperature, and time constraints. Thus, in practice, the actual concentration variation along the thickness of the second group III–V layer may even be abrupt, and may appear, as shown in FIG. **5**, as discrete layers.

FIG. **8** schematically illustrates the band diagram for the third exemplary embodiment of the semiconductor structure **700** shown in FIG. **7**. As shown in FIG. **8**, the band diagram **800** has a continuously varying gradient in the conduction band **811** and the valence band **812** of the second group III–V layer **140** situated between the first group III–V layer **110** and the metal layer **130**. In contrast, the conduction band **801** and the valence band **802** of the first group III–V layer **120** generally does not have a gradient, as in the other exemplary embodiments, although it could. Again, as in FIGS. **4** and **6**, the band bending occurring at the metal semiconductor junction **805** is not shown for simplicity. Similarly, the Fermi level **803** of the metal layer **130** and the Fermi levels of the second group III–V layer **140** and the first group V semiconductor layer **110** must generally align.

It should be appreciated that, as noted earlier, the actual gradient within the second group III–V layer **140** may not be as continuous or smooth as that shown in FIG. **8**. Small steps may be created depending on the processing condition as mentioned before. The small steps may even appear to be similar to that shown in FIG. **6**. It should further be appreciated that the exemplary embodiments shown in FIGS. **5**–**8** could be combined, such that two or more interlayers could be provided, where at least one interlayer has a varying composition. Moreover, two interlayers having gradients having different slopes could be provided as the at least two interlayers.

It should also be appreciated that the composition of the semiconductor interlayer closest to the metal layer **130** can be varied by diffusing a portion of the metal layer closest to the adjacent semiconductor interlayer into that semiconductor interlayer, or vice-versa.

It should be appreciated that any number of different methods could be used to form the group III–V contact interlayers according to this invention, such as gallium phosphide on gallium nitride. However, the miscibility of these alloys is low. Hence, in various exemplary embodiments, non-equilibrium growth at low temperatures may be used. In various other exemplary embodiments, molecular beam epitaxy or metal-organic chemical vapor deposition may be used. It should be appreciated that there

is no particular requirement to deposit the gallium nitride phosphide contact interlayer using the same growth technique used to form the underlying nitride-based semiconductor structures. Since the group III–V contact interlayers are formed over a top surface of the group III–V semiconductor device, the other layers and/or structures of the group III–V semiconductor device can be grown first using the one or more growth techniques of choice. Each of the one or more group III–V contact interlayers can be deposited using a desired technique.

It should further be appreciated that the metal layer **130** can itself be a single layer formed using a single metal, a single layer formed using a number of different metals, or a single layer formed using one or more metals and one or more non-metals. The metal layer **130** can also be formed as a plurality of separate sublayers, where each sublayer can be formed using a single metal, a number of different metals, or one or more metals and one or more non-metals. In particular, the specific composition of the metal layer is not important to the operation or scope of the systems and methods of this invention. Rather, the only parameter of the metal layer that need be considered is the Fermi level of the portion of the metal layer that is immediately over the adjacent semiconductor interlayer.

Finally, it should be appreciated that electronic devices that could make use of the semiconductor structures or devices shown in FIGS. **1** and **4–8** include transistors, sensors, optoelectronic devices, diodes, optical detectors, laser diodes and light emitting diodes. Furthermore, systems that incorporate such electronic devices include display devices, black and white or color image forming devices, optical communication devices, optical storage devices, black and white or color facsimile machines, black and white or color laser printers, black and white or color multipurpose devices, fiber-optic networks, microprocessors, gate arrays, radio-frequency transmitters and receivers, and digital signal processors.

While this invention has been described in conjunction with the exemplary embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the exemplary embodiments of the invention, as set forth above, are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A semiconductor device comprising:

a first p-doped group III–V semiconductor layer having a first conduction band energy level and a first valence band energy level,

a second p-doped group III–V semiconductor layer formed over the first p-doped group III–V semiconductor layer, and having a second conduction band energy level and a second valence band energy level; and

a metal layer formed over the second p-doped group III–V semiconductor layer and having a Fermi energy level,

wherein the Fermi energy level is above the first and second valence band energy levels and the second valence band energy level is between the Fermi energy level of the metal and the first valence band energy level.

2. The semiconductor device of claim **1**, wherein the first p-doped group III–V semiconductor layer comprises at least one of gallium nitride and an alloy of gallium nitride.

3. The semiconductor device of claim **1**, wherein the second p-doped group III–V semiconductor layer comprises at least one of gallium phosphide and at least one gallium phosphide nitride alloy.

4. The semiconductor device of claim **1**, wherein a portion of the metal layer is diffused into the second p-doped group III–V semiconductor layer.

5. The semiconductor device of claim **1**, wherein the metal layer comprises at least one of gold, nickel, palladium, or platinum.

6. The semiconductor device of claim **1**, wherein:

the second p-doped group III–V semiconductor layer comprises a plurality of p-doped group III–V semiconductor sublayers;

each p-doped group III–V semiconductor sublayer has a different composition and a distinct valence-band energy level; and

the distinct valence-band energy levels of the plurality of p-doped group III–V semiconductor sublayers are ordered in increasing order from the first valence-band energy level to the Fermi energy level.

7. The semiconductor device of claim **1**, wherein the second p-doped group III–V semiconductor layer comprises a p-doped group III–V semiconductor layer having a varying composition across its thickness, a valence-band energy level of the second p-doped group III–V semiconductor layer varying from at least the first valence-band energy level to at most the Fermi energy level across its thickness.

8. The semiconductor device of claim **7**, wherein the valence-band energy level of the second p-doped group III–V semiconductor layer varies substantially linearly across its thickness.

9. The semiconductor device of claim **7**, wherein the valence-band energy level of the second p-doped group III–V semiconductor layer varies substantially continuously across its thickness.

10. The semiconductor device of claim **1**, wherein the second p-doped group III–V semiconductor layer comprises a plurality of p-doped group III–V semiconductor sublayers, at least one of the plurality of p-doped group III–V semiconductor sublayers having a varying composition across its thickness such that, for each p-doped group III–V semiconductor sublayer that has a varying composition across its thickness, a valence-band energy level of that second p-doped group III–V semiconductor sublayer varies across the thickness of that second p-doped group III–V semiconductor sublayer.

11. The semiconductor device of claim **10**, wherein the valence-band energy level of at least one of the at least one p-doped group III–V semiconductor sublayer that has a varying composition across its thickness varies substantially linearly across the thickness of that second p-doped group III–V semiconductor sublayer.

12. The semiconductor device of claim **10**, wherein the valence-band energy level of at least one of the at least one p-doped group III–V semiconductor sublayer that has a varying composition across its thickness varies substantially continuously across the thickness of that second p-doped group III–V semiconductor sublayer.

13. The semiconductor device of claim **10**, wherein the plurality of p-doped group III–V semiconductor sublayers comprises:

a first sublayer having a varying composition across its thickness; and

a second sublayer having a generally constant composition across its thickness.

14. The semiconductor device of claim **10**, wherein the plurality of p-doped group III–V semiconductor sublayers comprises:

a first sublayer having a varying composition across its thickness, the composition of the first sublayer varying across the thickness of the first sublayer according to a first function; and

a second sublayer having a varying composition across its thickness, the composition of the second sublayer varying across the thickness of the second sublayer according to a second function that is different that the first function.

15. An electronic device, comprising the semiconductor device of claim **1**.

16. The electronic device of claim **15**, wherein the electronic device is one of a transistor, a sensor, an optoelectronic device, a diode, an optical detector, a laser diode and a light emitting diode.

17. An image forming apparatus, comprising at least one electronic device of claim **16**.

18. The image forming apparatus of claim **17**, wherein the image forming apparatus is one of a laser printer, a digital copier, a facsimile machine, a color laser printer, a color digital copier, a color facsimile machine, and a multipurpose image forming device.

19. An electronic system, comprising at least one electronic device of claim **16**.

20. The electronic system of claim **19**, wherein the electronic system is one of a display device, an image forming device, an optical communication device, an optical storage device, a facsimile machine, a laser printer, a fiber-optic network, a microprocessor, a gate array, a radio-frequency transmitter, a radio-frequency receiver, and a digital signal processor.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,605,832 B2
APPLICATION NO. : 09/682174
DATED : August 12, 2003
INVENTOR(S) : Christian G Vandewalle

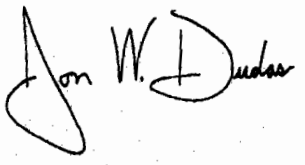
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 3, insert as a new paragraph:

This invention was made with Government support under Agreement No. MDA972-96-3-0014 awarded by ARPA. The Government has certain rights in this invention.

Signed and Sealed this

Eighth Day of August, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office