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Attorneys for Plaintiffs
LSI Corporation and Agere Systems Inc.

UNITED STATES DISTRICT COURT

FOR THE CENTRAL DISTRICT OF CALIFORNIA

WESTERN DIVISION

LSI CORPORATION and AGERE SYSTEMS INC., Plaintiffs, v. FUNAI ELECTRIC COMPANY, LTD.; FUNAI CORPORATION, INC.; FUNAI SERVICE CORPORATION; and P&F USA, INC., Defendants.	CASE NO. CV 12 2047 R (CWx) COMPLAINT FOR PATENT INFRINGEMENT DEMAND FOR JURY TRIAL

Plaintiffs LSI Corporation ("LSI") and Agere Systems Inc. ("Agere") (LSI and Agere, collectively, "Plaintiffs"), by and through their undersigned counsel, based upon actual knowledge as to themselves and their own actions, and upon information and belief as to all other persons and events, hereby plead the following claims for patent infringement against Defendants Funai Electric Company, Ltd. ("Funai Japan"), Funai Corporation, Inc. ("Funai USA"), Funai Service Corporation ("Funai Service"), and P&F USA, Inc. ("P&F USA") (Funai Japan, Funai USA, Funai Service, and P&F USA, collectively, "Defendants"). Plaintiffs hereby allege as follows:

NATURE OF THE ACTION

1. This is an action arising under the patent laws of the United States based on Defendants' infringement of claims in patents owned by Plaintiffs. Plaintiffs seek damages for Defendants' infringement, enhancement of damages due to Defendants' willful infringement, and a permanent injunction restraining Defendants from further infringement.

PARTIES

2. Plaintiff LSI is a corporation organized and existing under the laws of Delaware, having its principal place of business at 1621 Barber Lane, Milpitas, California 95035. LSI is the assignee and owns all right, title, and interest in and to U.S. Patent Nos. 5,870,087 ("the '087 patent") and 6,982,663 ("the '663 patent").

3. Plaintiff Agere is a corporation organized and existing under the laws of Delaware, having its principal place of business at 1110 American Parkway NE, Allentown, Pennsylvania 18109. Agere is the assignee and owns all right, title, and interest in and to U.S. Patent Nos. 6,452,958 ("the '958 patent") and 6,707,867 ("the '867 patent"). Plaintiff Agere is a wholly-owned subsidiary of Plaintiff LSI.

4. Plaintiffs are innovative technology companies which own and license patents in the wireless communications, multimedia digital processing, optical electronics, storage, semiconductor, and other high technology fields.

5. On information and belief, Defendant Funai Japan is a corporation organized and existing under the laws of Japan, having its principal place of business at 7-7-1 Nakagaito, Daito City, Osaka 574-0013, Japan. On information and belief, Funai Japan, directly or indirectly through affiliates, subsidiaries, or other entities it owns and/or controls, makes, imports into the United States, distributes, sells, offers to sell, and/or services throughout the United States, including in this judicial district, audiovisual components and products containing the same sold under brand names such as Philips, Magnavox, Sylvania, Emerson, Funai, and Symphonic that Funai owns or licenses (the "Accused Products"). Said Accused Products include, but are

not limited to, digital televisions (DTVs), Blu-ray disc players, DVD players, home theater systems, DTV/DVD player combinations, and other similar audiovisual products in relevant part. Said Accused Products are sold and/or offered for sale at retail stores across the State of California, such as Wal-Mart, Target, and Best Buy, and online stores such as www.amazon.com, store.philips.com, www.walmart.com, www.target.com, www.bestbuy.com, and thus are available for purchase and consumption in the Central District of California. Furthermore, on information and belief, said Accused Products are imported into the United States through Funai USA's operations in Long Beach, California. Funai Japan has voluntarily and purposely placed these products into the stream of commerce with the expectation that they will be offered for sale and sold in the State of California and in this judicial district.

6. On information and belief, Defendant Funai USA is a corporation organized and existing under the laws of New Jersey, having its principal place of business at 201 Route 17 North, Rutherford, New Jersey 07070. Funai USA is a wholly owned sales subsidiary of Funai Japan, and conducts business throughout the United States, including in the Central District of California. Furthermore, Funai USA maintains operations in Long Beach, California for importing the accused products into the United States. On information and belief, Funai USA, directly or indirectly through affiliates, subsidiaries, or other entities it owns and/or controls, imports into the United States, distributes, sells, and/or offers to sell throughout the United States, including in this judicial district, audiovisual components and products containing the same sold under brand names such as Philips, Magnavox, Sylvania, Emerson, Funai, and Symphonic that Funai owns or licenses. Said products include, but are not limited to, DTVs, Blu-ray disc players, DVD players, home theater systems, DTV/DVD player combinations, and other similar audiovisual products in relevant part. Said Accused Products are sold and/or offered for sale at retail stores across the State of California such as Wal-Mart, Target, and Best Buy, and online

stores such as www.amazon.com, store.philips.com, www.walmart.com, www.target.com, www.bestbuy.com, and thus are available for purchase and consumption in the Central District of California. Funai USA has voluntarily and purposely placed these products into the stream of commerce with the expectation that they will be offered for sale and sold in the State of California and in this judicial district.

7. On information and belief, Defendant Funai Service is a corporation organized and existing under the laws of Ohio, having its principal place of business at 2200 Spiegel Drive, Groveport, Ohio 43125. On information and belief, Funai Service is a wholly owned service subsidiary of Funai Japan, and conducts business throughout the United States, including in this judicial district. On information and belief, Funai Service, directly or indirectly through affiliates, subsidiaries, or other entities it owns and/or controls, provides customer support and repair services, among other things, to Funai's customers throughout the United States, including the State of California, for Funai's audiovisual components and products containing the same sold under brand names such as Philips, Magnavox, Sylvania, Emerson, Funai, and Symphonic. Said products include, but are not limited, to DTVs, Blu-ray disc players, DVD players, home theater systems, DTV/DVD player combinations, and other similar audiovisual products in relevant part. Said Accused Products are sold and/or offered for sale at retail stores across the State of California such as Wal-Mart, Target, and Best Buy, and online stores such as www.amazon.com, store.philips.com, www.walmart.com, www.target.com, www.bestbuy.com, and thus are available for purchase and consumption in the Central District of California. Furthermore, on information and belief, Funai Service imports products from Funai Japan through Funai USA's operations in Long Beach, California. Funai Service has voluntarily and purposely provided services to support the sale or offer of sale of these products with the expectation that they will be offered for sale and sold in the State of California and in this judicial district.

8. On information and belief, Defendant P&F USA is a corporation organized and existing under the laws of Georgia with its principal place of business at 3015 Windward Plaza, Windward Fairways II, Suite 100, Alpharetta, Georgia 30005. On information and belief, P&F USA is a wholly owned sales subsidiary of Funai Japan, and conducts business throughout the United States, including in this judicial district. On information and belief, P&F USA, directly or indirectly through affiliates, subsidiaries, or other entities it owns and/or controls, imports into the United States, distributes, sells, and/or offers to sell throughout the United States, including the State of California, audiovisual components and products containing the same sold under the brand name Philips. Said products include, but are not limited to, DTVs, Blu-ray disc players, DVD players, home theater systems, DTV/DVD player combinations, and other similar audiovisual products in relevant part. Said Accused Products are sold and/or offered for sale at retail stores across the State of California such as Wal-Mart, Target, and Best Buy, in online stores such as www.amazon.com, store.philips.com, www.walmart.com, www.target.com, www.bestbuy.com, and thus are available for purchase and consumption in the Central District of California. Furthermore, on information and belief, P&F USA imports products from Funai Japan through Funai USA's operations in Long Beach, California. P&F USA has voluntarily and purposely placed these products into the stream of commerce with the expectation that they will be offered for sale and sold in the State of California and in this judicial district.

JURISDICTION AND VENUE

9. This is an action for patent infringement arising under the patent laws of the United States of America, Title 35 of the United States Code. This Court has subject matter jurisdiction over the matters pleaded herein under 28 U.S.C. §§ 1331 and 1338(a) in that this is a civil action arising out of the patent laws of the United States of America.

10. As detailed in paragraphs 5 through 8, above, Defendants regularly and

deliberately engage in activities that result in the sale, offer for sale, and/or servicing of infringing products in the State of California and in this judicial district. These activities violate the Plaintiffs' United States patent rights with respect to the '087, '663, '958, and '867 patents (collectively, the "Asserted Patents").

11. This Court has personal jurisdiction over Defendants because, among other things, Defendants have purposefully availed themselves of the laws and protections of the State of California by conducting substantial business within the State, resulting in the sale, offer for sale, and/or service of infringing products in the State of California and this judicial district. Furthermore, on information and belief, Funai USA and Funai Service have consented to jurisdiction in the State of California by appointing an agent for service of process in Los Angeles, California.

12. Venue is proper in the Central District of California pursuant to 28 U.S.C. §§ 1391(b), (c), and (d), and 1400(b).

FIRST CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 5,870,087)

13. Plaintiffs re-allege and incorporate by reference each and every allegation previously set forth in the Complaint as if fully set forth herein.

14. The '087 patent, entitled "MPEG Decoder System and Method Having a Unified Memory for Transport Decode and System Controller Functions," was duly issued on February 9, 1999 in the name of inventor Kwok Kit Chau. A true and correct copy of the '087 patent is attached as Exhibit A hereto.

15. The '087 patent has been in full force and effect since its issuance. Plaintiff LSI owns by assignment the entire right, title, and interest in and to the '087 patent, including the right to sue for the past, present, and future infringement thereof.

16. On information and belief, Defendants are aware of Plaintiffs' patent portfolio, including the '087 patent. To the extent Defendants are not on actual notice of the '087 patent, they are willfully blind to its existence and/or on constructive notice thereof.

17. On information and belief, Defendants have directly infringed and continue to directly infringe at least one claim of the '087 patent, in violation of 35 U.S.C. § 271(a), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products falling within the scope of at least one claim of the '087 patent.

18. On information and belief, Defendants have induced and continue to induce the infringement of at least one claim of the '087 patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively, knowingly, and/or recklessly aiding and abetting others (including Defendants' customers and end users) through activities such as marketing the Accused Products, creating and/or distributing data sheets, application notes, and/or similar materials with instructions on using the Accused Products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States, without license or authority from Plaintiffs, Accused Products that fall within the scope of the '087 patent.

19. On information and belief, Defendants contributed to and continue to contribute to the infringement of at least one claim of the '087 patent, in violation of 35 U.S.C. § 271(c), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products which embody a material part of the claimed invention of the '087 patent, knowing that such products and/or components are specially made and/or specially adapted for use in the infringement of these claims, and that they are not staple articles or commodities of commerce suitable for substantial non-infringing use.

20. Unless enjoined by this Court, Defendants will continue to infringe the '087 patent. As a result of the infringing conduct of each Defendant, Plaintiffs have suffered and will continue to suffer irreparable injury as a direct and proximate result of Defendants' conduct, for which there is no adequate remedy at law. Accordingly,

Plaintiffs are entitled to temporary, preliminary, and/or permanent injunctive relief against each infringement pursuant to 35 U.S.C. § 283.

21. As a result of the infringement of the '087 patent by Defendants, Plaintiffs have been damaged, and will continue to be damaged, by Defendants' conduct. Plaintiffs are therefore entitled to such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

22. Plaintiffs believe that Defendants' past and continuing infringement has been deliberate and willful, and that this case is therefore an exceptional case, which warrants an award of treble damages and attorneys' fees to Plaintiffs pursuant to 35 U.S.C. § 285.

SECOND CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 6,982,663)

23. Plaintiffs re-allege and incorporate by reference each and every allegation previously set forth in the Complaint as if fully set forth herein.

24. The '663 patent, entitled "Method and System for Symbol Binarization," was duly issued on January 3, 2006 in the name of inventor Lowell Winger. A true and correct copy of the '663 patent is attached as Exhibit B hereto.

25. The '663 patent has been in full force and effect since its issuance. Plaintiff LSI owns by assignment the entire right, title, and interest in and to the '663 patent, including the right to sue for past, present, and future infringement thereof.

26. On information and belief, Defendants are aware of Plaintiffs' patent portfolio, including the '663 patent. To the extent Defendants are not on actual notice of the '663 patent, they are willfully blind to its existence and/or on constructive notice thereof.

27. On information and belief, Defendants have directly infringed and continue to directly infringe at least one claim of the '663 patent, in violation of 35 U.S.C. § 271(a), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs,

Accused Products falling within the scope of at least one claim of the '663 patent.

28. On information and belief, Defendants have induced and continue to induce the infringement of at least one claim of the '663 patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively, knowingly, and/or recklessly aiding and abetting others (including Defendants' customers and end users) through activities such as marketing the Accused Products, creating and/or distributing data sheets, application notes, and/or similar materials with instructions on using the Accused Products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States, without license or authority from Plaintiffs, Accused Products that fall within the scope of the '663 patent.

29. On information and belief, Defendants contributed to and continue to contribute to the infringement of at least one claim of the '663 patent, in violation of 35 U.S.C. § 271(c), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products which embody a material part of the claimed invention of the '663 patent, knowing that such products and/or components are specially made and/or specially adapted for use in the infringement of these claims, and that they are not staple articles or commodities of commerce suitable for substantial non-infringing use.

30. Unless enjoined by this Court, Defendants will continue to infringe the '663 patent. As a result of the infringing conduct of each Defendant, Plaintiffs have suffered and will continue to suffer irreparable injury as a direct and proximate result of Defendants' conduct, for which there is no adequate remedy at law. Accordingly, Plaintiffs are entitled to temporary, preliminary, and/or permanent injunctive relief against each infringement pursuant to 35 U.S.C. § 283.

31. As a result of the infringement of the '663 patent by Defendants, Plaintiffs have been damaged, and will continue to be damaged, by Defendants'

conduct. Plaintiffs are therefore entitled to such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

32. Plaintiffs believe that Defendants' past and continuing infringement has been deliberate and willful, and that this case is therefore an exceptional case, which warrants an award of treble damages and attorneys' fees to Plaintiffs pursuant to 35 U.S.C. § 285.

THIRD CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 6,452,958)

33. Plaintiffs re-allege and incorporate by reference each and every allegation previously set forth in the Complaint as if fully set forth herein.

34. The '958 patent, entitled "Digital Modulation System Using Extended Code Set," was duly issued on September 17, 2002 in the name of inventor Richard D. J. van Nee. A true and correct copy of the '958 patent is attached as Exhibit C hereto.

35. The '958 patent has been in full force and effect since its issuance. Plaintiff Agere owns by assignment the entire right, title, and interest in and to the '958 patent, including the right to sue for past, present, and future infringements thereof.

36. On information and belief, Defendants are aware of Plaintiffs' patent portfolio, including the '958 patent. To the extent Defendants are not on actual notice of the '958 patent, they are willfully blind to its existence and/or on constructive notice thereof.

37. On information and belief, Defendants have directly infringed and continue to directly infringe at least one claim of the '958 patent, in violation of 35 U.S.C. § 271(a), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products falling within the scope of at least one claim of the '958 patent.

38. On information and belief, Defendants have induced and continue to induce the infringement of at least one claim of the '958 patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively, knowingly, and/or recklessly aiding and abetting others (including Defendants' customers and end users) through activities such as marketing the Accused Products, creating and/or distributing data sheets, application notes, and/or similar materials with instructions on using the Accused Products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States, without license or authority from Plaintiffs, Accused Products that fall within the scope of the '958 patent.

39. On information and belief, Defendants contributed to and continue to contribute to the infringement of at least one claim of the '958 patent, in violation of 35 U.S.C. § 271(c), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products which embody a material part of the claimed invention of the '958 patent, knowing that such products and/or components are specially made and/or specially adapted for use in the infringement of these claims, and that they are not staple articles or commodities of commerce suitable for substantial non-infringing use.

40. Unless enjoined by this Court, Defendants will continue to infringe the '958 patent. As a result of the infringing conduct of each Defendant, Plaintiffs have suffered and will continue to suffer irreparable injury as a direct and proximate result of Defendants' conduct, for which there is no adequate remedy at law. Accordingly, Plaintiffs are entitled to temporary, preliminary, and/or permanent injunctive relief against each infringement pursuant to 35 U.S.C. § 283.

41. As a result of the infringement of the '958 patent by Defendants, Plaintiffs have been damaged, and will continue to be damaged, by Defendants' conduct. Plaintiffs are therefore entitled to such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

42. Plaintiffs believe that Defendants' past and continuing infringement has been deliberate and willful, and that this case is therefore an exceptional case, which warrants an award of treble damages and attorneys' fees to Plaintiffs pursuant to 35 U.S.C. § 285.

FOURTH CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 6,707,867)

43. Plaintiffs re-allege and incorporate by reference each and every allegation previously set forth in the Complaint as if fully set forth herein.

44. The '867 patent, entitled "Wireless Local Area Network Apparatus," was duly issued on March 16, 2004 in the name of inventors Wilhelmus J. M. Diepstraten, Hendrick van Bokhorst, and Hans van Driest. A true and correct copy of the '867 patent is attached as Exhibit D hereto.

45. The '867 patent has been in full force and effect since its issuance. Plaintiff Agere owns by assignment the entire right, title, and interest in and to the '867 patent, including the right to sue for past, present, and future infringements thereof.

46. On information and belief, Defendants are aware of Plaintiffs' patent portfolio, including the '867 patent. To the extent Defendants are not on actual notice of the '867 patent, they are willfully blind to its existence and/or on constructive notice thereof.

47. On information and belief, Defendants have directly infringed and continue to directly infringe at least one claim of the '867 patent, in violation of 35 U.S.C. § 271(a), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products falling within the scope of at least one claim of the '867 patent.

48. On information and belief, Defendants have induced and continue to induce the infringement of at least one claim of the '867 patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively, knowingly, and/or recklessly

aiding and abetting others (including Defendants' customers and end users) through activities such as marketing the Accused Products, creating and/or distributing data sheets, application notes, and/or similar materials with instructions on using the Accused Products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States, without license or authority from Plaintiffs, Accused Products that fall within the scope of the '867 patent.

49. On information and belief, Defendants contributed to and continue to contribute to the infringement of at least one claim of the '867 patent, in violation of 35 U.S.C. § 271(c), by, among other things, making, using, offering to sell, selling, and/or importing into the United States, without authority or license from Plaintiffs, Accused Products which embody a material part of the claimed invention of the '867 patent, knowing that such products and/or components are specially made and/or specially adapted for use in the infringement of these claims, and that they are not staple articles or commodities of commerce suitable for substantial non-infringing use.

50. Unless enjoined by this Court, Defendants will continue to infringe the '867 patent. As a result of the infringing conduct of each Defendant, Plaintiffs have suffered and will continue to suffer irreparable injury as a direct and proximate result of Defendants' conduct, for which there is no adequate remedy at law. Accordingly, Plaintiffs are entitled to temporary, preliminary, and/or permanent injunctive relief against each infringement pursuant to 35 U.S.C. § 283.

51. As a result of the infringement of the '867 patent by Defendants, Plaintiffs have been damaged, and will continue to be damaged, by Defendants' conduct. Plaintiffs are therefore entitled to such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

52. Plaintiffs believe that Defendants' past and continuing infringement has been deliberate and willful, and that this case is therefore an exceptional case, which warrants an award of treble damages and attorneys' fees to Plaintiffs pursuant to 35

U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs pray for entry of judgment against each Defendant as follows:

A. That Defendants have directly infringed each of the Asserted Patents under 35 U.S.C. § 271(a);

B. That Defendants have induced the infringement by others of each of the Asserted Patents under 35 U.S.C. § 271(b);

C. That Defendants have contributed to the infringement by others of each of the Asserted Patents under 35 U.S.C. § 271(c);

D. That injunctions, preliminary and/or permanent, be issued by this Court restraining each Defendant, their respective affiliates, subsidiaries, officers, directors, employees, agents, servants, representatives, licensees, successors, assigns, and all persons in active concert or participation with each, from directly or indirectly infringing each of the Asserted Patents;

E. That each Defendant provide to Plaintiffs an accounting of all gains, profits, and advantages derived by each Defendant's direct or indirect infringement of the Asserted Patents, and that Plaintiffs be awarded damages adequate to compensate them for the wrongful infringement by each Defendant, in accordance with 35 U.S.C. § 284;

F. That the damages awarded to Plaintiffs with respect to each of the Asserted Patents be increased up to three times, in view of Defendants' willful infringement, in accordance with 35 U.S.C. § 284;

G. That this case be declared an exceptional one in favor of Plaintiffs under 35 U.S.C. § 285, and that Plaintiffs be awarded its reasonable attorneys' fees and other expenses incurred in connection with this action in accordance with 35 U.S.C. § 285 and Rule 54(d) of the Federal Rules of Civil Procedure;

H. That Plaintiffs be awarded their interest and costs of suit incurred in this action;

I. That Plaintiffs be awarded any other supplemental damages and interest on all damages;

J. That Plaintiffs be awarded such other and further relief as this Court may deem just and proper.

DATED: March 12, 2012

Respectfully submitted,

KILPATRICK TOWNSEND & STOCKTON LLP

By: _____

David E. Sipiora
Kenneth S. Chang
Kristopher L. Reed

Attorneys for Plaintiffs

LSI Corporation and Agere Systems Inc.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), Plaintiffs hereby demand a trial by jury on all issues triable to a jury.

DATED: March 12, 2012

Respectfully submitted,

KILPATRICK TOWNSEND & STOCKTON LLP

By: _____
David E. Sipiora
Kenneth S. Chang
Kristopher L. Reed

Attorneys for Plaintiffs

LSI Corporation and Agere Systems Inc.

64025190 v1

EXHIBIT A

US005870087A

United States Patent [19]

Chau

[11] Patent Number: 5,870,087

[45] Date of Patent: Feb. 9, 1999

[54] **MPEG DECODER SYSTEM AND METHOD HAVING A UNIFIED MEMORY FOR TRANSPORT DECODE AND SYSTEM CONTROLLER FUNCTIONS**

[75] Inventor: **Kwok Kit Chau**, Los Altos, Calif.

[73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.

[21] Appl. No.: **748,269**

[22] Filed: **Nov. 13, 1996**

[51] **Int. Cl.**[6] **G06T 13/00**

[52] **U.S. Cl.** **345/302**

[58] **Field of Search** 345/302, 418; 707/101, 102, 103, 104

[56] **References Cited**

U.S. PATENT DOCUMENTS

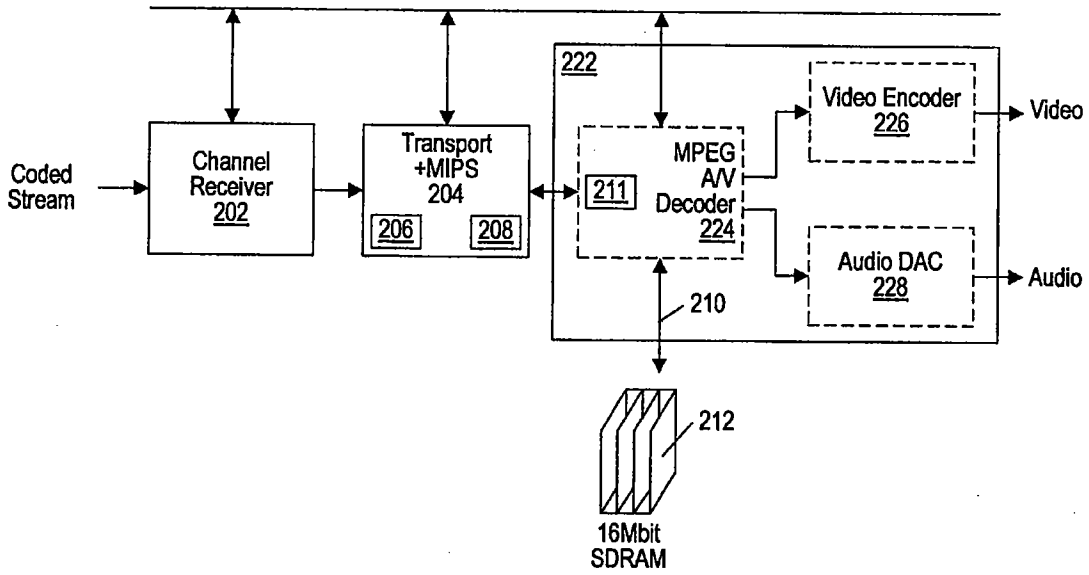
5,675,511	10/1997	Prasad et al.	345/302
5,692,213	11/1997	Goldberg et al.	345/302
5,767,846	6/1998	Nakamura et al.	345/302

Primary Examiner—Phu K. Nguyen
Assistant Examiner—Cliff N. Vo
Attorney, Agent, or Firm—Conley, Rose & Tayon; Jeffrey C. Hood

[57] **ABSTRACT**

An MPEG decoder system and method for performing video decoding or decompression which includes a unified memory for multiple functions according to the present invention. The video decoding system includes transport logic, a system controller, and MPEG decoder logic. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. The single unified memory is preferably a 16 Mbit memory. The MPEG decoder logic includes a memory controller which couples to the single unified memory, and each of the transport logic, system controller and MPEG decoder logic access the single unified memory through the memory controller. The video decoding system implements various frame memory saving schemes, such as compression or dynamic allocation, to more efficiently use the memory. In one embodiment, the memory is not required to store reconstructed frame data during B-frame reconstruction, thus considerably reducing the required amount of memory for this function. Alternatively, the memory is only required to store a portion of the reconstructed frame data. In addition, these savings in memory allow portions of the memory to also be used for transport and system controller functions. The present invention thus provides a video decoding system with reduced memory requirements.

20 Claims, 16 Drawing Sheets



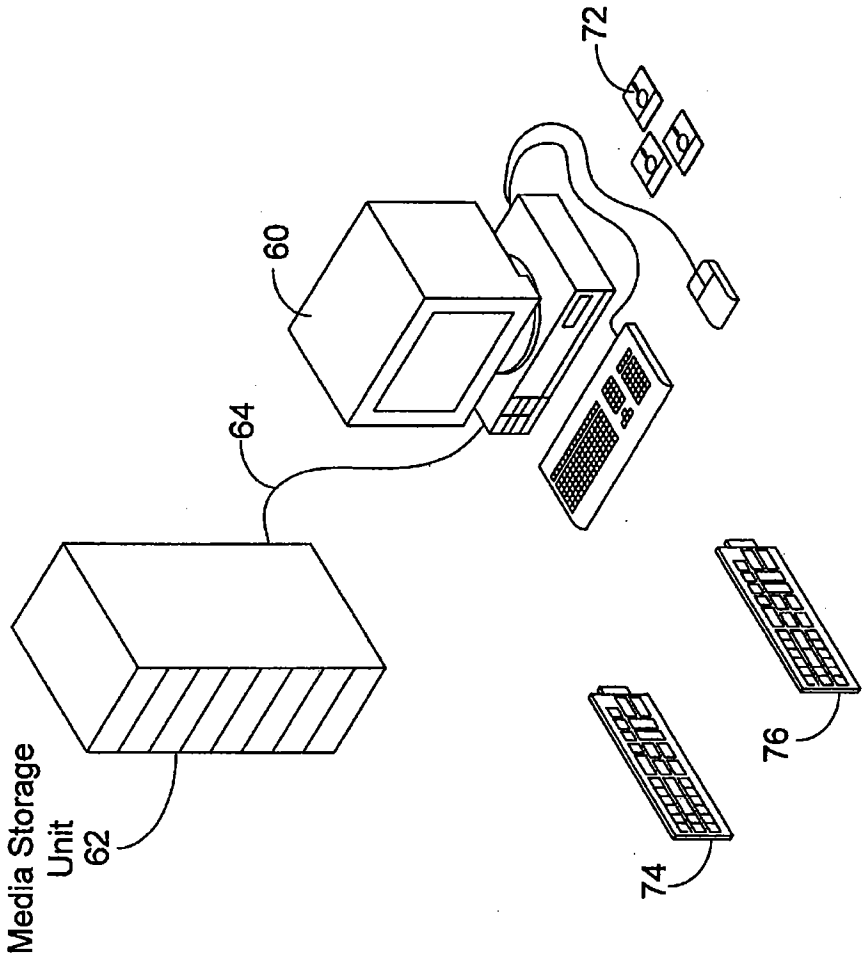


FIG. 1

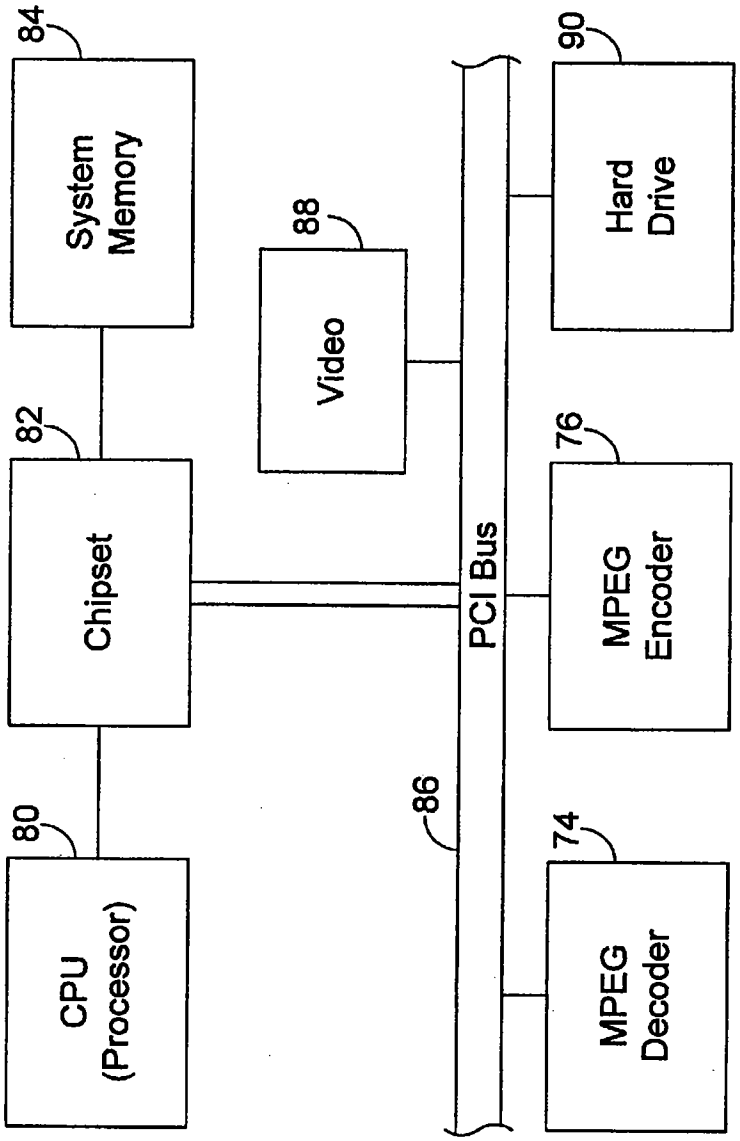

84
System Memory
88
Video
90
Hard Drive
82
Chipset
PCI Bus
76
MPEG Encoder
80
CPU (Processor)
86
74
MPEG Decoder

FIG. 2

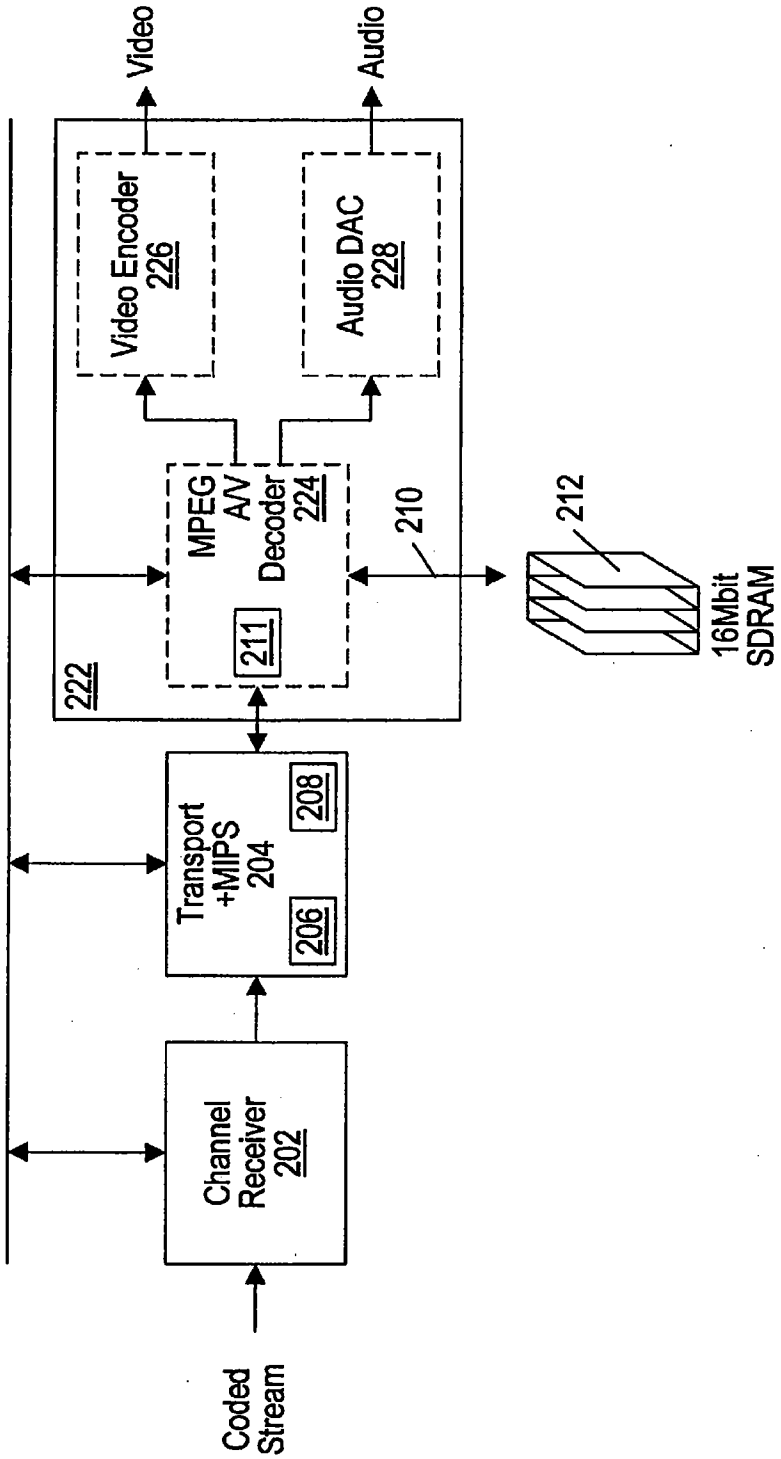

Video
Audio
Video Encoder 226
Audio DAC 228
MPEG A/V Decoder 224
211
210
212
16Mbit SDRAM
222
Transport +MIPS 204
208
206
Channel Receiver 202
Coded Stream

FIG. 3

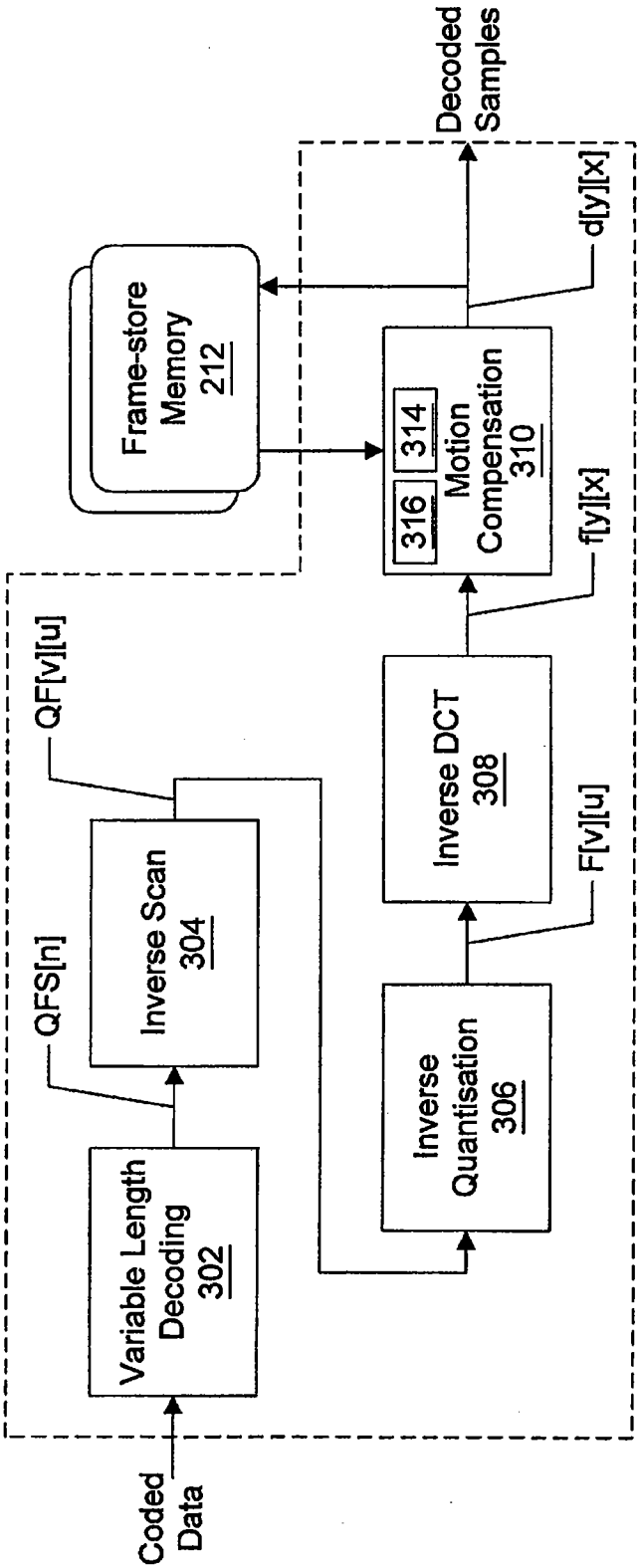

Decoded Samples
d[y][x]
Frame-store Memory 212
316
314
Motion Compensation 310
f[y][x]
QF[v][u]
Inverse DCT 308
F[v][u]
QFS[n]
Inverse Scan 304
Inverse Quantisation 306
Variable Length Decoding 302
Coded Data

FIG. 4

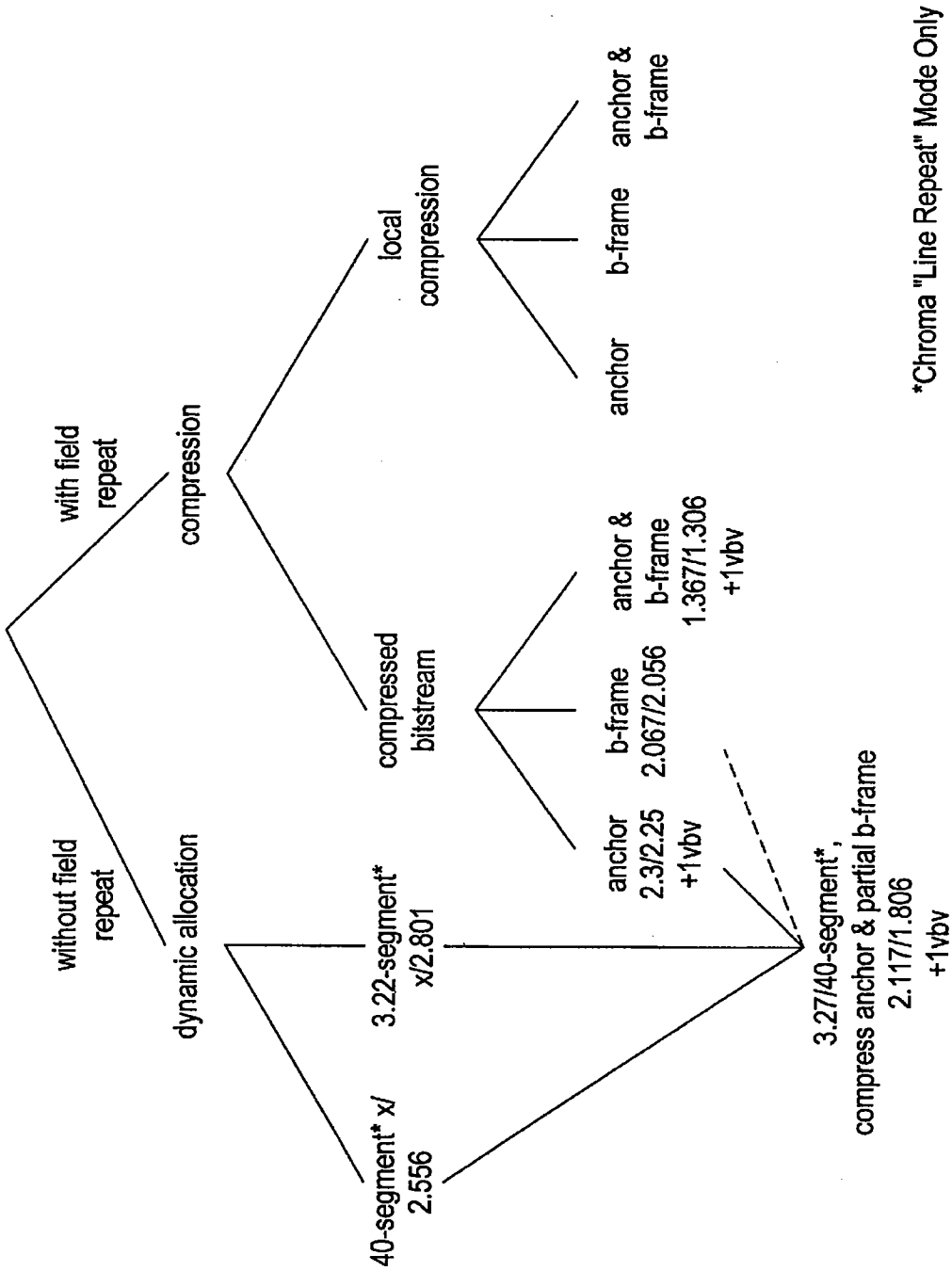

with field repeat
without field repeat
compression
dynamic allocation
local compression
compressed bitstream
anchor
b-frame
anchor & b-frame
anchor 2.3/2.25 +1vbv
b-frame 2.067/2.056
anchor & b-frame 1.367/1.306 +1vbv
3.22-segment* x/2.801
40-segment* x/ 2.556
3.27/40-segment*, compress anchor & partial b-frame 2.117/1.806 +1vbv
*Chroma "Line Repeat" Mode Only

FIG. 5

Table 1
MPEG Decoder. Memory Partition

	L64005		Compress Displayed Anchor	
frame store (number of frames)	NTSC 12,441,600 (3.000)	PAL 12,718,080 (2.556)	NTSC 9,538,560 (2.300)	PAL 11,197,440 (2.250)
vbv buffer	1,805,008	1,805,008	3,610,016	3,610,016
video non-instantaneous decode	430,765	520,575		
video-display sync	500,000	600,000		
audio buffer	28,672	28,672		
audio-video latency difference	19,200	23,040		
audio-display sync	12,800	15,360		
video transport buffer	4,096	4,096		
audio transport buffer	4,096	4,096		
4ms jitter at 15Mbps	60,000	60,000		
sub-total for channel buffer	2,864,637	3,060,847	4,669,645	4,865,855
packet header overhead	20,000	20,000		
OSD	675,840	808,192		
sub-total for software & data	775,139	170,097	1,873,171	(114,271)
Grand Total	16,777,216	16,777,216	14,208,205	16,063,295
frame store + channel buffer	15,306,237	15,778,927		

FIG. 6A

Table 1
MPEG Decoder: Memory Partition

Compress Anchor & Segment B		Compress B-Frame		Compress Anchor & B-Frame	
NTSC: 3.267 segments 8,778,240 (2.117)	PAL: 40 segments 8,985,600 (1.806)	NTSC 8,570,880 (2.067)	PAL 10,229,760 (2.056)	NTSC 5,667,840 (1.367)	PAL 6,497,280 (1.306)
3,610,016	3,610,016			3,610,016	3,610,016
4,669,645	4,865,855			4,669,645	4,865,855
2,633,491	2,097,569	4,645,859	2,658,417	5,743,891	4,585,889
13,447,885	13,851,455	11,435,517	13,290,607	10,337,485	11,363,135

FIG. 6B

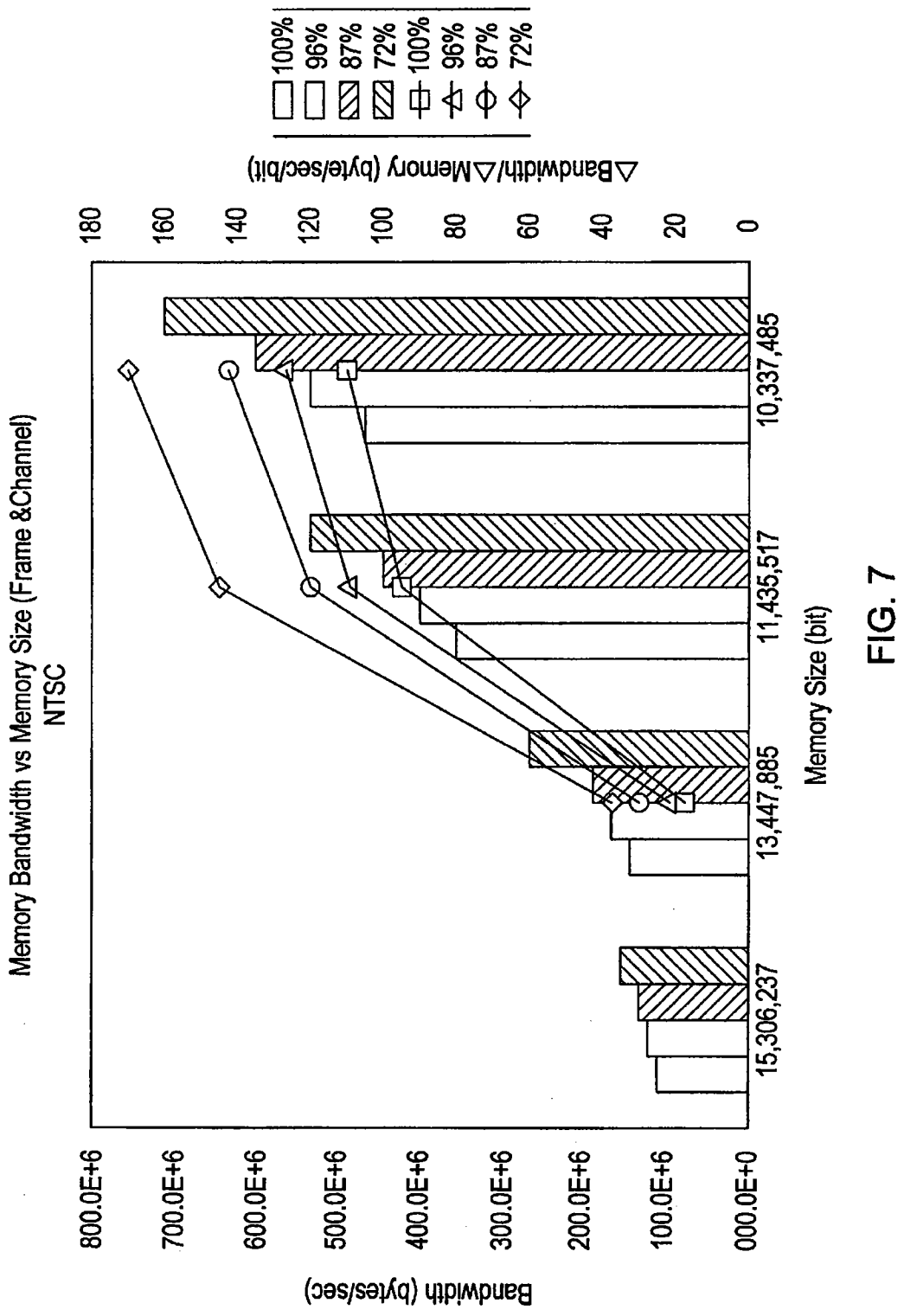

100%
96%
87%
72%
100%
96%
87%
72%
ΔBandwidth/ΔMemory (byte/sec/bit)
180
160
140
120
100
80
60
40
20
0
Memory Bandwidth vs Memory Size (Frame &Channel)
NTSC
10,337,485
11,435,517
13,447,885
15,306,237
Memory Size (bit)
800.0E+6
700.0E+6
600.0E+6
500.0E+6
400.0E+6
300.0E+6
200.0E+6
100.0E+6
000.0E+0
Bandwidth (bytes/sec)

FIG. 7

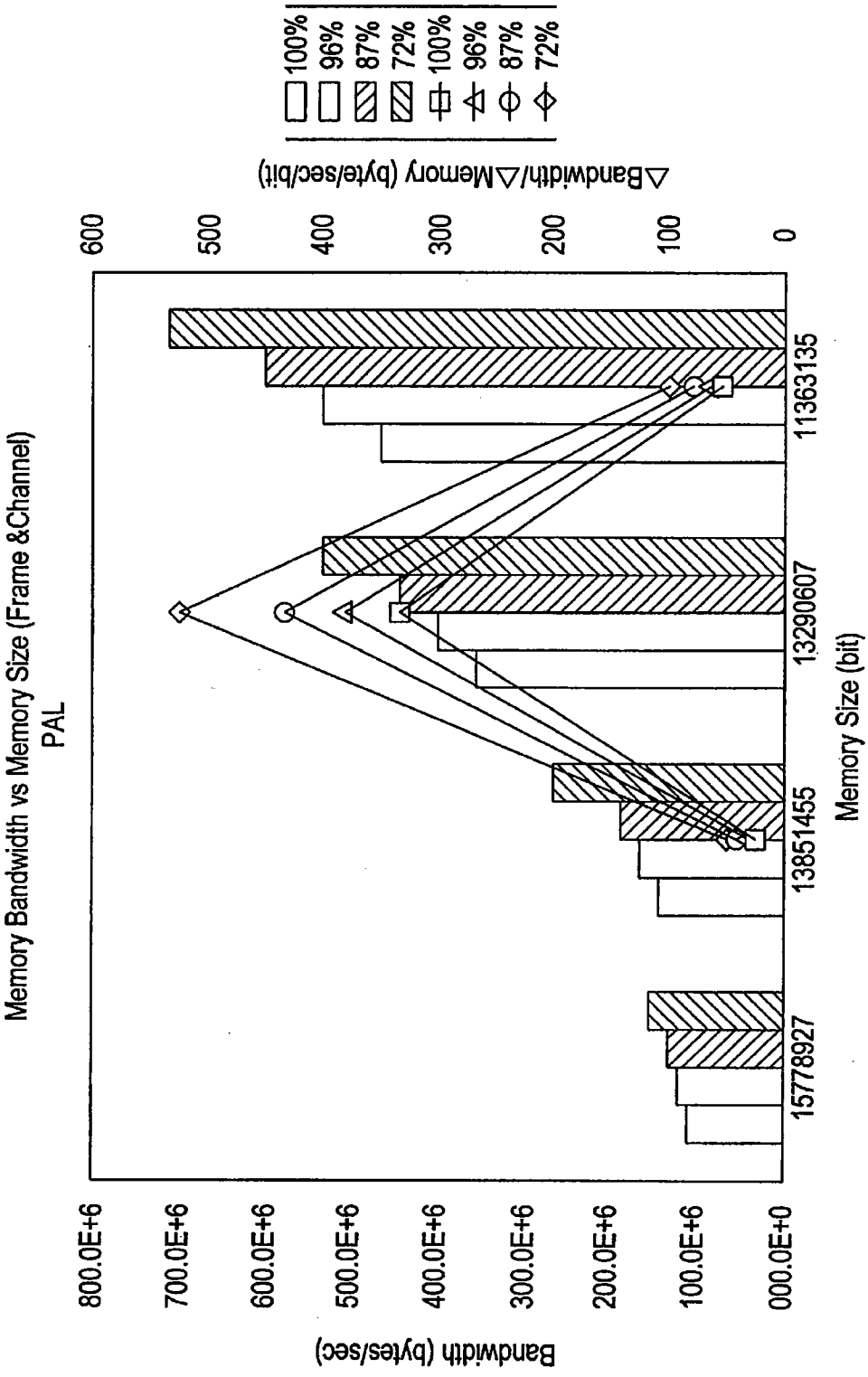

100%
96%
87%
72%
100%
96%
87%
72%
△Bandwidth/△Memory (byte/sec/bit)
600
500
400
300
200
100
0
Memory Bandwidth vs Memory Size (Frame &Channel)
PAL
11363135
13290607
13851455
15778927
Memory Size (bit)
800.0E+6
700.0E+6
600.0E+6
500.0E+6
400.0E+6
300.0E+6
200.0E+6
100.0E+6
000.0E+0
Bandwidth (bytes/sec)

FIG. 8

	bit	
	NTSC	PAL
Video Frames (incl. compressed)	10,583,248	10,790,608
VBV Buffer	1,805,008	1,805,008
Video Decode Buffer	430,765	520,575
Video-Display Sync Buffer	500,000	600,000
Audio Buffer	28,672	28,672
Audio-Video Latency Buffer	19,200	23,040
Audio-Display Sync Buffer	12,800	15,360
Transport Buffer	8,192	8,192
Jitter Buffer (4ms)	60,000	60,000
PES Header Overhead	20,000	20,000
OSD	675,840	808,192
MIPS Code and Data	2,633,491	2,097,569

FIG. 9

	Bandwidth (Mbyte/sec)	
	NTSC	PAL
Channel In/Out	18.82	15.98
Motion Compensation	72.70	72.59
Store	38.29	38.23
Display & OSD	30.38	30.38
TOTAL	160.19	157.18

- With 16x1M SDRAM running at 100 MHz, Bandwidth Available is 200Mbyte/sec
- Expecting 20Mbyte/sec for MIPS Code and Data

FIG. 10

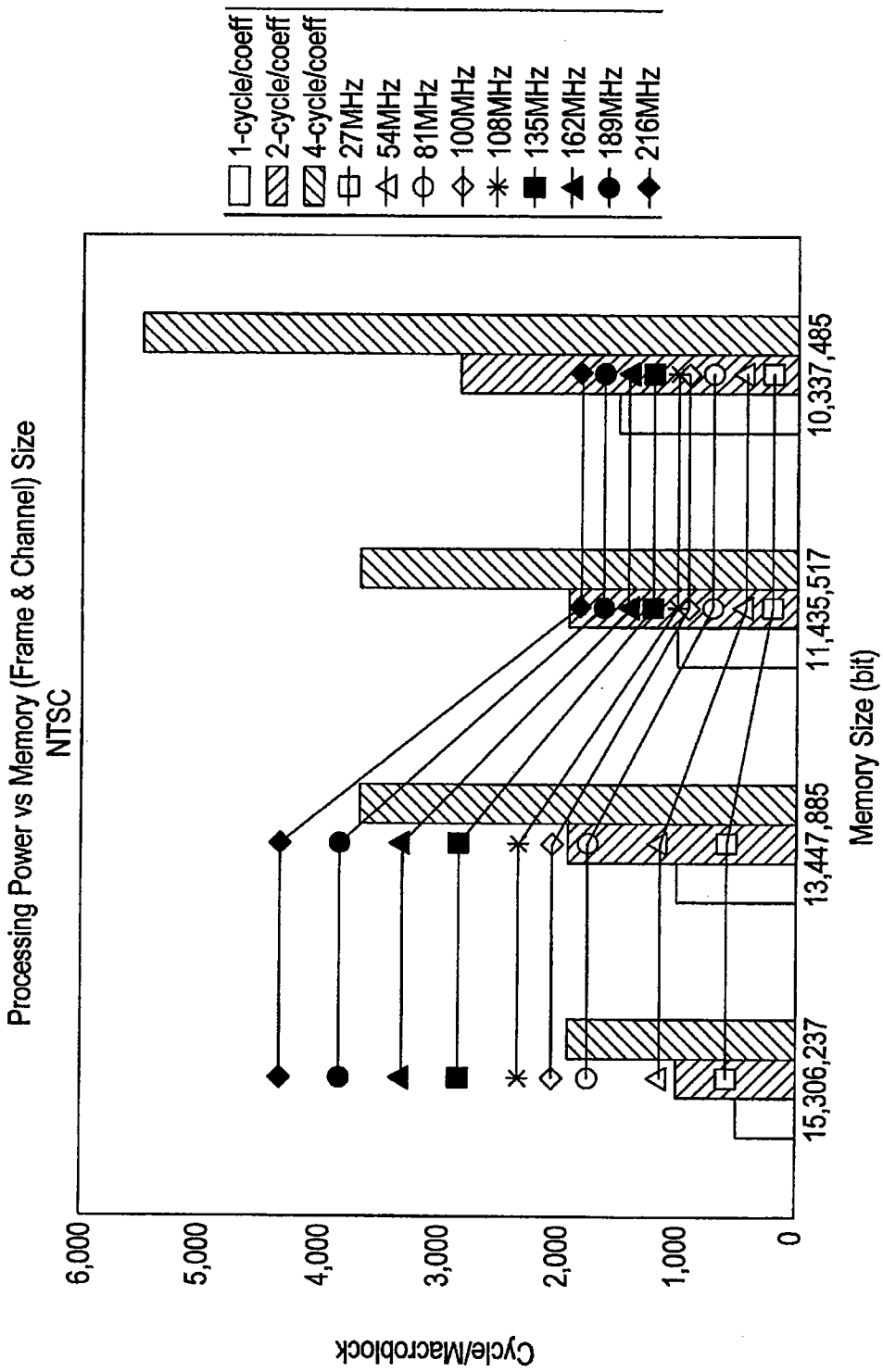

1-cycle/coeff
2-cycle/coeff
4-cycle/coeff
27MHz
54MHz
81MHz
100MHz
108MHz
135MHz
162MHz
189MHz
216MHz
Processing Power vs Memory (Frame & Channel) Size
NTSC
Cycle/Macroblock
6,000
5,000
4,000
3,000
2,000
1,000
0
Memory Size (bit)
10,337,485
11,435,517
13,447,885
15,306,237

FIG. 11

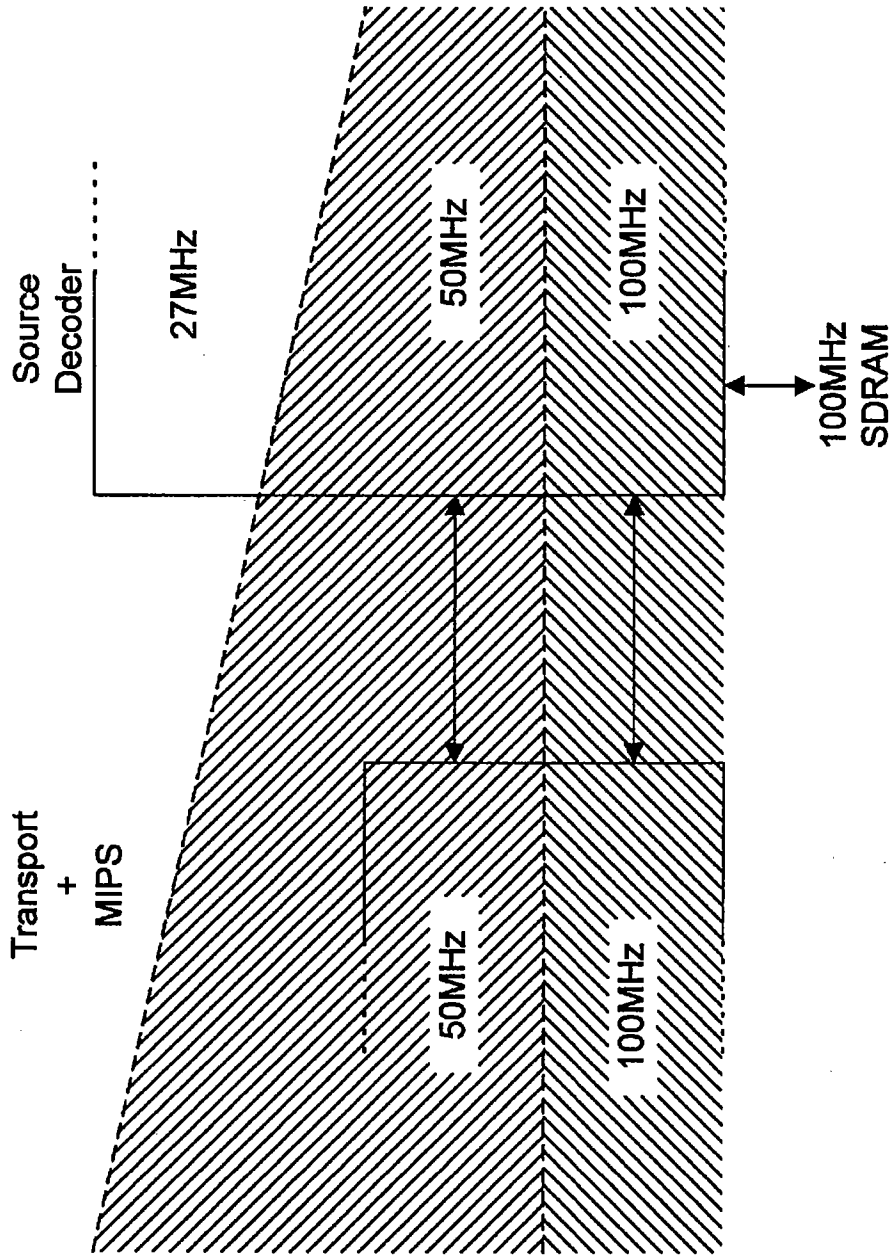

Source Decoder
27MHz
50MHz
100MHz
100MHz SDRAM
Transport + MIPS
50MHz
100MHz

FIG. 12

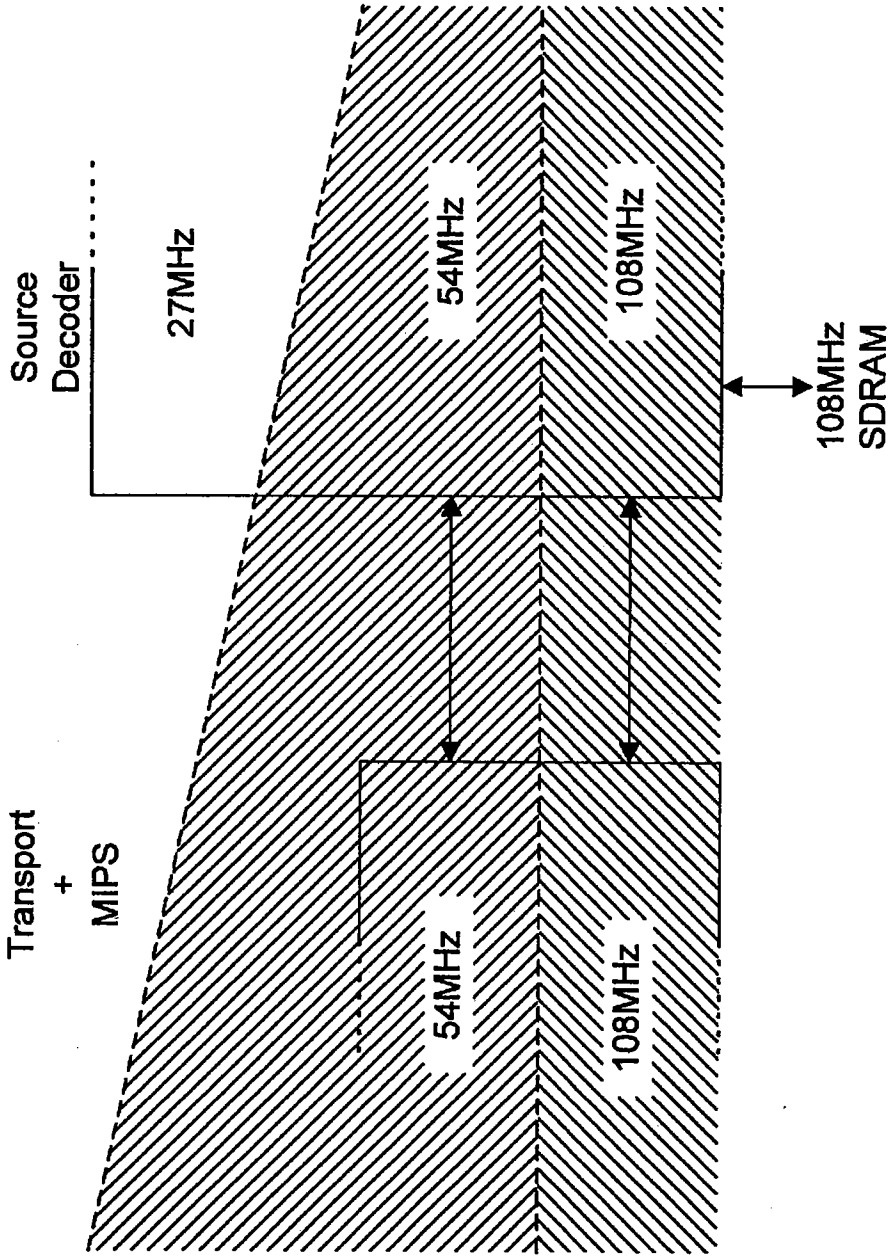
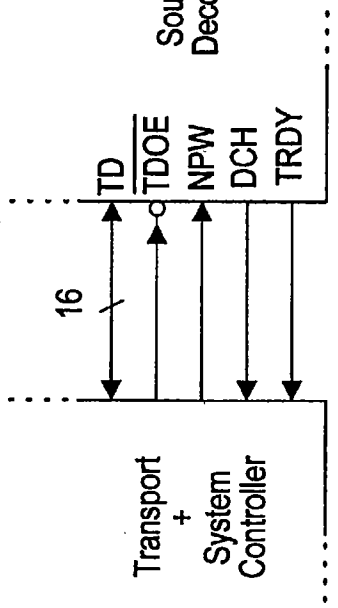

Source Decoder
27MHz
54MHz
108MHz
108MHz SDRAM
Transport + MIPS
54MHz
108MHz

FIG. 13



Signal	Description	Type
TD[15:0]	Transmission Data	Bidirectional
$\overline{\text{TDOE}}$	Transmission Data Output Enable (active low)	Input
NPW	New Packet Word (reset if TD[15:13]=000)	Input
DCH	Data Chain Hold (i.e. wait cycle request)	Output
TRDY	Transmission Ready (for new packet	Output

FIG. 14

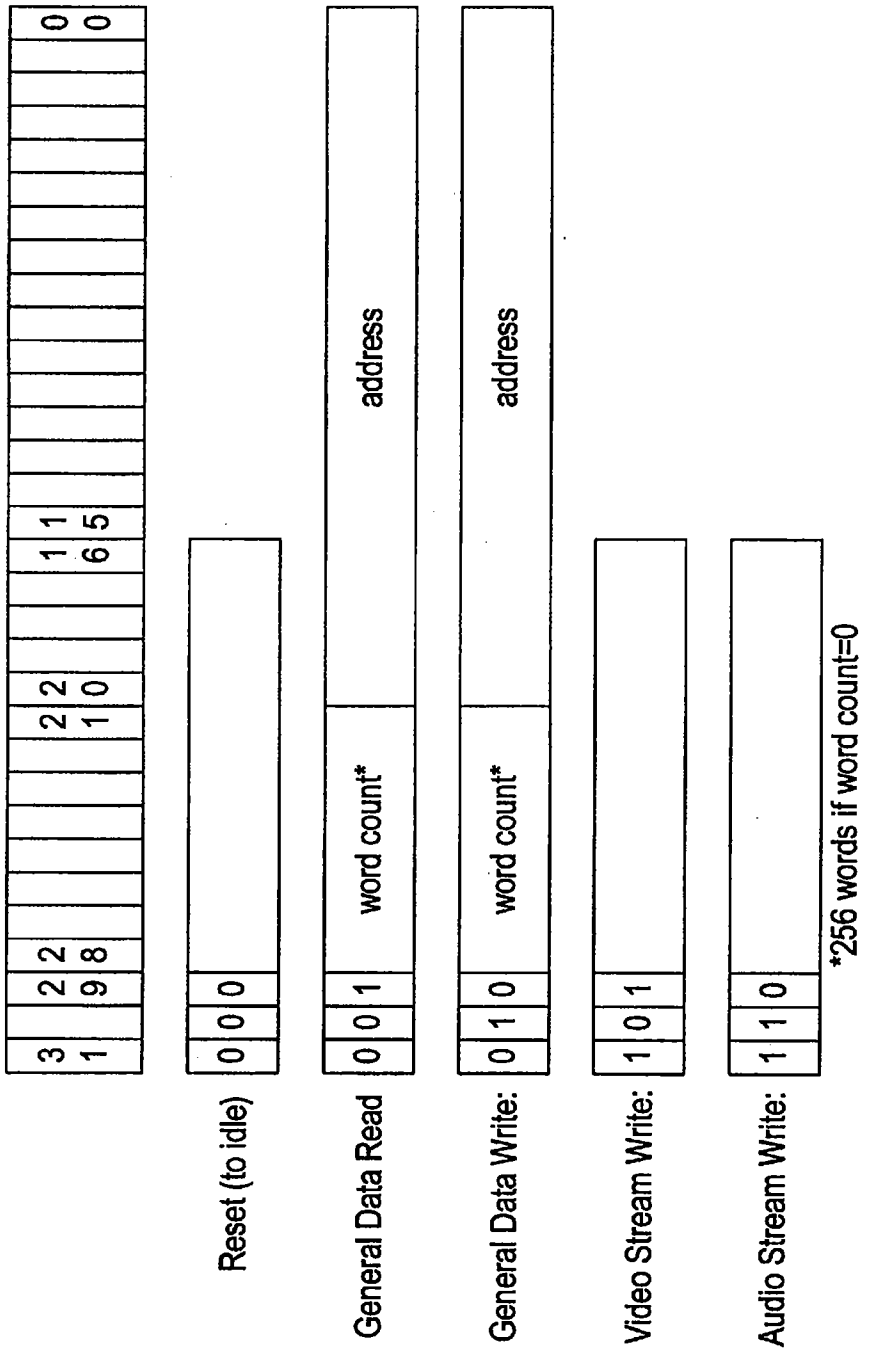

31 29 28 22 21 16 15 11 10 0
Reset (to idle)
0 0 0
General Data Read
0 0 1
word count*
address
General Data Write:
0 1 0
word count*
address
Video Stream Write:
1 0 1
Audio Stream Write:
1 1 0
*256 words if word count=0

FIG. 15

MPEG DECODER SYSTEM AND METHOD HAVING A UNIFIED MEMORY FOR TRANSPORT DECODE AND SYSTEM CONTROLLER FUNCTIONS

INCORPORATION BY REFERENCE

The following references are hereby incorporated by reference.

The ISO/IEC MPEG specification referred to as ISO/IEC 13818 is hereby incorporated by reference in its entirety.

U.S. patent application Ser. No. 08/654,321 titled "Method and Apparatus for Segmenting Memory to Reduce the Memory Required for Bidirectionally Predictive-Coded Frames" and filed May 28, 1996 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

U.S. patent application Ser. No. 08/653,845 titled "Method and Apparatus for Reducing the Memory Required for Decoding Bidirectionally Predictive-Coded Frames During Pull-Down" and filed May 28, 1996 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

U.S. patent application Ser. No. 08/689,300 titled "Method and Apparatus for Decoding B Frames in Video Codecs with Minimal Memory" and filed Aug. 8, 1996 now U.S. Pat. No. 5,818,533, whose inventors are David R. Auld and Kwok Chau, is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

1. Field of the Invention

The present invention relates generally to digital video compression, and more particularly to an MPEG decoder system which includes a single unified memory for MPEG transport, decode and system controller functions.

2. Description of the Related Art

Full-motion digital video requires a large amount of storage and data transfer bandwidth. Thus, video systems use various types of video compression algorithms to reduce the amount of necessary storage and transfer bandwidth. In general, different video compression methods exist for still graphic images and for full-motion video. Intraframe compression methods are used to compress data within a still image or single frame using spatial redundancies within the frame. Interframe compression methods are used to compress multiple frames, i.e., motion video, using the temporal redundancy between the frames. Interframe compression methods are used exclusively for motion video, either alone or in conjunction with intraframe compression methods.

Intraframe or still image compression techniques generally use frequency domain techniques, such as the discrete cosine transform (DCT). Intraframe compression typically uses the frequency characteristics of a picture frame to efficiently encode a frame and remove spatial redundancy. Examples of video data compression for still graphic images are JPEG (Joint Photographic Experts Group) compression and RLE (run-length encoding). JPEG compression is a group of related standards that provide either lossless (no image quality degradation) or lossy (imperceptible to severe degradation) compression. Although JPEG compression was originally designed for the compression of still images rather than video, JPEG compression is used in some motion video applications. The RLE compression method operates by testing for duplicated pixels in a single line of the bit map and storing the number of consecutive duplicate pixels rather than the data for the pixels themselves.

In contrast to compression algorithms for still images, most video compression algorithms are designed to compress full motion video. As mentioned above, video compression algorithms for motion video use a concept referred to as interframe compression to remove temporal redundancies between frames. Interframe compression involves storing only the differences between successive frames in the data file. Interframe compression stores the entire image of a key frame or reference frame, generally in a moderately compressed format. Successive frames are compared with the key frame, and only the differences between the key frame and the successive frames are stored. Periodically, such as when new scenes are displayed, new key frames are stored, and subsequent comparisons begin from this new reference point. It is noted that the interframe compression ratio may be kept constant while varying the video quality. Alternatively, interframe compression ratios may be content-dependent, i.e., if the video clip being compressed includes many abrupt scene transitions from one image to another, the compression is less efficient. Examples of video compression which use an interframe compression technique are MPEG, DVI and Indeo, among others.

MPEG BACKGROUND

A compression standard referred to as MPEG (Moving Pictures Experts Group) compression is a set of methods for compression and decompression of full motion video images which uses the interframe and intraframe compression techniques described above. MPEG compression uses both motion compensation and discrete cosine transform (DCT) processes, among others, and can yield compression ratios of more than 30:1.

The two predominant MPEG standards are referred to as MPEG-1 and MPEG-2. The MPEG-1 standard generally concerns frame data reduction using block-based motion compensation prediction (MCP), which generally uses temporal differential pulse code modulation (DPCM). The MPEG-2 standard is similar to the MPEG-1 standard, but includes extensions to cover a wider range of applications, including interlaced digital video such as high definition television (HDTV).

Interframe compression methods such as MPEG are based on the fact that, in most video sequences, the background remains relatively stable while action takes place in the foreground. The background may move, but large portions of successive frames in a video sequence are redundant. MPEG compression uses this inherent redundancy to encode or compress frames in the sequence.

An MPEG stream includes three types of pictures, referred to as the Intra (I) frame, the Predicted (P) frame, and the Bi-directional Interpolated (B) frame. The I or Intraframes contain the video data for the entire frame of video and are typically placed every 10 to 15 frames. Intraframes provide entry points into the file for random access, and are generally only moderately compressed. Predicted frames are encoded with reference to a past frame, i.e., a prior Intraframe or Predicted frame. Thus P frames only include changes relative to prior I or P frames. In general, Predicted frames receive a fairly high amount of compression and are used as references for future Predicted frames. Thus, both I and P frames are used as references for subsequent frames. Bi-directional pictures include the greatest amount of compression and require both a past and a future reference in order to be encoded. Bi-directional frames are never used as references for other frames.

In general, for the frame(s) following a reference frame, i.e., P and B frames that follow a reference I or P frame, only small portions of these frames are different from the corre-

sponding portions of the respective reference frame. Thus, for these frames, only the differences are captured, compressed and stored. The differences between these frames are typically generated using motion vector estimation logic, as discussed below.

When an MPEG encoder receives a video file, the MPEG encoder generally first creates the I frames. The MPEG encoder may compress the I frame using an intraframe compression technique. The MPEG encoder divides respective frames into a grid of 16×16 pixel squares called macroblocks in order to perform motion estimation/compensation. Thus, for a respective target picture or frame, i.e., a frame being encoded, the encoder searches for an exact, or near exact, match between the target picture macroblock and a block in a neighboring picture referred to as a search frame. For a target P frame the encoder searches in a prior I or P frame. For a target B frame, the encoder searches in a prior or subsequent I or P frame. When a match is found, the encoder transmits a vector movement code or motion vector. The vector movement code or motion vector only includes information on the difference between the search frame and the respective target picture. The blocks in target pictures that have no change relative to the block in the reference picture or I frame are ignored. Thus the amount of data that is actually stored for these frames is significantly reduced.

After motion vectors have been generated, the encoder then encodes the changes using spatial redundancy. Thus, after finding the changes in location of the macroblocks, the MPEG algorithm further calculates and encodes the difference between corresponding macroblocks. Encoding the difference is accomplished through a math process referred to as the discrete cosine transform or DCT. This process divides the macroblock into four sub blocks, seeking out changes in color and brightness. Human perception is more sensitive to brightness changes than color changes. Thus the MPEG algorithm devotes more effort to reducing color data than brightness.

Therefore, MPEG compression is based on two types of redundancies in video sequences, these being spatial, which is the redundancy in an individual frame, and temporal, which is the redundancy between consecutive frames. Spatial compression is achieved by considering the frequency characteristics of a picture frame. Each frame is divided into non-overlapping blocks, and each block is transformed via the discrete cosine transform (DCT). After the transformed blocks are converted to the "DCT domain", each entry in the transformed block is quantized with respect to a set of quantization tables. The quantization step for each entry can vary, taking into account the sensitivity of the human visual system (HVS)} to the frequency. Since the HVS is more sensitive to low frequencies, most of the high frequency entries are quantized to zero. In this step where the entries are quantized, information is lost and errors are introduced to the reconstructed image. Run length encoding is used to transmit the quantized values. To further enhance compression, the blocks are scanned in a zig-zag ordering that scans the lower frequency entries first, and the non-zero quantized values, along with the zero run lengths, are entropy encoded.

When an MPEG decoder receives an encoded stream, the MPEG decoder reverses the above operations. Thus the MPEG decoder performs inverse scanning to remove the zig zag ordering, inverse quantization to de-quantize the data, and the inverse DCT to convert the data from the frequency domain back to the pixel domain. The MPEG decoder also performs motion compensation using the transmitted motion vectors to recreate the temporally compressed frames.

When frames are received which are used as references for other frames, such as I or P frames, these frames are decoded and stored in memory. When a temporally compressed or encoded frame is received, such as a P or B frame, motion compensation is performed on the frame using the prior decoded I or P reference frames. The temporally compressed or encoded frame, referred to as a target frame, will include motion vectors which reference blocks in prior decoded I or P frames stored in the memory. The MPEG decoder examines the motion vector, determines the respective reference block in the reference frame, and accesses the reference block pointed to by the motion vector from the memory.

A typical MPEG decoder includes motion compensation logic which includes local or on-chip memory. The MPEG decoder also includes an external memory which stores prior decoded reference frames. The MPEG decoder accesses the reference frames or anchor frames stored in the external memory in order to reconstruct temporally compressed frames. The MPEG decoder also typically stores the frame being reconstructed in the external memory.

An MPEG decoder system also typically includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. An MPEG decoder system also generally includes a system controller which controls operations in the system and executes programs or applets.

Prior art MPEG video decoder systems have generally used a frame store memory for the MPEG decoder motion compensation logic which stores the reference frames or anchor frames as well as the frame being reconstructed. Prior art MPEG video decoder systems have also generally included a separate memory for the transport and system controller functions. It has generally not been possible to combine these memories, due to size limitations. For example, current memory devices are fabricated on an 4 Mbit granularity. In prior art systems, the memory requirements for the transport and system controller functions as well as the decoder motion compensation logic would exceed 16 Mbits of memory, thus requiring 20 or 24 Mbits of memory. This additional memory adds considerable cost to the system.

The amount of memory is a major cost item in the production of video decoders. Thus, it is desired to reduce the memory requirements of the decoder system as much as possible to reduce its size and cost. Since practical memory devices are implemented using particular convenient discrete sizes, it is important to stay within a particular size if possible for commercial reasons. For example, it is desired to keep the memory requirements below a particular size of memory, such as 16 Mb, since otherwise a memory device of 20 or 24 Mb would have to be used, resulting in greater cost and extraneous storage area. As mentioned above, it has heretofore not been possible to combine the memory required for the transport and system controller functions with the memory required for the MPEG decoder logic due to the memory size requirements.

Therefore, a new video decoder system and method is desired which efficiently uses memory and combines the memory subsystem for reduced memory requirements and hence reduced cost.

SUMMARY OF THE INVENTION

The present invention comprises an MPEG decoder system and method for performing video decoding or decompression which includes a unified memory for multiple

functions according to the present invention. The video decoding system includes transport logic, a system controller, and MPEG decoder logic. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport logic, system controller and MPEG decoder functions. The single unified memory is preferably a 16 Mbit memory. The present invention thus requires only a single memory, and thus has reduced memory requirements compared to prior art designs.

The video decoding system includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller which controls operations in the system and executes programs or applets. The video decoding system further includes decoding logic, preferably MPEG decoder logic, which performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The memory includes a plurality of memory portions, including a video frame portion for storing video frames, a system controller portion for storing code and data executable by the system controller, and a transport buffer for storing data used by the transport logic. The MPEG decoder logic preferably includes a memory controller which couples to the single unified memory. Each of the transport logic, system controller, and MPEG decoder logic accesses the single unified memory through the memory controller.

The video decoding system implements various frame memory saving schemes, such as compression or dynamic allocation, to reduce the required amount of frame store memory. Also, in one embodiment, the memory is not required to store reconstructed frame data during motion compensation, thus considerably reducing the required amount of memory for this function. Alternatively, the memory is only required to store a portion of the reconstructed frame data. These savings in memory allow portions of the memory to also be used for transport and system controller functions.

The present invention thus provides a video decoding system with reduced memory requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. **1** illustrates a computer system which performs video decoding and which includes a motion compensation logic having a frame memory which stores reference block data according to the present invention;

FIG. **2** is a block diagram illustrating the computer system of FIG. **1**;

FIG. **3** is a block diagram illustrating an MPEG decoder system including a unified memory for MPEG transport, system controller, and decode functions according to the present invention;

FIG. **4** is a block diagram illustrating the MPEG decoder logic in the system of FIG. **3**;

FIG. **5** illustrates various frame memory saving schemes used in various embodiments of the invention;

FIGS. **6***a* and **6***b* illustrate a table listing the memory partitions under different display schemes;

FIG. **7** illustrates the relationship of memory bandwidth vs. memory size in the NTSC decoding scheme;

FIG. **8** illustrates the relationship of memory bandwidth vs. memory size in the PAL encoding scheme;

FIG. **9** illustrates the memory partitions according to the preferred embodiment of the invention;

FIG. **10** illustrates the estimated memory bandwidth distribution in the preferred embodiment of the invention;

FIG. **11** illustrates the "worst case" relationship of processing power vs. memory size in the NTSC decoding scheme;

FIG. **12** illustrates the clock domains in the system;

FIG. **13** illustrates clock operating frequencies according to the preferred embodiment of the invention;

FIG. **14** illustrates an example of the packet data interface between the transport controller and the source decoder; and

FIG. **15** illustrates packet header formats used in the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Video Compression System

Referring now to FIG. **1**, a system for performing video decoding or decompression and including a unified memory according to the present invention is shown. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system.

As shown, in one embodiment the video decoding or decompression system is comprised in a general purpose computer system **60**. The video decoding system may comprise any of various types of systems, including a computer system, set-top box, television, or other device.

The computer system **60** is preferably coupled to a media storage unit **62** which stores digital video files which are to be decompressed or decoded by the computer system **60**. The media storage unit **62** may also store the resultant decoded or decompressed video file. In the preferred embodiment, the computer system **60** receives a compressed video file or bitstream and generates a normal uncompressed digital video file. In the present disclosure, the term "compressed video file" refers to a video file which has been compressed according to any of various video compression algorithms which use motion estimation techniques, including the MPEG standard, among others, and the term "uncompressed digital video file" refers to a stream of decoded or uncompressed video.

As shown, the computer system **60** preferably includes a video decoder **74** which performs video decoding or decompression operations. The video decoder **74** is preferably an MPEG decoder. The computer system **60** optionally may also include an MPEG encoder **76**. The MPEG decoder **74** and MPEG encoder **76** are preferably adapter cards coupled to a bus in the computer system, but are shown external to the computer system **60** for illustrative purposes. The computer system **60** also includes software, represented by floppy disks **72**, which may perform portions of the video decompression or decoding operation and/or may perform other operations, as desired.

The computer system **60** preferably includes various standard components, including one or more processors, one or more buses, a hard drive and memory. Referring now to FIG. **2**, a block diagram illustrating the components comprised in the computer system of FIG. **1** is shown. It is noted that FIG. **2** is illustrative only, and other computer architectures may be used, as desired. As shown, the computer

system includes at least one processor **80** coupled through chipset logic **82** to a system memory **84**. The chipset **82** preferably includes a PCI (Peripheral Component Interconnect) bridge for interfacing to PCI bus **86**, or another type of bus bridge for interfacing to another type of expansion bus. In FIG. **2**, MPEG decoder **74** and MPEG encoder **76** are shown connected to PCI bus **86**. Various other components may be comprised in the computer system, such as video **88** and hard drive **90**.

As mentioned above, in the preferred embodiment of FIG. **1** the computer system **60** includes or is coupled to one or more digital storage or media storage devices. For example, in the embodiment of FIG. **1**, the computer system **60** couples to media storage unit **62** through cable **64**. The media storage unit **62** preferably comprises a RAID (Redundant Array of Inexpensive Disks) disk array, or includes one or more CD-ROM drives and/or one or more Digital Video Disk (DVD) storage units, or other media, for storing digital video to be decompressed and/or for storing the resultant decoded video data. The computer system may also include one or more internal RAID arrays, CD-ROM drives and/or may couple to one or more separate Digital Video Disk (DVD) storage units. The computer system **60** also may connect to other types of digital or analog storage devices or media, as desired.

Alternatively, the compressed digital video file may be received from an external source, such as a remote storage device or remote computer system. In this embodiment, the computer system preferably includes an input device, such as an ATM (Asynchronous Transfer Mode) adapter card or an ISDN (Integrated Services Digital Network) terminal adapter, or other digital data receiver, for receiving the digital video file. The digital video file may also be stored or received in analog format and converted to digital data, either externally to the computer system **60** or within the computer system **60**.

As mentioned above, the MPEG decoder **74** in the computer system **60** performs video decoding or video decompression functions. As discussed further below, the video decoding system includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller which controls operations in the system and executes programs or applets comprised in the stream. The video decoding system further includes decoding logic, preferably MPEG decoder logic, which performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system. The MPEG decoder **74** thus performs functions with improved efficiency and reduced memory requirements according to the present invention.

It is noted that the system for decoding or decompressing video data may comprise two or more interconnected computers, as desired. The system for decoding or decompressing video data may also comprise other hardware, such as a set top box, either alone or used in conjunction with a general purpose programmable computer. It is noted that any of various types of systems may be used for decoding or decompressing video data according to the present invention, as desired.

FIG. **3**—MPEG Decoder Block Diagram

Referring now to FIG. **3**, a block diagram illustrating an MPEG decoder system architecture according to one embodiment of the present invention is shown. As shown, the MPEG decoder system includes a channel receiver **202** for receiving a coded stream. As mentioned above, in the preferred embodiment, the coded stream is an MPEG encoded stream. The MPEG encoded stream may include interactive program content comprised within this stream, as desired. The channel receiver **202** receives the coded stream and provides the coded stream to a transport and system controller block **204**.

The transport and system controller block **204** includes transport logic **206** which operates to demultiplex the received MPEG encoded stream into a plurality of multimedia data streams. In other words, the encoded stream preferably includes a plurality of multiplexed encoded channels or multimedia data streams which are combined into a single stream, such as a broadcast signal provided from a broadcast network. The transport logic **206** in the transport and system controller block **204** operates to demultiplex this multiplexed stream into one or more programs, wherein each of the programs comprise individual multimedia data streams including video and/or audio components.

It is noted that the MPEG stream may comprise one of two types of streams including either a transport stream or a program stream. A transport stream comprises a 188 byte stream which includes error correction and which is designed for an error prone environment. A program stream, on the other hand, is designed for an error free environment and this does not include error correction capabilities.

The transport and system controller block **204** also includes a system controller **208** which monitors the MPEG system and is programmable to display audio/graphics on the screen and/or execute interactive applets or programs which are embedded in the MPEG stream. The system controller **208** also preferably controls operations in the MPEG decoder system. In the preferred embodiment, the system controller **208** comprises a MIPS RISC CPU which is programmed to perform system controller functions.

The transport and system controller block **204** couples through a memory controller **211** in MPEG decoder **224** to an external memory **212**, also referred to as the single unified memory **212**. The transport logic **206** and system controller logic **208** comprised in the transport and system controller block **204** utilize the external memory **212** to store and/or receive code and data. In the preferred embodiment, the external memory **212** is a 16 MB synchronous dynamic random access memory (SDRAM).

As shown, the transport and system controller block **204** couples to an MPEG decoder block **222**. The MPEG decoder block **222** includes an MPEG audio visual decoder **224**, as shown. The MPEG audio visual decoder **224** receives data from the transport and system controller block **204** and operates to perform MPEG decoding to produce a decoded or decompressed signal. The visual component of the decompressed signal is output from the MPEG A/V decoder **224** and is provided to a video encoder **226**. The video encoder **226** operates to convert the digital video stream into a format more appropriate for transmission or display, such as NTSC or PAL format. The video encoder logic **226** includes digital to analog (D/A) converters for converting the decoded digital video stream into an analog stream. This analog video stream is then provided as an output of the system as shown.

The audio component of the decoded or decompressed MPEG stream is provided to an audio digital to analog converter (DAC) **228**. The audio DAC **228** operates to perform digital to analog conversion on the digital audio signal output from the MPEG A/V decoder **224**. The result-

ing analog audio signals are provided as an output to the system as shown.

As shown, the external memory **212** is coupled to the MPEG A/V decoder **224**. The MPEG A/V decoder **224** includes a memory controller **211** which controls access to the single unified memory **212**. As noted above, each of the transport logic **206** and system controller logic **208** comprised in the transport and system controller block **204** access the external memory **212** through the memory controller **211**.

The MPEG A/V decoder **224** utilizes the external memory **212** in the MPEG decode process. Thus the MPEG A/V decoder **224** uses the same memory **212** as the transport and system controller blocks. As is well-known in the art, the MPEG A/V decoder **224** uses the external memory **212** to store decoded reference frames or anchor frames which are used during motion compensation or reconstruction of temporally compressed frames. The MPEG A/V decoder **224** may also use the external memory **212** to store a portion or all of the reconstructed frames.

Reconstructed Frame Data Memory Saving Schemes

It is noted that reconstruction of a temporally compressed frame during MPEG decoding typically uses a full 16 MB of external memory. However, the MPEG decoder system **74** of the preferred embodiment uses one or more of various methods to reduce the amount of memory required for storing reconstructed frame data. For example, current prior art video decoder implementations use at least one frame of memory to store the reconstructed B-picture prior to display. In other words, prior art decoders require that there be a full frame store into which to reconstruct the B frame or picture.

In one embodiment of the invention, the video decoder system **74** uses as little as 2.528 frame stores when there is no pulldown during B-frames. In this embodiment, the system uses an improved method to reduce the required amount of memory, whereby the memory used to store the first field is used again for reconstruction as soon as that part of the picture has been displayed. This method reduces the amount of memory needed for B-frame reconstruction to about 0.528 frames. For more information on this method, please see U.S. patent application Ser. No. 08/654,321 titled "Method and Apparatus for Segmenting Memory to Reduce the Memory Required for Bidirectionally Predictive-Coded Frames" and filed May 27, 1996, which is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

In another embodiment of the invention, the video decoder system **74** uses as little as 2.75 frames when there is pulldown. In this embodiment, a method is used to reduce the memory required for decoding and displaying B frames during 3:2 pull-down. This method uses the fact that B frames are not used to predict other frames, so that once the B frame data is retrieved for display, it may be discarded. To enable re-use of memory, data from the top and bottom fields is separated into different segments of memory. Thus, once retrieval begins of the data in a segment, that segment becomes free for reconstruction. However, this initial scheme is not completely sufficient for the top field of every other frame during 3:2 pull-down, since the top field must be somehow made available again for re-display. Rather than requiring additional memory to save the top field of every other frame, the top field is reconstructed again during the period when reconstruction is typically stalled. In this manner, the amount of memory required is reduced, and the field requiring re-display for 3:2 pull-down is simply reconstructed again. For more information on this method for reducing the required amount of memory when pull-down is being performed, please see U.S. patent application Ser. No. 08/653,845 titled "Method and Apparatus for Reducing the Memory Required for Decoding Bidirectionally Predictive-Coded Frames During Pull-Down" and filed May 27, 1996, which is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

The above methods used to reduce memory requirements, which are disclosed in the above-referenced patent applications, are optimal, i.e., use the least possible memory, where the picture is decoded only once. In another embodiment, The MPEG decoder **74** includes frame reconstruction or decoder logic which operates to reconstruct a bi-directionally encoded (B) frame without requiring storage of the frame being constructed in the external memory **112**. In this embodiment, the MPEG decoder **74** operates to decode or reconstruct the frame twice, once during each field display period. This obviates the necessity of storing the reconstructed B frame data, thus reducing memory requirements.

In this embodiment, the MPEG decoder system includes a picture reconstruction unit, a picture display unit, a pointer register, and a temporary buffer (all not shown). The picture memory **212** includes separate buffers used for anchor pictures or reference frames (A1, A2) and a rate buffer which stores the temporally compressed frame, referred to as C. The pointer register stores the location of the first byte of the compressed picture, which is stored in the rate buffer. According to this embodiment, the picture memory **212** is not required to store data from the reconstructed frame.

The picture reconstruction unit operates to decode or reconstruct the B frame twice, once each during a first field time and a second field time. The first field time substantially corresponds to the time when the first or top field of the picture is displayed, and the second field time substantially corresponds to the time when the second or bottom field of the picture is displayed.

During the first field time, compressed picture data is read from the rate buffer into the picture reconstruction unit, where the picture is decoded. The top field data from the picture reconstruction unit is written to the temporary buffer, and the bottom field data is discarded. After one slice of the picture has been decoded, the data in the temporary buffer is retrieved by the picture display unit and is output for display. This process continues for the entire picture in order to display all of the first field. Thus, the entire picture is decoded or reconstructed, and only data from the top field is written to the temporary buffer for display.

During the second field time, the same compressed picture is again read from the rate buffer. The picture reconstruction unit again decodes the compressed picture. In the second field time, the picture reconstruction unit writes the bottom field data to the temporary buffer, and the top field data is discarded. After one slice of the picture has been decoded, the data in the temporary buffer is output by the picture display unit for display. This process continues for the entire picture in order to display all of the second field.

The reconstructed picture is never written to the memory during reconstruction of B-frames. It is also noted that the temporary buffer is about 32 times smaller than the external frame store required in the best implementation of prior art methods. This allows the temporary buffer to be comprised on the same monolithic substrate as the decoder itself.

Therefore, in this embodiment the video decoder system reconstructs the B-picture twice, once in each field time. This eliminates the storage requirement of the reconstructed B-frame entirely and thus allows this memory space to be used for transport and system controller functions.

In another embodiment, the MPEG decoder system of the preferred embodiment uses a dynamic segment allocation scheme and/or compression techniques which reduce the external memory requirement. These memory saving techniques are discussed further below.

Therefore, the video decoding system **74** includes transport logic **206** which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller **208** which controls operations in the system and executes programs or applets comprised in the stream. The video decoding system **74** further includes decoding logic **224**, preferably MPEG decoder logic, performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system.

As discussed above, prior art MPEG decoder systems include different memory systems for the transport and system controller logic **204** and the MPEG decoder logic **224**. These separate memories are required because of the separate bandwidth and processing requirements for each memory, as well as the memory size requirements of each block. According to the system and method of the present invention, the present invention includes a single or unified memory which is used for each of the transport and system controller block **204** and the MPEG A/V decoder logic **224**.

FIG. **4**—MPEG Decoder Block Diagram

Referring now to FIG. **4**, a block diagram illustrating the MPEG A/V decoder logic **224** in the MPEG decoder **74** which performs motion compensation according to the present invention is shown. As shown, the video decoder logic **224** receives an encoded or compressed digital video stream and outputs an uncompressed digital video stream. The compressed digital video stream is a bitstream of compressed video data which is used to present a video sequence, such as a television segment or movie, onto a screen, such as a television or a computer system. In the preferred embodiment, the compressed digital video stream is compressed using the MPEG-2 compression algorithm, and the video decoder **74** is thus preferably an MPEG-2 decoder. Since the operation of MPEG decoders is well known in the art, details of their operation which are not necessary to the operation of the present invention are omitted for simplicity.

As shown in FIG. **3**, the decoder logic **224** comprises a Variable Length Decoding block **302** coupled to provide an output to an Inverse Scan block **304**, which is coupled to provide an output to an Inverse Quantization block **306**, which is coupled to provide an output to an Inverse DCT block **308**, which is coupled to provide an output to a motion compensation block **310**. The motion compensation block **310** provides an output comprising decoded samples. A frame store memory **212** is coupled to the output of the motion compensation block **310** to receive and store decoded frame data. The motion compensation block **310** is coupled to an output of the frame store memory **212** to receive reference block data from the frame store memory **212** during motion compensation.

As shown in FIG. **3**, the Variable Length Decoding block **302** receives coded data and performs variable length decoding. As is well known, the MPEG standard provides that data is compressed for transmission using variable length codes. Thus the Variable Length Decoding block **302** decodes this data and produces an output, referred to as QFS[n]. The QFS[n]output of the Variable Length Decoding block **302** is provided to the Inverse Scan block **304**. The Inverse Scan block **304** reverses the zig zag scan ordering of the received data (is this right) and produces an output referred to as QF[v][u]. The output QF[v][u] is provided to the Inverse Quantization block **306**. The Inverse Quantization block **306** performs inverse quantization or de-quantizes the data to produce de-quantized data, referred to as F[v][u]. The output F[v][u] of the Inverse Quantization block **306** is provided to the Inverse DCT block **308**, which performs the inverse discrete cosine transform to convert the data from the frequency domain back to the pixel domain. The inverse DCT block **308** produces an output referred to as f[y][x]. The output f[y][x] of the inverse DCT block **308** is provided to the motion compensation block **310**.

The output f[y][x] from the inverse DCT block **308** comprises temporally encoded frames of pixel data. The motion compensation block **310** decompresses the temporally compressed frames using motion compensation techniques. As described above, an MPEG encoded stream comprises I, P and B frames. P and B frames are temporally compressed relative to other frames. P frames are temporally compressed relative to prior I or P frames, and B frames are temporally compressed relative to prior or subsequent I or P frames. When a frame is temporally compressed, the frame is partitioned into macroblocks, referred to as target blocks, and then the compression method searches in neighboring frames for blocks which are most similar to the block being encoded. When the best fit block is found, the respective target block is encoded by a motion vector which points to this best fit reference block in the reference frame. The difference between the block being encoded and the best fit block is also computed and transferred in the MPEG stream.

Output pixel values from the motion compensation block **310** are provided to a frame store memory **212**. The frame store memory **212** is thus coupled to the motion compensation block **310** and stores one or more reference frames of video data. These reference frames of video data are used in performing motion compensation on temporally compressed frames, such as P and B frames. In general, an MPEG stream includes encoded reference frame data which is transmitted before temporally compressed data that depends on the prior transmitted reference frame data. Thus, incoming temporally encoded frame data, such as P and B frame data, comprises motion vectors which point to reference blocks in a prior transmitted reference frame of video data, which has been stored in the frame store memory **212**. The motion compensation block **310** analyzes each motion vector from the incoming temporally compressed data and retrieves a reference block from the frame store memory **212** in response to each motion vector. The motion compensation block **310** includes a local memory or on-chip memory **116** which stores the retrieved reference block. The motion compensation block **110** then uses this retrieved reference block to decompress the temporally compressed data.

In the preferred embodiment, the frame store memory **212** is 1M×16 SDRAM, such as Samsung KM416S1120AT-12, having an operating frequency of 81 MHz or 108 MHz and a burst size of **4** words. As discussed above, the frame store memory **112** is also used according to the present invention to store code and data for the transport logic **206** and the system controller logic **208**.

FIG. **5**—Memory Saving Schemes

FIG. **5** illustrates various frame memory saving schemes used in various embodiments of the invention. As shown, in European systems which do not include a field repeat,

dynamic memory segment allocation techniques are used to more efficiently use the memory space. In other words, memory segments or areas are dynamically allocated to minimize unused space. These dynamic memory segment allocation techniques range from a 40 segment technique (×/2.556) to a 3.22 (3) segment technique (×/2.801). As the memory segment size decreases, a larger amount of granularity is provided, and the memory can be used in a more "detailed" or specific fashion. The dynamic allocation scheme operates to dynamically allocate segments of memory of different size to more efficiently use the available memory and correspondingly result in little or no un-used space.

In U.S. systems with field repeat, compression techniques are preferably used to reduce memory requirements. These compression techniques include a "compressed bitstream" technique and a "local compression" technique.

The compressed bitstream technique operates to store frame data in its received MPEG compressed format, instead of storing the frame data in a decoded or decompressed format. When this compressed data is read from memory, the compressed memory is decoded or decompressed "on the fly". As shown, the compressed bitstream technique may involve storing only one of the anchor frames in a compressed format, storing only the B frames in a compressed format, or storing both the anchor and B frames in a compressed format.

The local compression technique comprises re-encoding the decoded or compressed bitstream, preferably using a standard compression standard such as DPCM or MPEG. Thus, once frames have been decoded or reconstructed, the frame data is re-encoded prior to storage in memory. As shown, the local compression may involve compressing one of the anchor frames only, the B frames only, or both the anchor and B frames.

FIGS. 6*a* and 6*b*—Memory Partitions

FIGS. 6A and 6B illustrate a table listing the memory partitions under different memory reduction schemes. As shown, the table of FIG. 1 illustrates the memory requirements for both the NTSC and PAL decoding schemes for a standard LSI L64005 part, a method which compresses the displayed anchor frame, a method which compresses both the anchor and the segment storing the B frame, a method which compresses only the B frame, and a method which compresses both the anchor and entire B frame. LSI part no. L64005 is a device produced by LSI Logic that has no memory reduction for NTSC and has dynamic allocation for PAL.

As shown, in the NTSC format using LSI part No. L64005, the frame store memory requires 12,441,600 bits of memory for storing three full frames. The channel buffer requires 2,864,637 bits of memory for various functions. As shown in the table, these functions include the vbv (video buffer verifier) buffer, the video non-instantaneous decode function, the video display sync function, the audio buffer, the audio-video latency difference function, the audio-display sync function, the video transport buffer, the audio transport buffer, and the jitter buffer (4 ms jitter at 15 Mbps). Each of the above functions collectively requires 2,864,637 bits for the channel buffer. The packet header overhead requires 20,000 bits of memory, the on-screen display (OSD) requires 675,840 bits of memory. This provides a subtotal for the software and data storage of 775,139 bits. The total required storage for the NTSC format is 16,777,216 bits of memory. As shown, the frame store and channel buffer collectively require 15,306,237 bits of memory.

As shown, the PAL decoding scheme using L64005 is similar. As shown the PAL decoding scheme requires 12,718,080 bits of memory to store 2.556 frames of memory. The channel buffer's subtotal for the PAL decoding scheme requires 3,060,847 bits of memory. The packet header overhead for the pal scheme is also 20,000 bits, and the onscreen display requires 808,192 bits. The subtotal for software and data storage in the PAL decoding scheme is 170,097 bits. Thus, the PAL decoding scheme using L64005 requires a total of 16,777,216 bits. As shown, for the PAL format, the frame store and channel buffer collectively require 15,778,927 bits of memory.

As shown, when the displayed anchor is compressed, the NTSC format requires 9,538,560 bits for the frame store, which is required to store the equivalent of 2.3 frames. The total for the frame store and channel buffer requirements is 14,208,205 bits, as well as 1,873,171 bits for the software and data. For the PAL decoding scheme with a compressed display anchor, 11,197,440 bits are required for the frame store. The frame store and channel buffer collectively require 16,063,295 bits, and the software and data requirement is (114,271). Thus, there are 114,271 bits "over budget" over a 16 Mbit target.

Where the anchor and the B segment are both compressed, for the NTSC decoding scheme, assuming 3.267 segments, the frame store is reduced to 8,778,240 bits and is required to store only 2.117 frames. Under this method, the frame store and channel buffer collectively require 13,447,885 bits of memory, and the subtotal for the software and data requirement is 2,633,491 bits of memory. In the PAL decoding scheme where the method compresses an anchor and segment B, assuming 40 segments, the frame store requires 8,985,600 bits and requires 1.806 frames to be stored. This method requires 13,851,455 bits to collectively store the frame store and channel buffer data, and the subtotal for software and data storage is 2,097,569 bits.

When the memory compresses only the B frame to optimize memory storage, in the NTSC format, the frame store required is 8,570,880 bits of memory and stores an equivalent of 2.067 frames. Under this method, the frame store and channel buffer require a total of 11,435,517 bits and a subtotal for software and data storage of 4,645,859 bits. In the PAL decoding scheme where the B frame only is compressed, the frame store requires 10,229,760 bits and thus stores 2.056 equivalent number of frames. In this method, the frames store and channel buffer collectively require 13,290,607 bits of memory, and the subtotal for software and data storage requires 2,658,417 bits of memory.

Where the system compresses both the anchor and the B frame to optimize memory, in the NTSC format, the frame store required is 5,667,840 bits of memory and stores an equivalent of 1.367 frames. Under this method, the frame store and channel buffer require a total of 10,337,485 bits and a subtotal for software and data storage of 5,743,891 bits. In the PAL decoding scheme where both the anchor frame and B frame are compressed, the frame store requires 6,497,280 bits and thus stores 1.306 equivalent number of frames. In this method, the frames store and channel buffer collectively require 11,363,135 bits of memory, and the subtotal for software and data storage requires 4,585,889 bits of memory.

FIG. 7—Memory Bandwidth vs. Memory Size in the NTSC Decoding Scheme

FIG. 7 illustrates the relationship of memory bandwidth vs. memory size in the NTSC decoding scheme. The memory size on the x axis of the graph is the memory size required for the frame store memory and the channel buffer. As shown, as the memory size decreases from left to right,

the required amount of memory and/or processing bandwidth increases. Thus, a greater amount of memory transfer and/or processing bandwidth is required as the memory size is reduced. FIG. **7** illustrates four different plots for each memory size, where these plots comprise 100%, 96%, and 87%, and 72% of useable bandwidth. The various lines illustrated in the graph of FIG. **7** illustrate the change in bandwidth versus the change in memory size, i.e., the Δbandwidth/Δmemory, which comprises the units bytes/second/bit. As shown, the optimum memory size in the NTSC format is 13,447,885 bits.

FIG. **8**—Memory Bandwidth vs. Memory Size in the NTSC Decoding Scheme

FIG. **8** illustrates the relationship of memory bandwidth vs. memory size in the PAL decoding scheme. As with FIG. **7**, the memory size on the x axis of the graph is the memory size required for the frame store memory and the channel buffer. As shown, as the memory size decreases from left to right, the required amount of memory and/or processing bandwidth increases. Thus, a greater amount of memory transfer and/or processing bandwidth is required as the memory size is reduced. FIG. **8** also illustrates four different plots for each memory size, where these plots comprise 100%, 96%, and 87%, and 72% of useable bandwidth. The various lines illustrated in the graph of FIG. **8** illustrate the change in bandwidth versus the change in memory size, i.e., the Δbandwidth /Δmemory, which comprises the units bytes/second/bit. As shown, the Δbandwidth/ Δmemory peaks at 13,851,455 bits, which is the optimum memory size in the PAL format.

FIG. **9**—Memory Partitions

FIG. **9** illustrates the memory partitions of the external memory **212** for each of the NTSC and PAL encoding formats according to one embodiment of the invention. FIG. **9** illustrates the number of bytes of memory size allocated for different purposes in the unified memory **212**, including number of bits for video frames, the vbv buffer, the video decode buffer, the video-display synch buffer, the audio buffer, the audio-video latency buffer, the audio-display synch buffer, the transport buffer, the jitter buffer, the PES header overhead memory, the OSD, and the system controller code and data storage. It is noted that FIG. **9** illustrates the memory partition according to one embodiment of the invention, and it is noted that the memory **212** may be allocated differently, as desired. As shown, the memory size requirement are substantially comparable. In this example, the NTSC format uses 10,583,248 bytes for storing video frames, and the PAL format uses 10,790,608 bytes for storing video frames.

FIG. **10**—Decoding Memory Bandwidth

FIG. **10** illustrates the estimated memory bandwidth distribution in the preferred embodiment of the invention for the NTSC and PAL formats. FIG. **10** illustrates the estimated memory bandwidth distribution using the memory partition embodiment of FIG. **9**. The estimated memory bandwidth distribution shown in FIG. **10** presumes a 16×1 MB SDRAM running at 100 MHz, wherein bandwidth is available at 200 MB per second. This memory bandwidth distribution also presumes a requirement of 20 Mbytes per second for code and data executed by the system controller **208** in the transport and system controller block **204**. As noted above, the system controller **208** is preferably a MIPS RISC CPU. As shown, the NTSC scheme requires 160.19 MB per second bandwidth, whereas the PAL decoding scheme requires 157.18 MB per second of bandwidth. The bandwidth requirements for each of the NTSC and PAL formats are substantially comparable with the exception that the NTSC format requires a greater amount of memory bandwidth for the channel in/out function than does the PAL format.

FIG. **11**—Processing Power vs. Memory Size (NTSC)

FIG. **11** illustrates the "worst case" relationship of processing power vs. memory size in the NTSC decoding scheme. In FIG. **11**, the lines represent available cycles per macroblock for a decoder operating at 27 to 216 MHz. The bars represent the required cycles per macroblock reconstructed for 1 to 4 cycle/coefficient throughput. For example, a 100 MHz decoder can operate with 13,447,885 memory points at 1 and 2-cycle/coefficient throughput only (not the slow 4-cycle/coefficient). However, as shown, the processing power tends to increase as the memory decreases in size from 13,447,885 bytes to 11,435,517 bytes. The 11,435,517 and 19,337,485 memory points require a large amount of processing power, and thus even 216 MHz processing speed is not sufficient with 2-cycle/coefficient throughput.

FIGS. **12** and **13**—Clock Domains

FIG. **12** illustrates the clock domains in the system, i.e., the various possible clock rates for the external memory **212** according to one embodiment of the invention. The video decoder system in the preferred embodiment includes a source decoder which operates at 27 Megahertz. The source decoder clock frequency of 27 Megahertz is required according to modern video encoding schemes. However, current memory operating frequencies are not designed for video applications, i.e., are not designed to operate at multiples of 27 MHz. As shown, the memory **212** operates near multiples of this source decoder frequency such as 50 MHz or 100 MHz.

FIG. **13** illustrates clock operating frequencies according to the preferred embodiment of the invention. In this embodiment, the external memory **212** is SDRAM or other suitable memory operating at 108 MHz, or a higher multiple. As shown, the transport and system controller block **204** preferably operates at either 54 MHz or 108 MHz. The source decoder **224** preferably also operates at 54 MHz or 108 MHz. Thus, as shown in FIG. **13**, in the preferred embodiment the memory and hardware elements operate at multiples of the 27 MHz required clock frequency, i.e., either 54 Megahertz or 108 Megahertz.

FIG. **14**—Packet Data Interface

FIG. **14** illustrates an example of the packet data interface between the transport and system controller block **204** and the source decoder **224**. As shown, the transport and system controller block **204** and the source decoder **224** communicate 16 bit transmission data, referred to as TD[**15:0**], in a bi-directional manner. The transmission data signals TD[**15:0**] comprise a data bus for transmitting data between the transport and system control logic **204** and the source decoder **224**. The transport and system controller block **204** provides a transmission data output enable (TDOE) signal which is provided as an input to the source decoder **224**. The transport and system controller block **204** also provides a new packet word (NPW) signal as an input to the source decoder **224**. The source decoder **224** provides two outputs to the transport and system controller block **204**, these being a data chain hold (DCH) signal, which is a wait cycle request, and a TRDY (transmission ready) signal which indicates that the logic is ready for a new packet.

FIG. **15**—Packet Header Formats

FIG. **15** illustrates packet header formats used in the preferred embodiment. As shown, different packet header values are used to indicate a reset, a general data read, a general data write, a video stream write, and an audio stream write. The general data read and general data write packets each include fields for word count and address.

Conclusion

Therefore, the present invention comprises a video decoder system and method which includes a single unified memory for MPEG transport, decode, and system controller functions. This reduces the required amount of memory, thus simplifying system design and reducing system cost.

Although the system and method of the present invention has been described in connection with the described embodiments, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention as defined by the appended claims.

I claim:

1. An MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:

a channel receiver for receiving and MPEG encoded stream;

transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream;

a system controller coupled to the transport logic which controls operations within the MPEG decoder system;

an MPEG decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the MPEG decoder operates to perform MPEG decoding on the multimedia data streams; and

a memory coupled to the MPEG decoder, wherein the memory is used by the MPEG decoder during MPEG decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the MPEG decoder system, wherein the memory is used by the transport logic for demultiplexing operations;

wherein the MPEG decoder is operable to access the memory during MPEG decoding operations;

wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and

wherein the system controller is operable to access the memory to retrieve code and data during system control functions.

2. The MPEG decoder system of claim 1, wherein the MPEG decoder includes a memory controller coupled to the memory;

wherein the transport logic is coupled to the memory controller and is operable to access the memory through the memory controller; and

wherein the system controller is coupled to the memory controller and is operable to access the memory through the memory controller.

3. The MPEG decoder system of claim 2, wherein the memory controller is operable to store compressed data in the memory to reduce memory storage requirements.

4. The MPEG decoder system of claim 2, wherein the memory controller is operable to dynamically allocate segments of memory space in the memory to optimize memory use.

5. The MPEG decoder system of claim 1, wherein the memory stores anchor frame data during reconstruction of temporally compressed frames.

6. The MPEG decoder system of claim 1, wherein said memory has a memory size which does not exceed 16 Mbit.

7. The MPEG decoder system of claim 1, wherein said memory includes a plurality of memory portions, wherein said memory includes a video frame portion for storing video frames, a system controller portion for storing code and data executable by the system controller, and a transport buffer portion for storing data used by the transport logic.

8. The MPEG decoder system of claim 7, wherein said memory further includes a video decode buffer portion for storing decoded video data, a video display sync buffer, and an on-screen display buffer.

9. The MPEG decoder system of claim 8, wherein said memory further includes one or more audio buffers for storing audio data.

10. A method for performing video decoding in an MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, the method comprising:

receiving an MPEG encoded stream;

demultiplexing one or more multimedia data streams from the encoded stream, wherein said demultiplexing one or more multimedia data streams from the encoded stream operates using a first unified memory;

performing MPEG decoding on the multimedia data streams, wherein said performing MPEG decoding operates using said first unified memory; and

a system controller controlling operations within the MPEG decoder system, wherein said controlling operations accesses code and data from said first unified memory;

wherein said demultiplexing one or more multimedia data streams, said performing MPEG decoding, and said controlling operations each use said first unified memory.

11. The method of claim 10,

wherein said demultiplexing one or more multimedia data streams from the encoded stream includes accessing multimedia data stream data from said first unified memory;

wherein said performing MPEG decoding on the multimedia data streams includes accessing video frame data from said first unified memory; and

wherein said controlling operations includes accessing code and data from said first unified memory.

12. The method of claim 11, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory;

wherein said accessing multimedia data stream data from said first unified memory comprises accessing said multimedia data stream data through the memory controller;

wherein said accessing video frame data from said first unified memory comprises accessing said video frame data through the memory controller; and

wherein said accessing code and data from said first unified memory comprises accessing said code and data through the memory controller.

13. The method of claim 10, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory, the method further comprising:

the memory controller storing compressed data in the first unified memory to reduce memory storage requirements.

14. The method of claim 10, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory, the method further comprising:

the memory controller dynamically allocating segments of memory space in the first unified memory to optimize memory use.

15. The method of claim **10**, wherein said first unified memory has a memory size which does not exceed 16 Mbit.

16. A video decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:

a channel receiver for receiving an encoded video stream;

transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream;

a system controller coupled to the transport logic which controls operations within the video decoder system;

a video decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the video decoder operates to perform video decoding on the multimedia data streams; and

a memory coupled to the video decoder, wherein the memory is used by the video decoder during video decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the video decoder system, wherein the memory is used by the transport logic for demultiplexing operations;

wherein the video decoder is operable to access the memory during video decoding operations;

wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and

wherein the system controller is operable to access the memory to retrieve code and data during system control functions.

17. The video decoder system of claim **16**, wherein the video decoder includes a memory controller coupled to the memory;

wherein the transport logic is coupled to the memory controller and is operable to access the memory through the memory controller; and

wherein the system controller is coupled to the memory controller and is operable to access the memory through the memory controller.

18. The video decoder system of claim **17**, wherein the memory controller is operable to store compressed data in the memory to reduce memory storage requirements.

19. The video decoder system of claim **17**, wherein the memory controller is operable to dynamically allocate segments of memory space in the memory to optimize memory use.

20. The video decoder system of claim **16**, wherein said memory has a memory size which does not exceed 16 Mbit.

* * * * *

EXHIBIT B

US006982663B2

(12) **United States Patent**
Winger

(10) **Patent No.: US 6,982,663 B2**
(45) **Date of Patent: Jan. 3, 2006**

(54) **METHOD AND SYSTEM FOR SYMBOL BINARIZATION**

(75) Inventor: **Lowell Winger**, Waterloo (CA)

(73) Assignee: **LSI Logic Corporation**, Milpitas, CA (US)

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(21) Appl. No.: **10/770,213**

(22) Filed: **Feb. 2, 2004**

(65) **Prior Publication Data**

US 2004/0150540 A1 Aug. 5, 2004

Related U.S. Application Data

(63) Continuation of application No. 10/191,596, filed on Jul. 10, 2002, now Pat. No. 6,744,387.

(51) **Int. Cl.**
H03M 7/00 (2006.01)

(52) **U.S. Cl.** **341/107**

(58) **Field of Classification Search** 341/50, 341/51, 107, 106; 704/221, 222, 201, 204, 704/503, 500, 200, 211, 236
See application file for complete search history.

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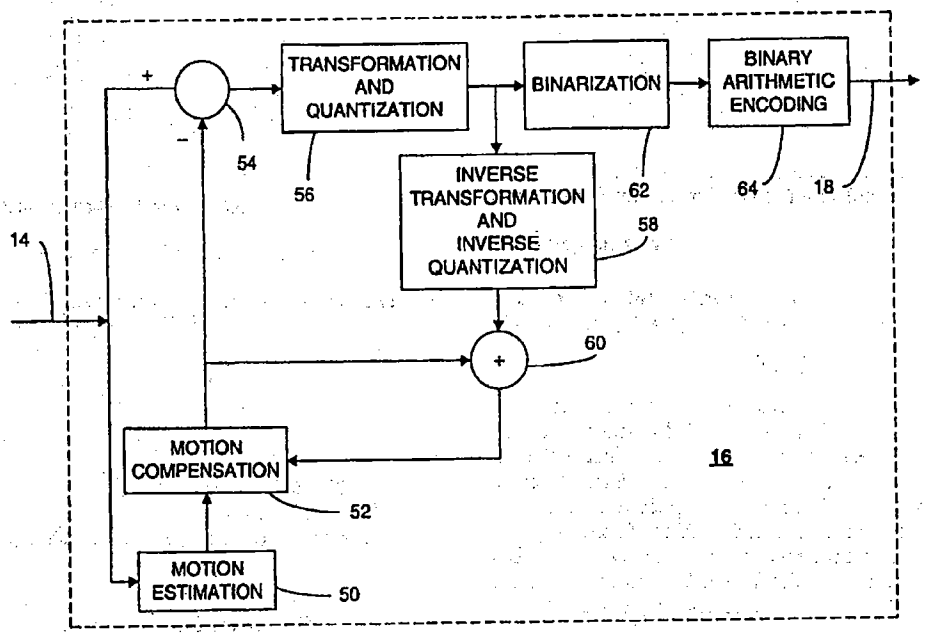
(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana

(57) **ABSTRACT**

The present invention is directed to an improved method for the binarization of data in an MPEG data stream. The invention makes use of unary binarization to create codewords up until an index threshold. Once the threshold has been met, succeeding code symbols have appended to them an exp-Golomb suffix. This hybrid binarization scheme reduces the number of binary codewords to be processed by a Binary Arithmetic Coder (BAC), thus reducing the computation required by the BAC.

21 Claims, 6 Drawing Sheets



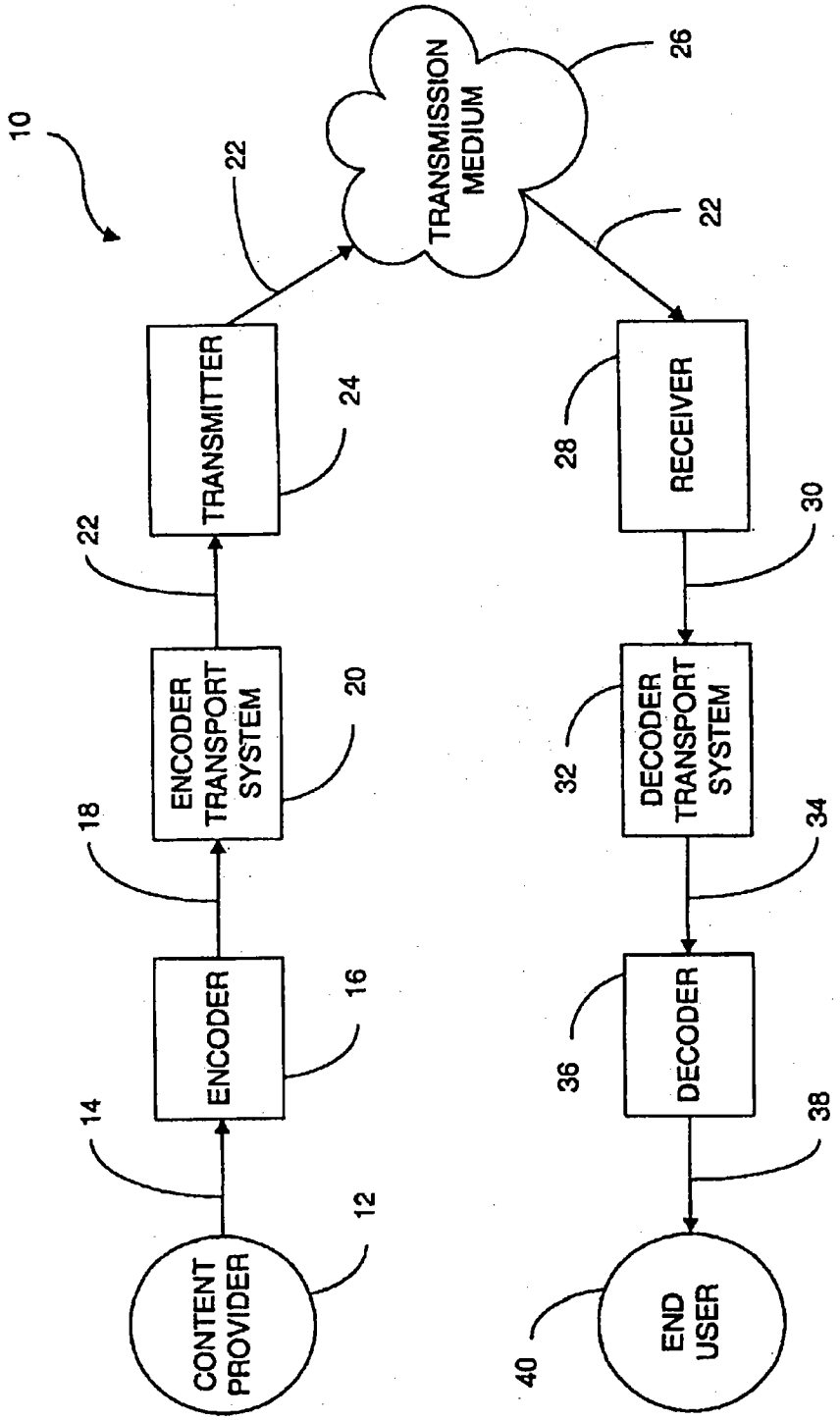

10
TRANSMISSION MEDIUM
26
22
22
TRANSMITTER
24
RECEIVER
28
22
30
ENCODER TRANSPORT SYSTEM
20
DECODER TRANSPORT SYSTEM
32
18
34
ENCODER
16
DECODER
36
14
38
CONTENT PROVIDER
12
END USER
40

FIG. 1

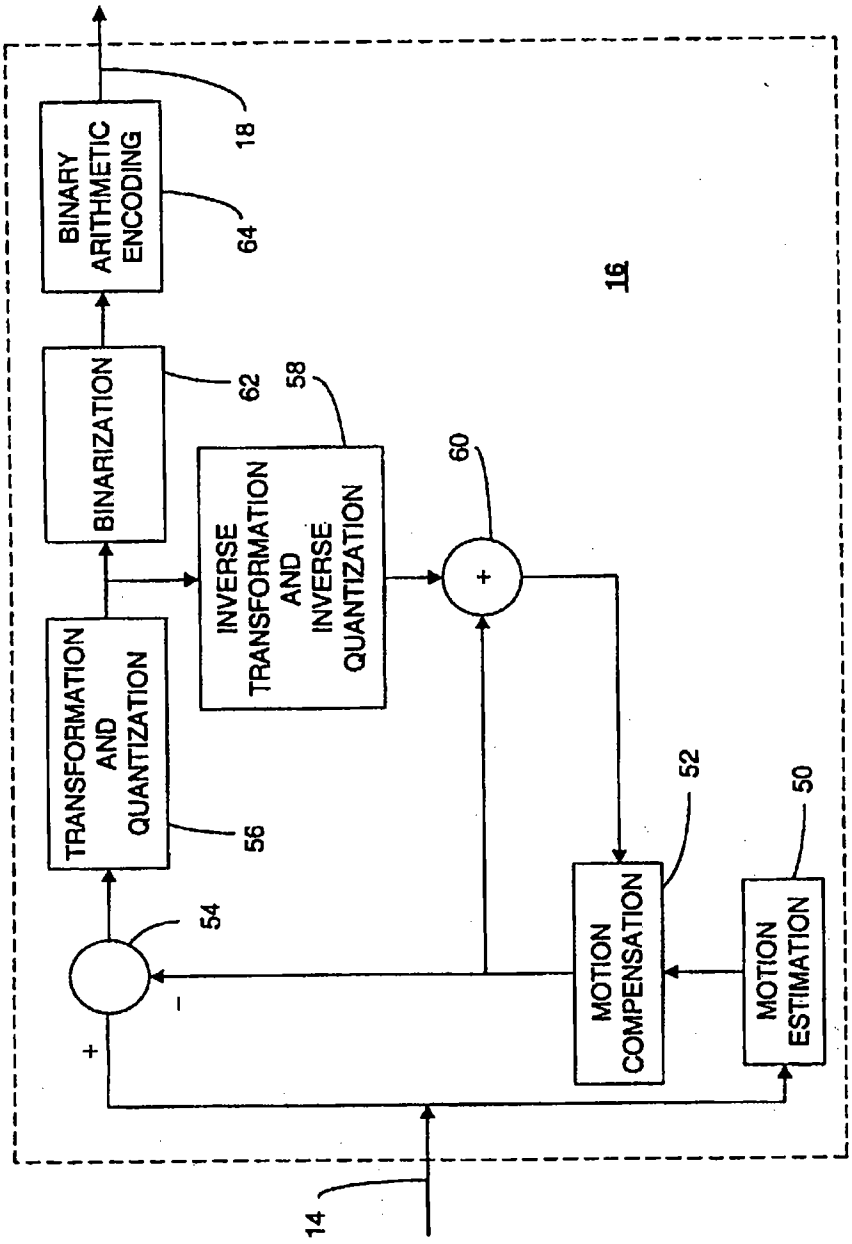

16
18
BINARY ARITHMETIC ENCODING
64
BINARIZATION
62
58
INVERSE TRANSFORMATION AND INVERSE QUANTIZATION
60
+
TRANSFORMATION AND QUANTIZATION
56
54
-
+
MOTION COMPENSATION
52
MOTION ESTIMATION
50
14

FIG. 2

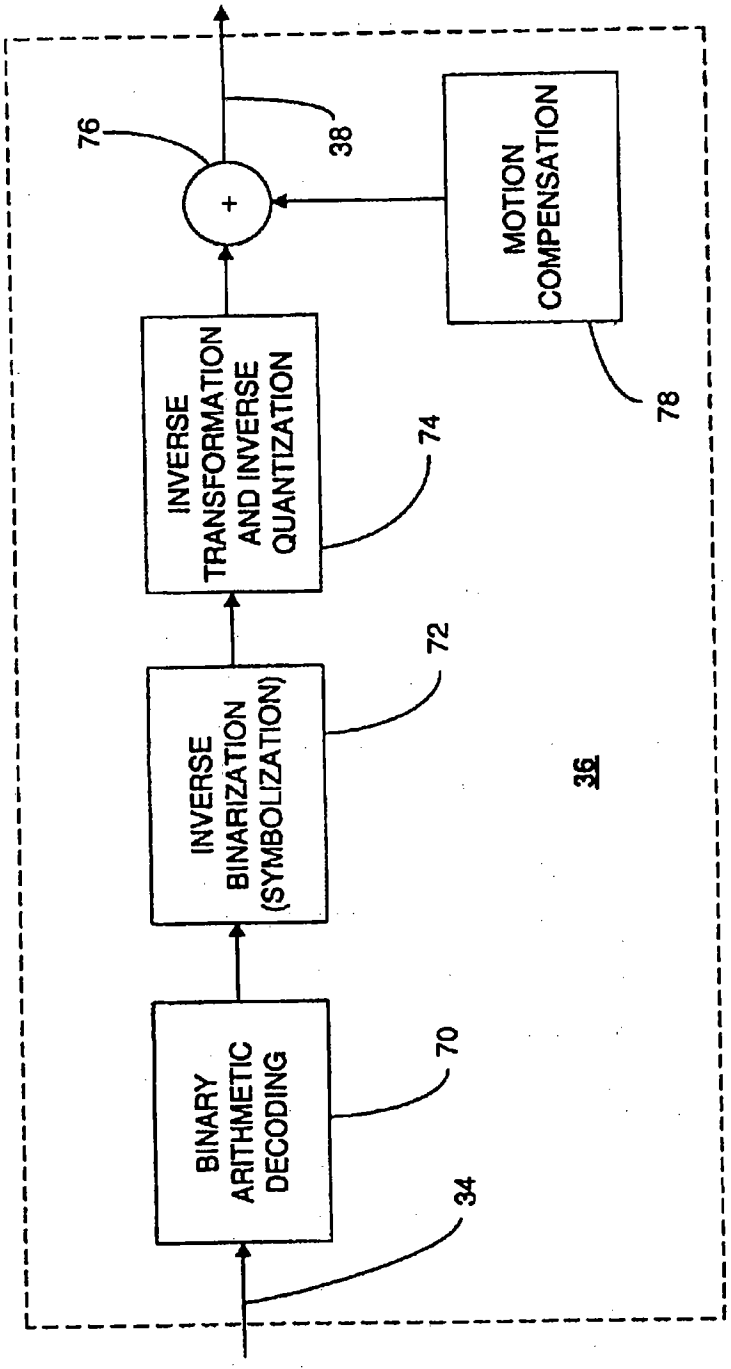

BINARY ARITHMETIC DECODING
70
INVERSE BINARIZATION (SYMBOLIZATION)
72
INVERSE TRANSFORMATION AND INVERSE QUANTIZATION
74
MOTION COMPENSATION
78
+
76
38
34
36

FIG. 3

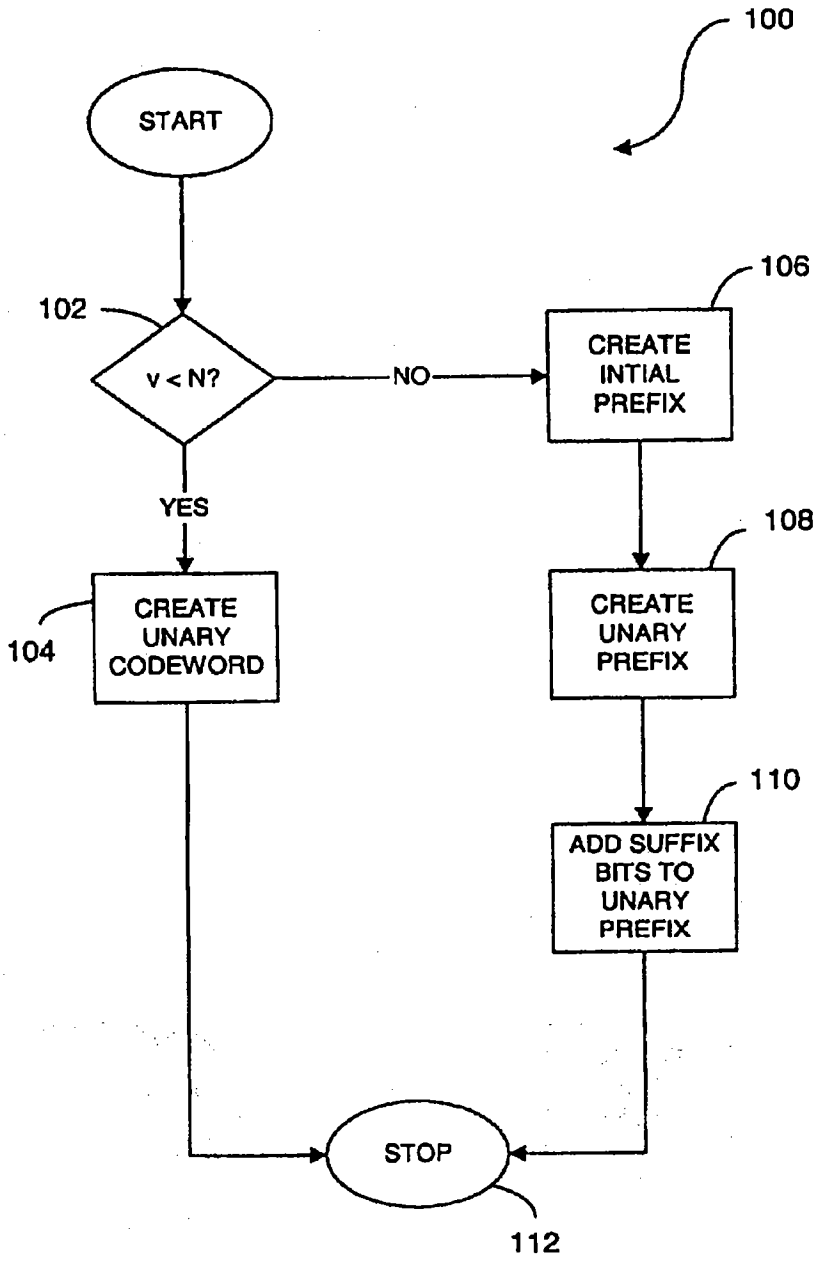

100
START
102
v < N?
NO
YES
106
CREATE INTIAL PREFIX
108
CREATE UNARY PREFIX
110
ADD SUFFIX BITS TO UNARY PREFIX
104
CREATE UNARY CODEWORD
STOP
112

FIG. 4

Table 3 - Motion vector magnitude residual binarization.

Index	Unary Prefix	exp-Golomb Suffix
0	0	
1	10	
2	110	
...		
63	1...1 0	
64	1...1 10	0
65	1...1 10	1
66	1...1 110	00
67	1...1 110	01
68	1...1 110	10
69	1...1 110	11
70	1...1 1110	000
71	1...1 1110	001
72	1...1 1110	010
73	1...1 1110	011
74	1...1 1110	100
75	1...1 1110	101
...		

FIG. 5

Table 4 - Coefficient level binarization.

Index	Unary Prefix	exp-Golomb Suffix
0	0	
1	10	
2	110	
...		
15	1...1 0	
16	1...1 10	0
17	1...1 10	1
18	1...1 110	00
19	1...1 110	01
20	1...1 110	10
21	1...1 110	11
22	1...1 1110	000
23	1...1 1110	001
24	1...1 1110	010
25	1...1 1110	011
26	1...1 1110	100
27	1...1 1110	101
...		

FIG. 6

METHOD AND SYSTEM FOR SYMBOL BINARIZATION

This is a continuation of U.S. Ser. No. 10/191,596, filed Jul. 10, 2002, now U.S. Pat. No. 6,744,387.

FIELD OF THE INVENTION

The present invention relates generally to a system and method for the compression of digital signals. More specifically, the present invention relates to reducing the file size or the bit rate required by a system using binary arithmetic encoding to entropy encode a digital signal such as a digital image or digital video.

BACKGROUND OF THE INVENTION

Throughout this specification we will be using the term MPEG as a generic reference to a family of international standards set by the Motion Picture Expert Group. MPEG reports to sub-committee 29 (SC29) of the Joint Technical Committee (JTC1) of the International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC).

Throughout this specification the term H.26x will be used as a generic reference to a closely related group of international recommendations by the Video Coding Experts Group (VCEG). VCEG addresses Question 6 (Q.6) of Study Group 16 (SG16) of the International Telecommunications Union Telecommunication Standardization Sector (ITU-T). These standards/recommendations specify exactly how to represent visual and audio information in a compressed digital format. They are used in a wide variety of applications, including DVD (Digital Video Discs), DVB (Digital Video Broadcasting), Digital cinema, and videoconferencing.

Throughout this specification the term MPEG/H.26x will refer to the superset of MPEG and H.26x standards and recommendations.

A feature of MPEG/H.26x is that these standards are often capable of representing a video signal with data roughly $1/50^{th}$ the size of the original uncompressed video, while still maintaining good visual quality. Although this compression ratio varies greatly depending on the nature of the detail and motion of the source video, it serves to illustrate that compressing digital images is an area of interest to those who provide digital transmission. MPEG/H.26x achieves high compression of video through the successive application of four basic mechanisms:

1) Storing the luminance (black & white) detail of the video signal with more horizontal and vertical resolution than the two chrominance (colour) components of the video.
2) Storing only the changes from one video frame to another, instead of the entire frame. Thus, often storing motion vector symbols indicating spatial correspondence between frames.
3) Storing these changes with reduced fidelity, as quantized transform coefficient symbols, to trade-off a reduced number of bits per symbol with increased video distortion.
4) Storing all the symbols representing the compressed video with entropy encoding, which exploits the statistics of the symbols, to reduce the number of bits per symbol without introducing any additional video signal distortion.

With regard to point 4), the symbols may be encoded as codewords in a variety of ways. One such encoding is binarization. Small codewords are well handled by unary or exp-Golomb binarizations while large codewords are best represented with the binarization limited to a reasonable length. Thus there is a need for a method and system binarization system that retains the most valuable properties of the unary and exp-Golomb binarizations. That is, small codewords should be distinguishable as with a unary binarization, while large codewords should have their binarization limited to a reasonable length. A binarization that simultaneously satisfies these two requirements will reduce the complexity and the bitrate/size for compressing and decompressing video, images, and signals that are compressed using binary arithmetic encoding for entropy encoding. The present invention addresses this need.

SUMMARY OF THE INVENTION

The present invention is directed to a method of binarization, the method comprising the step of determining if a code symbol index value is less than a threshold value, if so then constructing a codeword using a first binarization model; else constructing a codeword using a second binarization model.

The present invention is also directed to a binarization system, the system comprising means for determining if a code symbol index value is less than a threshold value, if so then utilizing means for constructing a codeword using a first binarization model; else utilizing means for constructing a codeword using a second binarization model.

The present invention is further directed to a computer readable medium containing instructions for binarization, comprising instructions for determining if a code symbol index value is less than a threshold value, if so then constructing a codeword using a first binarization model; else constructing a codeword using a second binarization model.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example, to the accompanying drawings which aid in understanding an embodiment of the present invention and in which:

FIG. **1** is a block diagram of a video transmission and receiving system;

FIG. **2** is a block diagram of an encoder;

FIG. **3** is a block diagram of a decoder;

FIG. **4** is a flowchart of a process for codeword construction;

FIG. **5** is a table for motion vector magnitude residual binarization; and

FIG. **6** is a table for coefficient level binarization.

DETAILED DESCRIPTION OF THE INVENTION

By way of introduction we refer first to FIG. **1**, a video transmission and receiving system, is shown generally as **10**. A content provider **12** provides a video source **14** to an encoder **16**. A content provider may be anyone of a number of sources but for the purpose of simplicity one may view video source **14** as originating from a television transmission, be it analog or digital. Encoder **16** receives video source **14** and utilizes a number of compression algorithms to reduce the size of video source **14** and passes an encoded stream **18** to encoder transport system **20**. Encoder transport system **20** receives stream **18** and restructures it into a transport stream **22** acceptable to transmitter **24**. Transmitter **24** then distributes transport stream **22**

through a transport medium **26** such as the Internet or any form of network enabled for the transmission of MPEG data streams. Receiver **28** receives transport stream **22** and passes it as received stream **30** to decoder transport system **32**. In a perfect world, steams **22** and **30** would be identical. Decoder transport system **32** processes stream **30** to create a decoded stream **34**. Once again, in a perfect world streams **18** and **34** would be identical. Decoder **36** then reverses the steps applied by encoder **16** to create output stream **38** that is delivered to the user **40**.

There are several existing major MPEG/H.26x standards: H.261, MPEG-1, MPEG-2/H.262, MPEG-4/H.263. Among these, MPEG-2/H.262 is clearly most commercially significant, being sufficient for all the major TV standards, including NTSC (National Standards Television Committee) and HDTV (High Definition Television). Of the series of MPEG standards that describe and define the syntax for video broadcasting, the standard of relevance to the present invention is the draft standard ITU-T Recommendation H.264, ISO/IEC 14496-10 AVC, which is incorporated herein by reference and is hereinafter referred to as "MPEG-AVC/H.264".

An MPEG video transmission is essentially a series of pictures taken at closely spaced time intervals. In the MPEG/H.26x standards a picture is referred to as a "frame", and a "frame" is completely divided into rectangular sub-partitions known as "picture blocks", with associated "motion vectors". Often a picture may be quite similar to the one that precedes it or the one that follows it. For example, a video of waves washing up on a beach would change little from picture to picture. Except for the motion of the waves, the beach and sky would be largely the same. Once the scene changes, however, some or all similarity may be lost. The concept of compressing the data in each picture relies upon the fact that many images often do not change significantly from picture to picture, and that if they do the changes are often simple, such as image pans or horizontal and vertical block translations. Thus, transmitting only block translations (known as "motion vectors") and differences between picture blocks, as opposed to the entire picture, can result in considerable savings in data transmission.

Usually motion vectors are predicted, such that they are represented as a difference from their predictor, known as a predicted motion vector residual. In practice, the pixel differences between picture blocks are transformed into frequency coefficients, and then quantized to further reduce the data transmission. Quantization allows the frequency coefficients to be represented using only a discrete number of levels, and is the mechanism by which the compressed video becomes a "lossy" representation of the original video. This process of transformation and quantization is performed by an encoder.

Referring now to FIG. **2** a block diagram of an encoder is shown generally as **16**. Encoder **16** accepts as input video source **14**. Video source **14** is passed to motion estimation module **50**, which determines the motion difference between frames. The output of motion estimate module **50** is passed to motion compensation module **52**. At combination module **54**, the output of motion compensation module **52** is subtracted from the input video source **14** to create input to transformation and quantization module **56**. Output from motion compensation module **52** is also provided to module **60**. Module **56** transforms and quantizes output from module **54**. The output of module **56** may have to be recalculated based upon prediction error, thus the loop comprising modules **52**, **54**, **56**, **58** and **60**. The output of module **56** becomes the input to inverse transformation module **58**. Module **58** applies an inverse transformation and an inverse quantization to the output of module **56** and provides that to module **60** where it is combined with the output of module **52** to provide feedback to module **52**.

Binarization module **62** is where the present invention resides. Module **62** accepts as input, symbols created by module **56** and creates a binary representation of each one in of the form of a codeword. The codewords are passed to binary arithmetic encoding module **64** where the frequency of each codeword is determined and the most frequently occurring codewords are assigned the lowest values. The output of module **64** is encoded stream **18**.

With regard to the above description of FIG. **2**, as those skilled in the art will appreciate that the functionality of the modules illustrated are well defined in the MPEG family of standards. Further, numerous variations of modules of FIG. **2** have been published and are readily available.

Referring now to FIG. **3** a block diagram of a decoder is shown. Decoder **36** accepts as input decoded stream **34** to binary arithmetic decoding module **70**. Module **70** decodes the binary arithmetic encoding performed by module **64** (see FIG. **2**) and passes the output to inverse binarization module **72**. Module **72** reverses the binarization of module **62** (see FIG. **2**) and passes its output to inverse transformation and inverse quantization module **74**, which reverses the effects of module **56** (see FIG. **2**). At combination module **76** the output from module **74** is combined with the output of motion compensation module **78** to create output stream **38**.

The MPEG/H.26x standards define precisely the syntax that is used for specifying how quantized coefficients, motion vectors, and other associated information such as block modes are to be represented, as well as the semantics for reconstructing video source **14** from the syntax of encoded stream **18**. In particular, codewords such as transformed-quantized picture differences and predicted motion vector residuals are entropy coded with such schemes as variable length codes (e.g. Huffman codes) or arithmetic encoding to become the syntax elements that form encoded bitstream **18**.

Several types of arithmetic codecs (encoder/decoder pairs) exist. One of the most efficient is the family of binary arithmetic coders (BACs). Well-known members of this family include, among others, the Q-coder, QM-coder, MQ-coder, and Qx-coder. A BAC accepts as input a binary representation of a codeword and by recursively examining the codewords it receives, is able to compress the codewords based upon the probability of their frequency.

Since BACs operate only on binary valued data, a signal compression standard such as MPEG-AVC/H.264 maps codewords such as transformed-quantized picture differences and motion vector residuals to binarized symbol representations prior to binary arithmetic encoding.

Among the commonly used binarization methods are the following: unary, binary, Golomb, and exp-Golomb.

Unary binarization consists of a number of binary 1's equal to an index for a symbol followed by a zero as shown in Table 1.

TABLE 1

Binarization by means of the unary code tree

Symbol Index	Codeword							
0	0							
1	1	0						
2	1	1	0					
3	1	1	1	0				
4	1	1	1	1	0			
5	1	1	1	1	1	0		
6	1	1	1	1	1	1	0	
...	.	.	.	.	.	.	.	.
bin_no.	1	2	3	4	5	6	7	...

The first column of Table 1 contains an index for a symbol. The corresponding row for each index contains a

binarization of the symbol represented by the index into a codeword. Thus symbol index "0" results in a codeword of a single bit, namely "0". Symbol "1" results in a codeword of "10", which comprises two bits, and so on. The row labeled bin_no at the bottom of Table 1 contains the frequency of each bit for a codeword. For example bin_no "1" will contain the number of 0's and 1's that occur as the first bit of a codeword. Similarly bin_no "2" contains the number of 0's and 1's in the second bit of a codeword, and so on.

A BAC by examining each bin_no can determine the length and frequency of a codeword by determining if there is a zero in the bin. For example bin_no "5" will contain a zero for each codeword having a length of five, thus allowing the BAC to determine the number or frequency of five bit codewords.

The advantage of the unary binarization is that a bin containing a value 0 distinguishes a particular codeword from all codewords with a larger symbol index. Therefore, the BAC can be constructed to separately account for the statistical frequency of every individual codeword by maintaining separate statistics on the frequency of zeroes and ones for every bin. A disadvantage of unary binarization is that in practice the statistics of high bins are lumped together since the smaller, more frequent codewords account for the majority of the bitstream, and infrequently occurring codewords do not occur often enough to enable accurate gathering of statistical data. A major disadvantage of unary binarization is that the number of binary values that must run through the BAC will, in the worst case, be as many bins as the largest symbol index (which may range into the tens of thousands). For example, the encoding of a large symbol index may require tens of thousands of binary bins to be sent through the BAC.

Binary binarization creates a codeword as a fixed length binary representation of the symbol index. Thus symbol index "3" is encoded as "11", with the appropriate number of leading zeros applied. The disadvantage of binary binarization is that a single bin no longer distinguishes each codeword uniquely. This results in a greatly reduced compression ratio.

Golomb and exp-Golomb codewords, which use a unary prefix followed by a binary postfix, may be regarded as compromise positions between unary and binary binarizations. Golomb codewords with parameter 'k' begin with unary binarizations as shown by the column labeled MSB (Most Significant Bits) in Table 2. Appended to the unary binarization are 'k' binary bits as is shown in the column labeled LSB (Least Significant Bits) in Table 2. This combination produces 2**k distinct binarizations for each MSB. The example illustrated in Table 2 shows an exp-Golomb code with k=1, thus the first LSB contains 2**1 values. The next level contains 2**2 LSB values and so on. Unfortunately, this still permits extremely long binarizations to occur for large symbol indices.

TABLE 2

	Exp-Golomb codes.	
Index	MSB	LSB
0	0	
1	10	0
2	10	1
3	110	00
4	110	01
5	110	10
6	110	11
7	1110	000

TABLE 2-continued

	Exp-Golomb codes.	
Index	MSB	LSB
8	1110	001
9	1110	010
10	1110	011
11	1110	100
12	1110	101

The exp-Golomb code does greatly reduce the maximum possible number of bins in the binarization of symbol indices. However, it does not permit codewords with a small symbol index (other than index 0) to be uniquely distinguished from codewords with larger symbol indices. This results in reduced compression ratio for the binarizations, relative to the unary binarization of Table 1.

The present invention provides a binarization that retains the most valuable properties of the unary and exp-Golomb binarizations. That is, small codewords are distinguishable as with a unary binarization, while large codewords have their binarization limited to a reasonable length. By doing so, the present invention provides a binarization that reduces the complexity and the bitrate/size for compressing and decompressing video, images, and signals that are compressed using binary arithmetic encoding for entropy encoding.

The present invention allows for the maintenance of a true prefix code, while switching between a unary binarization for small codeword indices and a modified exp-Golomb binarization for larger codewords. The invention prepends a fixed prefix to an exp-Golomb code that begins at a fixed index value, prior to which unary binarization is used.

Referring to FIG. **5** and **6**, Tables 3 and Table 4 demonstrate particular instances of this new class of binary codes: hybrid unary-exp-Golomb codes. Table 3 illustrates a binarization that is particularly appropriate for the binarization of quarter pixel motion vector residual magnitudes of MPEG-AVC/H.264.

With these binarizations illustrated in Tables 3 and 4, bitrate and complexity are both reduced for MPEG-AVC/H.264 relative to other known binarizations.

A detailed description of the method for constructing such hybrid binarizations follows. Let N be the threshold at which unary to exp-Golomb switching occurs (N=64 for Table 3, N=16 for Table 4). The construction of a codeword of this modified unary binarization table for a given index v is given by the following algorithm:

If v<N

1) use a unary code of v 1's terminated with a 0

If v>=N

1) Form an initial prefix of (N−1) 1's;

2) Determine the number of bits γ+1 required to represent v−(N−2). For example, for N=64, $\gamma=\lfloor \log_2(v-62) \rfloor$, and put it in a unary representation. The unary representation is appended to the initial prefix to form the unary prefix as shown in Tables 3 and 4.

3) Append the γ least significant bits of "g" where g=v−(N−2)−2**γ in its binary representation to the prefix.

4) The corresponding bits obtained at step 3) are shown in the exp-Golomb Suffix column of Tables 3 and 4.

Referring now to FIG. **4**, a flowchart of a process for codeword construction is shown generally as **100**. Process **100** illustrates the steps of the present invention. Process **100** begins at step **102** where a test is made to determine if the

value of the code symbol index is less than the value of the threshold. If it is processing moves to step **104** were a unary codeword is constructed comprising a series of v 1's terminated with a 0. Processing then ends at step **112**. Returning to step **102** if the test is negative, processing moves to step **106**, where an initial prefix of N 1's is created. Processing then moves to step **108** where the most significant bits of the value v−(N−2) are extracted and converted to a unary representation. The unary representation is then appended to the initial prefix to create a unary prefix. Process **100** then moves to step **110** where the binary representation of the least significant bits of the value of v−(N−2) are appended to the unary prefix to create the codeword.

Although the description of the present invention describes a binarization scheme for MPEG-AVC/H.264, it is not the intent of the inventors to restrict this binarization scheme solely to the referenced proposed standard. As one skilled in the art can appreciate any system utilizing BAC may make use of the present invention improve binarization.

Although the present invention has been described as being implemented in software, one skilled in the art will recognize that it may be implemented in hardware as well. Further, it is the intent of the inventors to include computer readable forms of the invention. Computer readable forms meaning any stored format that may be read by a computing device.

Although the invention has been described with reference to certain specific embodiments, various modifications thereof will be apparent to those skilled in the art without departing from the spirit and scope of the invention as outlined in the claims appended hereto.

What is claimed is:

1. A method for generating an index value from a codeword for digital video decoding, comprising the steps of:

(A) setting said index value to a threshold in response to a first portion of said codeword having a first pattern;

(B) adding an offset to said index value based on a second pattern in a second portion of said codeword following said first portion in response to said first portion having said first pattern; and

(C) adding a value to said index value based on a third pattern in a third portion of said codeword following said second portion in response to said first portion having said first pattern.

2. The method according to claim **1**, further comprising the step of:

generating said index value based on a fourth pattern in said first portion in response to said fourth pattern being other than said first pattern.

3. The method according to claim **2**, wherein said first pattern is a predetermined pattern unique from all possible representations of said fourth pattern.

4. The method according to claim **2**, wherein said fourth pattern comprises (i) between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state.

5. The method according to claim **4**, wherein said second bit follows said first bits.

6. The method according to claim **1**, wherein said first pattern comprises a plurality of bits each having a first state.

7. The method according to claim **1**, wherein said second pattern comprises between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state.

8. The method according to claim **1**, wherein said third pattern comprises a binary number.

9. The method according to claim **1**, wherein said codeword in compatible with at least one of an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264.

10. The method according to claim **1**, further comprising the step of:

generating said index value based on a fourth pattern in said first portion in response to said fourth pattern being other than said first pattern, wherein (i) said first pattern comprises a plurality of bits each having a first state, (ii) said first pattern is unique from all possible representations of said fourth pattern, (iii) each of said representations of said fourth pattern ends in a bit having a second state opposite said first state and (iv) said second pattern has a same number of bits as said third pattern.

11. A system comprising:

a decoder configured to generate a codeword; and

a circuit configured to (i) set an index value to a threshold in response to a first portion of said codeword having a first pattern, (ii) add an offset to said index value based on a second pattern in a second portion of said codeword following said first portion in response to said first portion having said first pattern and (iii) add a value to said index value based on a third pattern in a third portion of said codeword following said second portion in response to said first portion having said first pattern.

12. A method for generating a codeword from an index value for digital video encoding, comprising the steps of:

(A) generating a first pattern in a first portion of said codeword in response to said index value being at least as great as a threshold;

(B) generating a second pattern in a second portion of said codeword following said first portion representing an offset of said index value above said threshold; and

(C) generating a third pattern in a third portion of said codeword following said second portion representing a value of said index value above said offset.

13. The method according to claim **12**, further comprising the step of:

generating a fourth pattern in said first portion based on said index value in response to said index value being below said threshold.

14. The method according to claim **13**, wherein said first pattern is a predetermined pattern unique from all possible representations of said fourth pattern.

15. The method according to claim **13**, wherein said fourth pattern comprises (i) between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state.

16. The method according to claim **12**, wherein (i) said offset has a first representation and (ii) said value has a second representation different than said first representation.

17. The method according to claim **12**, wherein said second pattern has a same number of bits as said third pattern.

18. The method according to claim **12**, wherein said second portion is void in response to said index value being below said threshold.

19. The method according to claim **12**, wherein said third portion is void in response to said index value being below said threshold.

20. The method according to claim **12**, wherein said codeword in compatible with at least one of an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264.

21. A system comprising:

a circuit configured to (i) generate a first pattern in a first portion of a codeword in response to an index value

being at least as great as a threshold, (ii) generate a second pattern in a second portion of said codeword following said first portion representing an offset of said index value above said threshold and (iii) generating a third pattern in a third portion of said codeword following said second portion representing a value of said index value above said offset; and

an encoder configured to encode said codeword.

* * * * *

EXHIBIT C

US006452958B1

(12) **United States Patent**
van Nee

(10) **Patent No.: US 6,452,958 B1**
(45) **Date of Patent: Sep. 17, 2002**

(54) **DIGITAL MODULATION SYSTEM USING EXTENDED CODE SET**

(75) Inventor: **Richard D. J. van Nee**, De Meern (NL)

(73) Assignee: **Agere Systems Guardian Corp**, Miami Lakes, FL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/064,188**

(22) Filed: **Apr. 22, 1998**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/057,310, filed on Apr. 8, 1998, which is a continuation-in-part of application No. 08/688,574, filed on Jul. 30, 1996, now Pat. No. 5,862,182.

(51) **Int. Cl.**[7] **H04B 1/69**

(52) **U.S. Cl.** **375/130**; 375/140; 370/208

(58) **Field of Search** 375/136, 146, 375/145, 130, 135, 140, 142, 147, 150, 271, 280, 281, 299, 308, 329, 331, 332, 349, 284, 285; 370/18, 206, 208, 209; 380/34, 37

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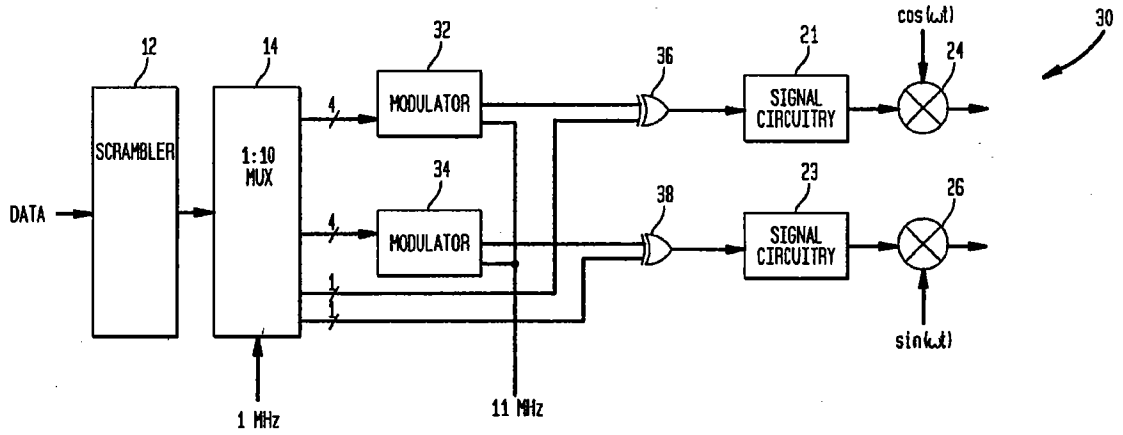
Primary Examiner—Stephen Chin
Assistant Examiner—Chieh M. Fan
(74) *Attorney, Agent, or Firm*—John A. Ligon

(57) **ABSTRACT**

A digital (de)modulation system uses a larger code set of M codes for N length codes, where M>N, to provide an increased data rate while maintaining the coding gain. For example, the system can use 16 different codes each having a length of 11 chips in a code set while the conventional M-ary keying systems use a code set size of 8 for 11-chip codes or 8-chip codes. By extending the code set size, the system increases the data rate of the system. With 16 codes and the ability to change the sign of the code to be transmitted, the system can encode 5 data bits on both I and Q, so a total of 10 data bits can be encoded per code symbol. In this embodiment, a code symbol contains an 11 chip code on a I modulation branch and an 11 chip code on a Q modulation branch. As such, using 11 chip codes and a chip rate of 11 Mhz, the system provides a data rate of 10 Mbps while conventional M-ary keying systems can only achieve 8 Mbps using the same code length and chip rate. By extending the code length, the processing gain is increased. The extended code set is not orthogonal, so a non-zero cross-correlation value results between the different codes of the code set. However, the resulting noise and multipath performance degradation can be kept small by choosing code sets with small cross-correlation values (nearly orthogonal). The magnitudes of both cross-correlation values and auto-correlation sidelobes should preferably be below half a code length. In some embodiments, the code set is derived from orthogonal codes which are modified to reduce the autocorrelation sidelobes associated with the orthogonal codes. In other embodiments, the code set is derived using a complementary code which provides low autocorrelation sidelobes and is modified to reduce the cross-correlation values between the codes.

49 Claims, 5 Drawing Sheets



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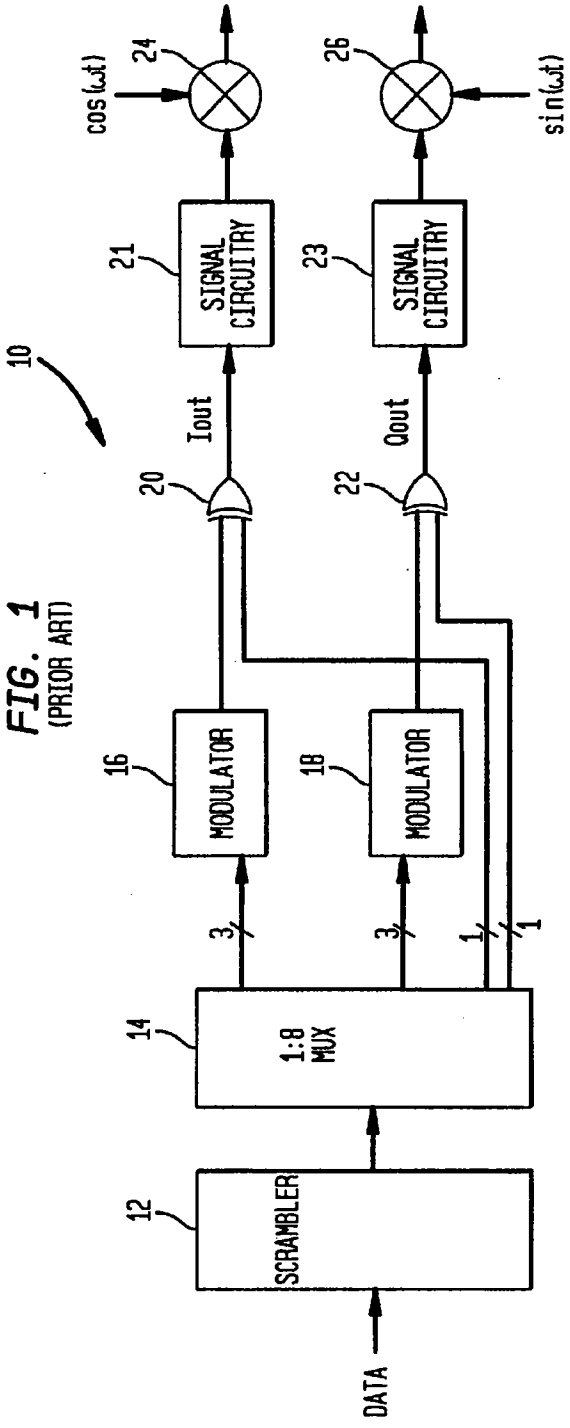


FIG. 1
(PRIOR ART)

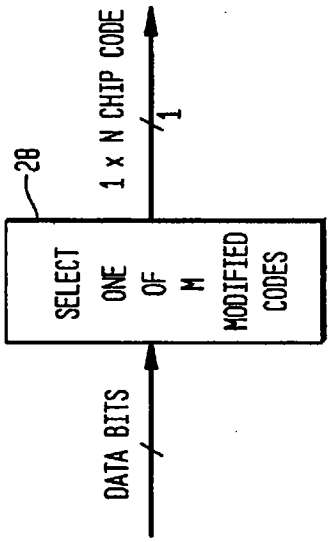


FIG. 2

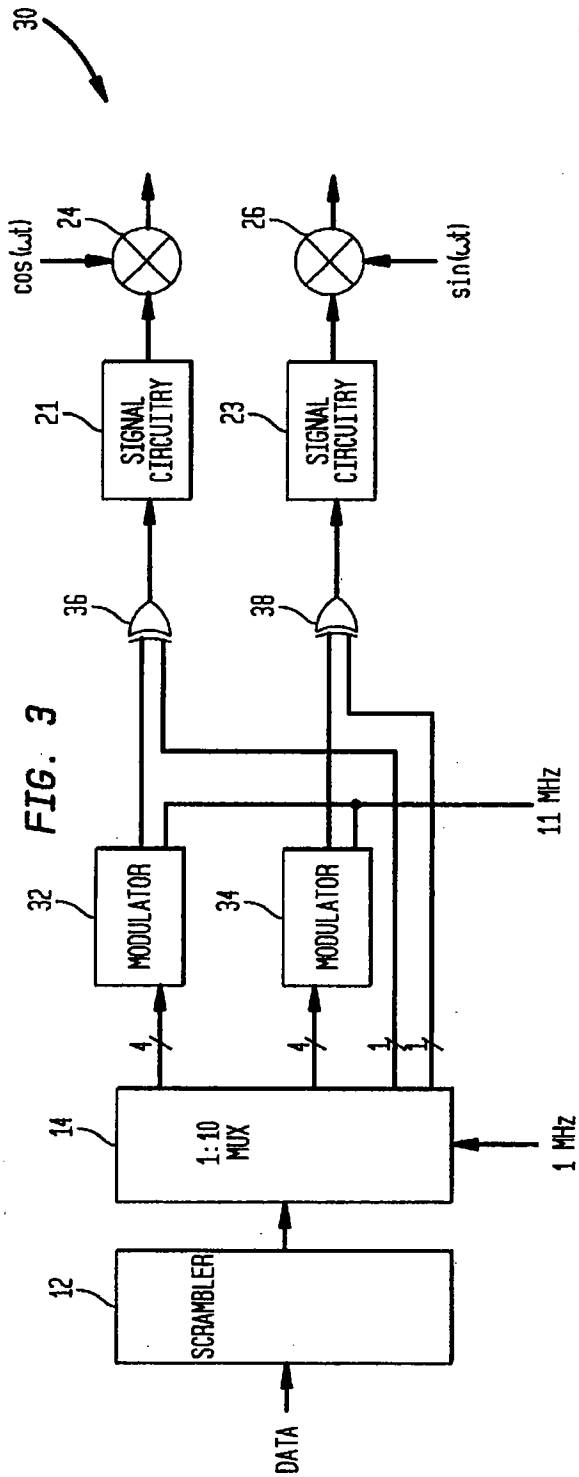

30
cos(ωt)
24
26
sin(ωt)
21
SIGNAL CIRCUITRY
23
SIGNAL CIRCUITRY
36
38
11 MHz
32
MODULATOR
34
MODULATOR
4
4
1
1
14
1:10 MUX
1 MHz
12
SCRAMBLER
DATA

FIG. 3

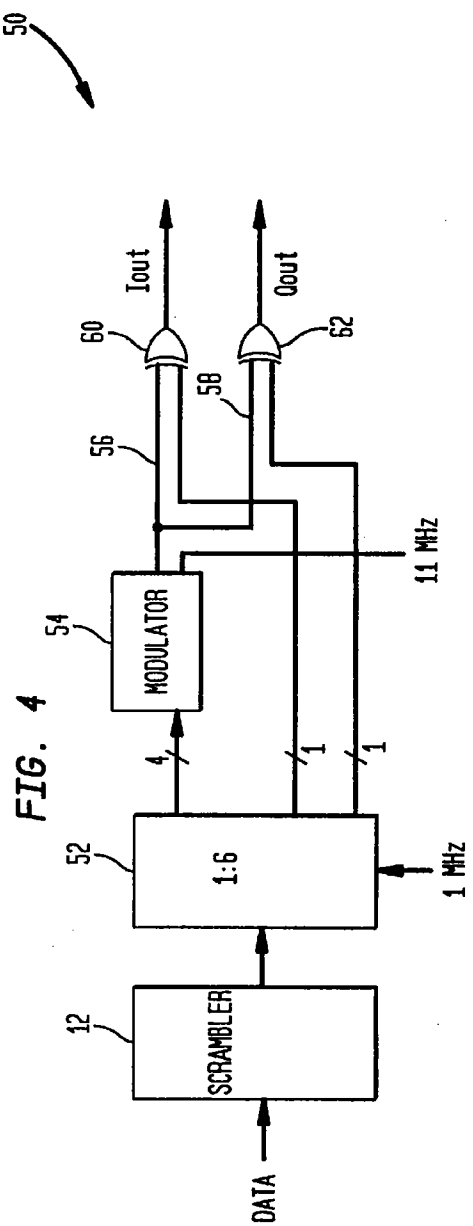

50
Iout
Qout
60
62
58
56
11 MHz
54
MODULATOR
4
1
1
52
1:6
1 MHz
12
SCRAMBLER
DATA

FIG. 4

FIG. 5

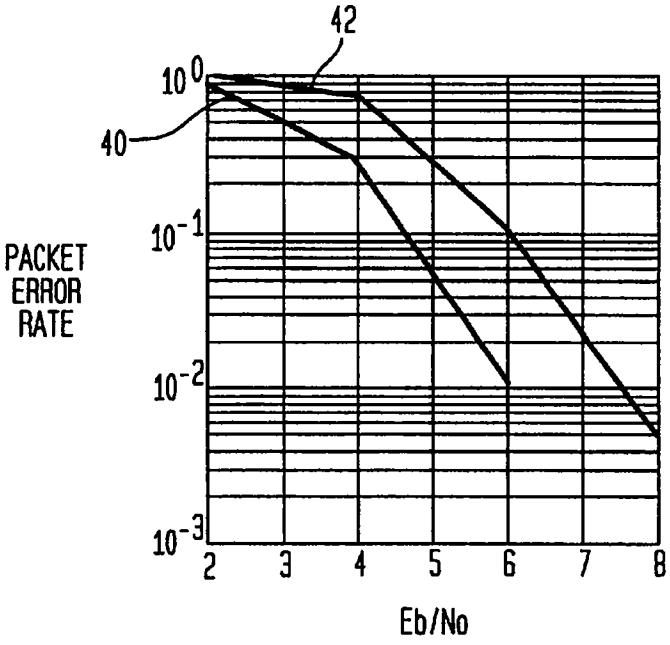
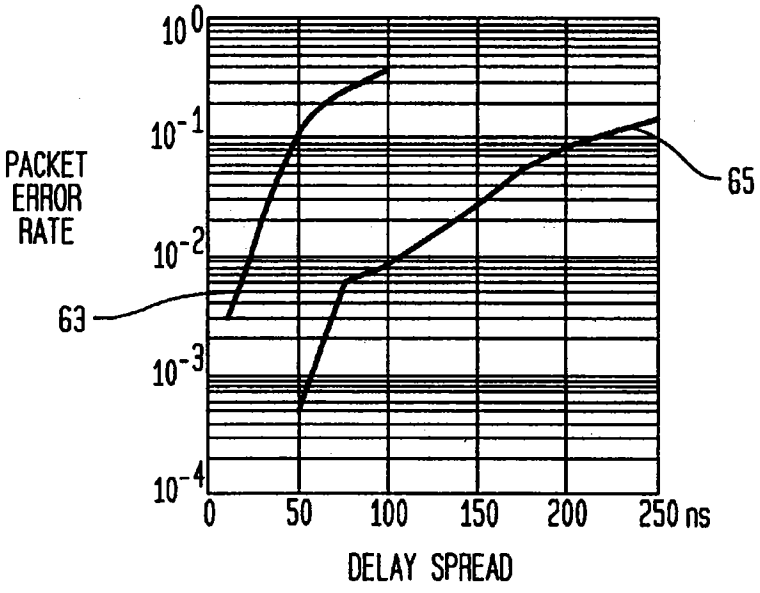

42
40
10^0
10^{-1}
10^{-2}
10^{-3}
PACKET ERROR RATE
2
3
4
5
6
7
8
Eb/No

FIG. 6


10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
PACKET ERROR RATE
63
65
0
50
100
150
200
250 ns
DELAY SPREAD

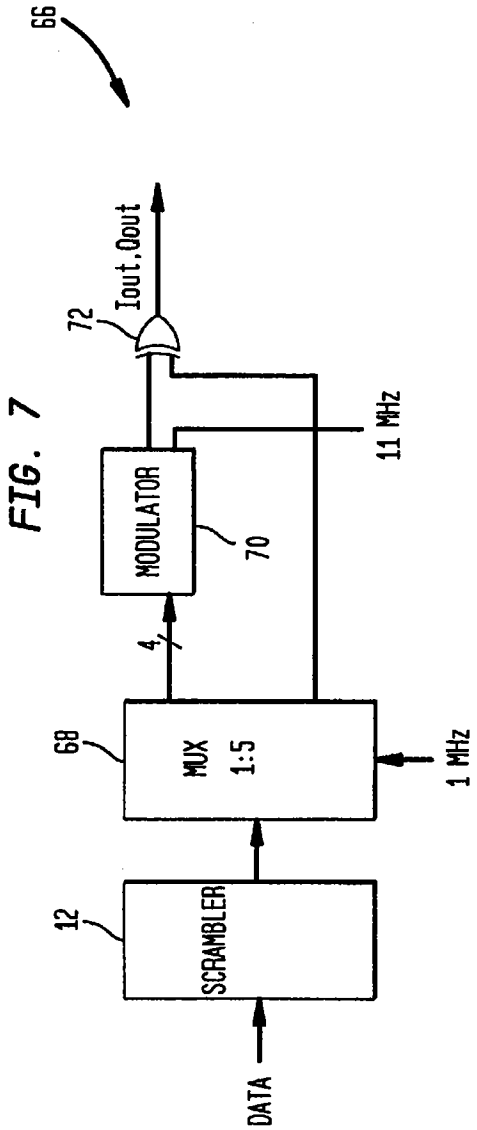

66
72
Iout.Qout
11 MHz
MODULATOR
70
4
68
MUX 1:5
1 MHz
12
SCRAMBLER
DATA

FIG. 7

110
114
DETECT PHASE
DEMODULATOR
76
116
112
FIND CODE WITH LARGEST COMPLEX MAGNITUDE
CORRELATORS
90
92
CORRELATORS
LPF
LPF
cosωt
sinωt
86
88
82
84

FIG. 10

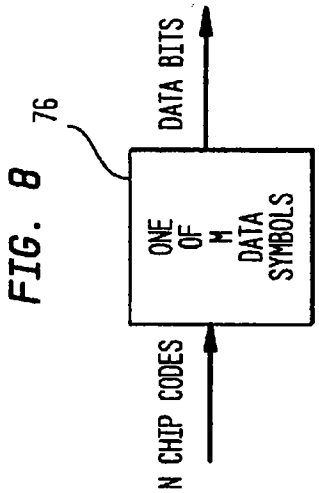

76
DATA BITS
ONE OF M DATA SYMBOLS
N CHIP CODES

FIG. 8

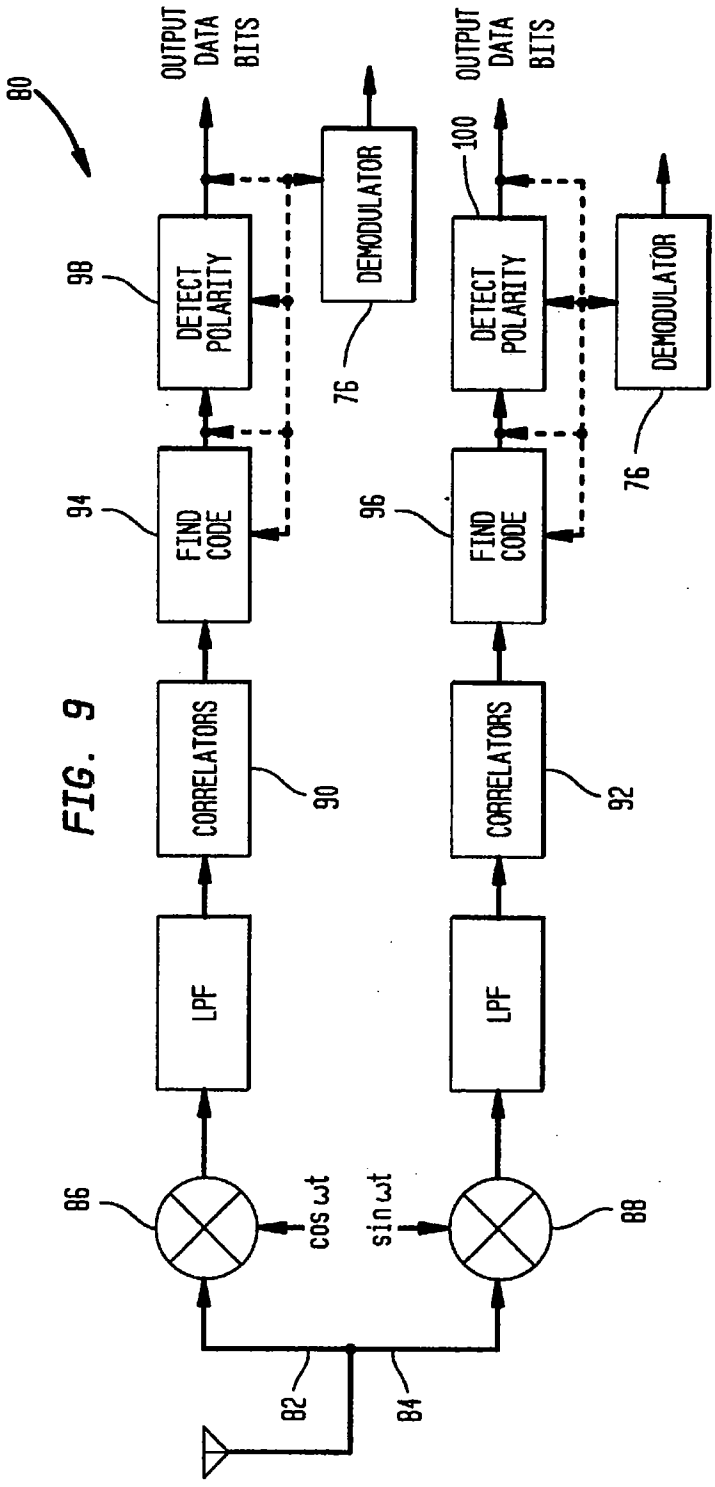

80
OUTPUT DATA BITS
DEMODULATOR
98
DETECT POLARITY
94
FIND CODE
CORRELATORS
90
LPF
86
cos ωt
82
OUTPUT DATA BITS
100
DETECT POLARITY
DEMODULATOR
76
96
FIND CODE
CORRELATORS
92
LPF
sin ωt
88
84

FIG. 9

DIGITAL MODULATION SYSTEM USING EXTENDED CODE SET

This application is a continuation in part of U.S. patent application Ser. No. 09/057,310, filed Apr. 8, 1998, which is a continuation in part of US. patent application Ser. No. 08/688,574, filed Jul. 30, 1996, and issued Jan. 19, 1999 as U.S. Pat. No. 5,862,182, the disclosures of both applications being incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to wireless communication systems and, more particularly, to a digital modulation system that uses an extended code set to encode information.

2. Description of Related Art

A wireless communications channel can rarely be modeled as purely line-of-site. Therefore, one must consider the many independent paths that are the result of scattering and reflection of a signal between the many objects that lie between and around the transmitting station and the receiving station. The scattering and reflection of the signal creates many different "copies" of the transmitted signal ("multipath signals") arriving at the receiving station with various amounts of delay, phase shift and attenuation. As a result, the received signal is made up of the sum of many signals, each traveling over a separate path. Since these path lengths are not equal, the information carried over the radio link will experience a spread in delay as it travels between the transmitting station and the receiving station. The amount of time dispersion between the earliest received copy of the transmitted signal and the latest arriving copy having a signal strength above a certain level is often referred to as delay spread. Delay spread can cause intersymbol interference (ISI). In addition to delay spread, the same multipath environment causes severe local variations in the received signal strength as the multipath signals are added constructively and destructively at the receiving antenna. A multipath component is the combination of multipath signals arriving at the receiver at nearly the same delay. These variations in the amplitude of the multipath components is generally referred to as Rayleigh fading, which can cause large blocks of information to be lost.

Digital modulation techniques can be used to improve the wireless communication link by providing greater noise immunity and robustness. In certain systems, the data to be transmitted over the wireless communication link can be represented or encoded as a time sequence of symbols, where each symbol has M finite states, and each symbol represents n bits of information. Digital modulation involves choosing a particular code symbol from the M finite code symbols based on the data bits of information applied to the modulator. For M-ary keying schemes, $\log_2 M$ bits of information can be represented or encoded by M different codes or code symbols of at least M chips long. The codes are transmitted and received as several delayed replicas of the transmitted codes, and the receiver correlates the delayed versions of the received codes with the known codes.

Autocorrelation sidelobes show the correlation values between the known codes and the time shifted replicas of the received codes. For example, for a code (111-1), the autocorrelation for a zero shift is:

code	1 1 1 −1
shifted code	1 1 1 −1
multiplication	1 1 1 1
correlation = sum of multiplied values = 4.	

For a shift of one chip, the autocorrelation is:

code	1 1 1 −1
shifted code	1 1 1 −1
multiplication	1 1 −1
correlation = sum of multiplied values = 1.	

For a shift of 2 chips, the autocorrelation is:

code	1 1 1 −1
shifted code	1 1 1 −1
multiplication	1 −1
correlation = sum of multiplied values = 0.	

For a shift of 3 chips, the autocorrelation is:

code	1 1 1 −1
shifted code	1 1 1 −1
multiplication	−1
correlation = sum of multiplied values = −1.	

Larger shifts give an autocorrelation value of zero, so the maximum autocorrelation sidelobe in this example has a value or magnitude of 1. In this example, −1's are used in the receiver instead of 0's. The autocorrelation sidelobes give an indication about multipath performance. If the autocorrelation sidelobes are large, several multipath components heavily interfere with each other. Cross-correlation refers to a code being correlated with different codes. As such, if the cross-correlation between codes is high, then the different codes will interfere with each other.

M-ary orthogonal keying is a form of digital modulation which provides good cross-correlation between codes by encoding data using orthogonal codes which do not interfere with each other. FIG. **1** shows a general block diagram of an M-ary orthogonal keying system **10**. In this example, input data is scrambled by a scrambler **12** as specified in the current (1997) Institute of Electrical and Electronics Engineers (IEEE) 802.11 standard. The data is then provided to a serial-to-parallel converter **14** which converts the serial data into 8 parallel bits forming a data symbol. A first modulator **16** receives three (3) of the parallel bits and produces a code of length 8 chips from a look-up table; and a second modulator **18** receives three (3) of the parallel bits and produces a second code of length 8 from a look-up table. Chips are actually code bits, but they are called chips to distinguish them from data bits. In this implementation, one of the parallel bits is provided to a first exclusive-or (XOR) gate **20** which inverts the code from the first modulator **16** if the bit has a value of one. Similarly, the last remaining bit is provided to a second XOR gate **22** which inverts the code from the second modulator **18** if the bit has a value of one. In this embodiment, the output I_{out} of the XOR gate **20** is applied to signal circuitry **21** to convert all 0's to −1's for transmission. The circuitry **21** can also manipulate, convert and/or process I_{out} before being used to modulate a carrier

with frequency ω by mixer **24**. The output Q_{out} from the XOR **22** is applied to signal circuitry **23** to convert all 0's into −1's for transmission. The circuitry **23** can manipulate, convert and/or process Q_{out} before being used to modulate a 90 degrees shifted carrier by mixer **26**. In this particular embodiment, the first modulator 16 corresponds to the in-phase (I) component of the output signal, and the second modulator **18** corresponds to the quadrature (Q) component of the output signal.

In the system, the modulators **16** and **18** are performing 8-ary orthogonal keying or encoding because each receive 3 bits of information and chooses one out of 8 orthogonal codes. By having both I and Q components with different polarities, a total of 256 possible code combinations exist, so a total of 8 bits can be encoded into one orthogonal code. The code set in the 8-ary orthogonal keying system is based on eight (8) Walsh codes of 8 chips in length. Using the 8 chip Walsh codes in an M-ary orthogonal keying (MOK) system is advantageous because the 8 chip Walsh codes are orthogonal, which means they exhibit zero cross-correlation, so the 8 chip Walsh codes tend to be easily distinguishable from each other. However, using the 8 chip Walsh codes reduces the coding gain for the system of FIG. **1** to below **10**, and the United States Federal Communications Commission (FCC) requires a processing gain of at least 10 for transmission systems operating in the 2.4 GHz Industrial, Scientific and Medical (ISM) band. Processing gain can be simply measured by the number of chips per code symbol. For the MOK system to achieve a processing gain of at least 10, the code length should be at least 10 chips. However, if the MOK system is designed for code lengths of 10 chips or more, the data rate drops to less than 10 Mbps.

Another M-ary keying scheme encodes data bits using a Barker code (like used for the IEEE 802.11 standard for 1 and 2 Mbit/s). The operation is similar to the previously described MOK system with length 8 codes, except that the code length for the non-orthogonal Barker sequences is 11. By choosing one out of 8 time shifted Barker codes of length 11 chips for the in-phase and quadrature components and changing polarities, a total of 8 bits per symbol can be encoded. However, a symbol now consists of 11 chips instead of 8, so for the same chip rate the effective data rate is a factor 8/11 lower. This means that with code lengths of 10 chips or more, you cannot achieve a data rate of 10 Mbps or more as in the case of length 8 codes.

SUMMARY OF THE INVENTION

The present invention involves a digital (de)modulation system which uses a larger code set of M codes for N length codes, where M>N, to provide an increased data rate while maintaining the coding gain. For example, the system can use 16 different codes each having a length of 11 chips in a code set while the conventional M-ary keying systems use a code set size of 8 for 11-chip codes or 8-chip codes. By extending the code set size, the system increases the data rate of the system. With 16 codes and the ability to change the sign of the code to be transmitted, the system can encode 5 data bits on both I and Q, so a total of 10 data bits can be encoded per code symbol. In this embodiment, a code symbol contains an 11 chip code on an I modulation branch and an 11 chip code on a Q modulation branch. As such, using 11 chip codes and a chip rate of 11 Mhz, the system provides a data rate of 10 Mbps while conventional M-ary keying systems can only achieve 8 Mbps using the same code length and chip rate. By extending the code length, the processing gain is increased. The extended code set is not orthogonal, so a non-zero cross-correlation value results between the different codes of the code set. However, the resulting noise and multipath performance degradation can be kept small by choosing code sets with small cross-correlation values (nearly orthogonal). The magnitudes of both cross-correlation values and auto-correlation sidelobes should preferably be below half a code length. In some embodiments, the code set is derived from orthogonal codes which are modified to reduce the autocorrelation sidelobes associated with the orthogonal codes. In other embodiments, the code set is derived using a complementary code which provides low autocorrelation sidelobes and is modified to reduce the cross-correlation values between the codes.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects and advantages of the present invention may become apparent upon reading the following detailed description and upon reference to the drawings in which:

FIG. **1** shows a block diagram of a M-ary orthogonal keying (MOK) system using Walsh codes modified by a cover sequence (11111100);

FIG. **2** shows a block diagram of a digital modulation system using an extended code set according to the principles of the present invention;

FIG. **3** shows a block diagram of an embodiment of a digital modulation system using the digital modulation system of FIG. **2**;

FIG. **4** shows a block diagram of another embodiment of the digital modulation system which can be used as the fallback mode for the embodiment of FIG. **3**;

FIG. **5** shows a graphical comparison of packet error ratio versus E_b/N_0 in dB for the digital modulation systems of FIG. **3** and FIG. **4**;

FIG. **6** shows a graphical comparison of packet error ratio versus delay spread in nanoseconds (ns) for the embodiments of FIG. **3** and FIG. **4**;

FIG. **7** shows a block diagram of another embodiment using the digital modulation system according to certain principles of the present invention;

FIG. **8** shows a digital demodulator according to certain principles of the present invention;

FIG. **9** shows a demodulation system using the digital demodulator according to certain principles of the present invention; and

FIG. **10** shows another embodiment of a demodulation system using the digital demodulator according to the principles of the present invention.

DETAILED DESCRIPTION

Illustrative embodiments of the digital (de)modulation system to achieve higher data rates while providing acceptable autocorrelation sidelobes and cross-correlation values for a wireless communications system is described below. FIG. **2** shows a digital modulator **28** according to the principles of the present invention. In response to data bits forming a data symbol, the modulator **28** chooses a corresponding one of M codes of length N, where M represents an extended number of codes of length N when compared to conventional M-ary keying systems. In conventional M-ary keying systems, the number of possible codes M is not more than the code length N in chips. In the present invention, the number M of codes is always larger than the code length N. In some embodiments, the code set can be derived from orthogonal codes which are modified to reduce the autocorrelation sidelobes associated with the orthogonal codes,

and/or the code set is derived using a complementary code which provides low autocorrelation sidelobes and modified to reduce the cross-correlation properties of the code set.

For example, an extended code set is given below in Table 1 which derived using complementary Barker codes. Complementary Barker codes are discussed in Robert L. Frank, "Polyphase Complementary Codes." IEEE Transactions On Information Theory, Vol. IT-26, No. 6, November 1980, pp.641–647. In this particular embodiment, the code set in table 1 is based upon 2 codes, which are cyclically shifted. For example, a code of length 4, such as {1110} can be cyclically shifted by rotating the code to get three (3) other codes. If the code is shifted by one position to the right, the code {0111} is created. Two shifts give {1011 1}, and three (3) shifts give {1101}. In this particular embodiment, the two codes are cyclically shifted over 8 chips to get a total of 16 different codes. One of the 2 codes is actually the length 11 Barker sequence that is used in the current 2 Mbps IEEE 802.11 standardwhichis {1-111-1111-1-1-1}. Theothercode{1-1-1111111-11} is a code which gives low cross correlation with the Barker code set and low autocorrelation. The maximum autocorrelation value (when correlating with a non-zero shifted replica of itself) of the code set in table 1 is 2, while the maximum cross-correlation magnitude is 5.

TABLE 1

Code set based on cyclic shifted codes

1	-1	1	1	-1	1	1	1	-1	-1	-1
-1	1	-1	1	1	-1	1	1	1	-1	-1
-1	-1	1	-1	1	1	-1	1	1	1	-1
-1	-1	-1	1	-1	1	1	-1	1	1	1
1	-1	-1	-1	1	-1	1	1	-1	1	1
1	1	-1	-1	-	1	-1	1	1	-1	1
1	1	1	-1	-1	-1	1	-1	1	1	-1
-1	1	1	1	-1	-1	-1	1	-1	1	1
1	-1	-1	1	1	1	1	1	1	-1	1
1	1	-1	-1	1	1	1	1	1	1	-1
-1	1	1	-1	-1	1	1	1	1	1	1
1	-1	1	1	-1	-1	1	1	1	1	1
1	1	-1	1	1	-1	-1	1	1	1	1
1	1	1	-1	1	1	-1	-1	1	1	1
1	1	1	1	-1	1	1	-1	-1	1	1
1	1	1	1	1	-1	1	1	-1	-1	1

The code set of tables 2 and 3 are derived using modified orthogonal Walsh codes. For, example, in the code set of table 2, the first 8 codes are length 8 Walsh codes, extended with 3 ones to get a length of 11. Further, the 4^{th}, 7^{th} and 10^{th} chips are inverted. The second group of 8 codes is again the Walsh code set extended with 3 ones, but now the 4^{th}, 6^{th} and 11^{th} chips are inverted.

TABLE 2

Code set based on modified Walsh codes

1	1	1	-1	1	1	-1	1	1	-1	1
1	-1	1	1	1	-1	-1	-1	1	-1	1
1	1	-1	1	1	1	1	-1	1	-1	1
1	-1	-1	-1	1	-1	1	1	-1	1	1
1	1	1	-1	-1	-1	1	-1	1	-1	1
1	-1	1	1	-1	1	1	1	1	-1	1
1	1	-1	1	-1	-1	-1	1	1	-1	1
1	-1	-1	-1	1	-1	-1	-1	-1	1	1
1	1	1	-1	1	-1	1	1	1	1	-1
1	-1	1	1	1	1	1	-1	1	1	-1
1	1	-1	1	-1	1	-1	1	-1	1	-1
1	-1	-1	-1	-1	-1	1	1	-1	1	-1

TABLE 2-continued

Code set based on modified Walsh codes

1	-1	1	1	-1	-1	-1	1	1	1	-1
1	1	-1	1	-1	1	1	1	1	1	-1
1	-1	-1	-1	-1	-1	1	-1	1	1	-1

The code set of table 3 uses length 16 modified Walsh codes. This set has better cross correlation properties, than the set based on two cyclic shifted codes; the maximum cross correlation value is 3, versus 5 for the cyclic shifted case. This means that the signal-to-noise performance of the code set in table 3 will be slightly better. However, the cross-correlation values for delayed code words are worse than those of the cyclic shifted set, which means that the multipath performance is slightly worse. The set of table 3 was obtained by multiplying the length 16 Walsh code set by the length 16 complementary sequence {111-111-11111-1-1-11-1}. The length 16 codes were then reduced to length 11 codes by puncturing (i.e. removing) the 3^{rd}, 6^{th}, 9^{th}, 12^{th} and 15^{th} elements of the codes.

TABLE 3

Code set based on modified and punctured length 16 Walsh codes

1	1	-1	1	-1	1	1	1	-1	-1	-1
1	-1	1	1	-1	-1	-1	1	-1	1	1
1	1	1	1	1	-1	1	-1	-1	-1	1
1	-1	-1	1	1	1	-1	-1	-1	1	-1
1	1	-1	-1	1	-1	1	1	1	1	1
1	-1	1	-1	1	1	-1	1	1	-1	-1
1	1	1	-1	-1	1	1	-1	1	1	-1
1	-1	-1	-1	-1	-1	-1	-1	1	-1	1
1	1	-1	1	-1	1	-1	-1	1	1	1
1	-1	1	1	-1	-1	1	-1	1	-1	-1
1	1	1	1	1	-1	-1	1	1	1	-1
1	-1	-1	1	1	1	1	1	1	-1	1
1	1	-1	-1	1	-1	-1	-1	-1	-1	-1
1	-1	1	-1	1	1	1	-1	-1	1	1
1	1	1	-1	-1	1	-1	1	-1	-1	1
1	-1	-1	-1	-1	-1	1	1	-1	1	-1

The modulator **28** can perform the derivation of the extended code set(s) using processing circuitry implementing some logic to perform the derivation, or the modulator **28** can store the code set(s) in a look-up table. The modulator **28** can also store different sets of modified orthogonal codes depending on desired changes in operation or calculate different extended sets derived from different codes. In this embodiment, the data bits are shown as being received in parallel, and the code chips are shown as being produced serially. Depending on the application, the data bits can be received serially, and/or the code chips can be produced in parallel.

FIG. **3** shows an embodiment of a digital modulation system **30** using modulators **32** and **34** to produce one of 16 codes of length 11 chips in response to 4 information bits from the serial to parallel converter **14**. In MOK systems, the modulators respond to 3 information bits to produce one of eight (8) modified Walsh codes of length 8 chips. By using only 8 chip codes, the MOK systems fail to achieve a processing gain of 10 which is required by the FCC for the 2.4 GHz ISM band. To achieve the processing gain of 10, it is believed that at least 10 chips long codes should be used. That is why the length 11 Barker code is used in the current IEEE 802.11 standard for direct sequence spread-spectrum in the 2.4 GHz band. However, the system using 11 Barker codes is limited to 8 codes per set, thereby limiting the data rate.

In the operation of the embodiment of FIG. **3**, the scrambler **12** receives data and scrambles the data according to the IEEE 802.11 standard. In other embodiments, the scrambler **12** may not be necessary, and the data can be manipulated by some other form of data conversion, interleaving or modification, or the data can be fed directly into the serial-to-parallel converter **14**. In this embodiment, the serial-to-parallel converter **14** is a 1:10 multiplexer (MUX) which produces a data symbol of 10 data bits in parallel according to a 1 MHz clock signal. The ten bit data symbol is encoded into a I/Q code pair of 11 chip codes or codewords. Four (4) of the bits of the data symbol are provided to the first modulator **32** which produces a corresponding one of sixteen (16) length 11 codes from the extended code set according to the principles of the present invention. The first modulator **32** produces the length 11 code at a chip rate of about 11 MHz as dictated by an 11 MHz clock signal. In the above example, each symbol contains 10 data bits, which are encoded into independent I and Q codes of 11 chips. Chips are actually code bits, but they are called chips to distinguish them from data bits. In this embodiment, the first modulator **32** corresponds to the I phase modulation branch of the system **30** which produces the I component of the of the signal to be transmitted.

A second set of four (4) bits of the data symbol from the converter **14** is provided to the second modulator **34** which produces a corresponding one of 16 length 11 codes from the extended code set according to the principles of the present invention. The second modulator **34** corresponds to the Q phase modulation branch of the system **30** which produces the Q component of the of the signal to be transmitted. In response to the four data bits, the second modulator **34** also produces a length 11 code at a chip rate of about 11 MHz as dictated by the 11 MHz clock signal.

Of the remaining two of 10 bits of the data symbol from the serial to parallel converter **14**, one is provided to a first XOR gate **36**. If the bit is a 0, the first XOR gate **36** changes the polarity of the length 11 code from the first modulator **32**. The resulting code I_{out} is provided to signal circuitry **21** to change any 0's to −1's and perform any additional signal processing and/or conversion before being provided to the first mixer **24** to modulate a carrier of frequency ω. The last remaining bit is provided to a second XOR gate **38**. If the bit is a 0, the second XOR gate **38** changes the polarity of the length 11 Walsh code from the second modulator **34**. The resulting modified Walsh code Q_{out} is provided to the signal circuitry **23** for any conversion and/or processing before being provided to the second mixer **26** to modulate a 90 degree shifted version of the carrier with frequency ω. If instead of 0's, −1's are used, the first and second XOR gates **36** and **38**, can be replaced by multipliers to change the polarity of I_{out} and Q_{out}. Subsequently, the I_{out} modulated carrier and the Q_{out} modulated carrier are combined and transmitted. As such, this particular embodiment of the system **30** partitions 10 bits of incoming data into 5 bits for the I branch and 5 bits for the Q branch. Four data bits on the I branch are encoded into a code of 11 chips from the extended code set, and four data bits on the Q branch are encoded in parallel into one of 16 11-chip codes. Because the last two bits encode information by determining the polarity of the 11 chip codes respectively, the system **30** encodes 10 data bits into 2 codes which are both picked from a set of 32 possible codes. In this example, there are 16 codes, which can be inverted to get 32 codes. With a symbol rate of 1 MSps and 10 bits/symbol, the data rate for the system **30** is 10 MBps.

FIG. **4** shows an embodiment of a extended code digital modulation system **50** which can be used as a fallback mode for the system **30** (FIG. **3**). Once again, the input data is scrambled by the scrambler **12** according to the IEEE 802.11 standard. The data is provided to a serial to parallel converter **52**. The serial to parallel converter **52** in this embodiment produces 6 bit data symbols in parallel at a data symbol rate of 1 MSps. From the 6 bit data symbol, four bits are received by a modulator **54** which encodes the 4 bits into one of 16 length 11 codes according to the principles of the present invention. The length 11 code is provided to both I and Q branches **56** and **58**. In accordance with another inventive aspect of this particular embodiment, by providing the same code to multiple phase modulation paths or branches, this embodiment allows a fallback mode with independent phase modulation, such as quadrature phase shift keying (QPSK) or 8-phase shift keying (8-PSK), of the same code on the multiple phase modulation paths, such as the I and Q branches **56** and **58** in this embodiment. On the I branch **56**, the 11 chip code is serially provided to a first XOR gate **60**, and on the Q branch **58**, the 11 chip code is serially provided to a second XOR gate **62**. Of the two remaining bits from the serial to parallel converter **52**, one bit goes to the first XOR gate **60** to adjust the polarity of the length 11 code and produce I_{out} on the I branch **56**, and the other bit goes to the second XOR gate **62** to adjust the polarity of the length 11 code and produce Q_{out} on the Q branch **58**. Depending on the implementation, if −1's are used instead of 0's, the first and second XOR gates **60** and **62** can be replaced by multipliers. As such, given data symbols of 6 bits/symbol and a symbol rate of 1 MSps, this embodiment provides a data rate of 6 Mbps.

FIG. **5** graphically shows packet error rates versus E_b/N_o for the system **30** using 16 11 -chips codes. In fact, the E_b/N_o. requirement to get a certain packet error ratio is only half a dB worse than the 8 8-chip code set of the MOK system described in FIG. **1** using 8 length Walsh codes modified by a cover sequence of (11111100) as described in co-pending patent application Ser. No. 09/057,310 entitled "Digital Modulation System Using Modified Orthogonal Codes to Reduce Autocorrelation," filed on Apr. 8, 1998 and herein incorporated by reference. Curve **40** corresponds to a digital modulation system using 16 11 -chip codes at 6 Mbps, and curve **42** corresponds to a digital modulation system using 16 11 -chip codes at 10 Mbps. This shows that the 6 Mbps achieves 1.5 dB more gain than the 10 Mbps mode (curve **40** is about 1.5 dB to the left of curve **42**).

FIG. **6** graphically shows packet error ratio versus delay spread in ns for a digital modulation system using 16 codes of length 11 chips with different codes on I and Q at 10 Mbps (curve **63**) and using the same code on I and Q with QPSK at 6 Mbps (curve **65**). The channel model used has an exponentially decaying power delay profile and independent Rayleigh fading paths. FIG. **6** shows that the 10 Mbps mode can handle a delay spread of about 50 ns using only a 6 taps channel matched filter (or a 6 finger RAKE) as would be understood by one of ordinary skill in the art. In the fallback mode of 6 Mbps (same code on I and Q), a delay spread of about 200 ns can be tolerated.

FIG. **7** shows an embodiment of a digital modulation system **66** which can be used as a fallback mode for the system **30** (FIG. **3**). The input data is scrambled by the scrambler **12** according to the IEEE 802.11 standard. The scrambled data is provided to a serial to parallel converter **68**. The serial to parallel converter **68** in this embodiment produces 5 bit data symbols in parallel at a symbol rate of 1 MSps. From the 5 bit data symbol, four bits are received by a modulator **70** which encodes the 4 bits into one of 16 11-chip codes according to the principles of the present

invention. The modulator **70** serially produces the length 11 codes at a rate of 11 MHz. The length 11 code is provided to an XOR gate **72** corresponding to both the I and Q branches. The length 11 code is exclusive-ored by the remaining bit of the data symbol from the serial-to-parallel converter **68** to adjust the polarity of the length 11 code and produce I_{out} and Q_{out} in serial form. Depending on the implementation, if −1's are used instead of 0's, the XOR gate **72** can be replaced by a multiplier. As such, given data symbols of 5 bits/symbol and a symbol rate of 1 MSps, this embodiment provides a data rate of 5 Mbps.

FIG. **8** shows a digital demodulation system **76** which can be used at a receiver (not shown) to receive transmitted codes from a transmitter (not shown) using an embodiment of the digital modulation system described above. The digital demodulation system **76** receives one of 16 11-chip codes according to the principles of the present invention. In response to the code, the digital demodulation system produces a corresponding 4 data bits. Depending on the particular implementation, the code chips and/or the data bits can be in parallel or in series.

FIG. **9** shows a demodulation system **80** using the digital demodulation system according to the principles of the present invention. In this particular embodiment, the received signal is supplied to both I and Q branches **82** and **84** of the demodulation system **80**. A first mixer **86** multiplies the received signal by the cosωt, where ω is the carrier frequency, to extract the modulated I information, and a second mixer **88** multiplies the received signal by sin ωt to extract the modulated Q information. After low pass filtering, the I and Q information are provided to correlator blocks **90** and **92**, respectively. In this particular embodiment, the correlator blocks **90** and **92** each contain **16** correlators corresponding to the 16 codes in the code set for correlating time delayed versions of the I information and the Q information, respectively. The find code blocks **94** and **96** find the known codes according to the present invention which give the highest correlation magnitudes for the I and Q information. In certain embodiments, the demodulator **76** (FIG. **8**) or portions thereof can be performed in or receive the output from the find code blocks **94** and **96** to decode the known codes into corresponding data bits. Depending on the embodiment, the digital demodulation system **76** (FIG. **8**) or portions thereof can be implemented in the find code blocks **94** and **96**, in the detect polarity blocks **98** and **100**, branching off of the of the I and Q paths **82** and **84** and/or at the output of detect polarity blocks **98** and **100** to decode the codes to produce the corresponding data bits. In this embodiment, the detect polarity blocks **98** and **100** each decode an additional data bit from the polarity of the found code.

FIG. **10** shows an embodiment of a demodulation system **110** which can be used at the fallback rate for the demodulator system **80** (FIG. **9**) receiving code symbols from the modulator system **50** (FIG. **5**) where the same code is transmitted on multiple modulation paths. The difference between the demodulation system **110** and the full rate demodulation system of FIG. **9** is that the code detection block **112** adds the squared correlation outputs of the I and Q correlators **90** and **92** and detects the code according to the present invention which gave the highest correlation complex magnitude. In accordance with an inventive aspect of this particular embodiment, the same code is on both the I and Q paths **82** and **84** for digital demodulation. In this particular embodiment, a block **114** finds the code with the highest complex correlation magnitude. In certain embodiments, the demodulator **76** or portions thereof can be performed in or receive the output from the find code block **112** to decode the codes into corresponding data bits. Depending on the embodiment, the digital demodulation system **76** (FIG. **8**) or portions thereof can be implemented in the code detection block **112**, in a phase detector **114**, branching off of the path **115** and/or at the output of the phase detector **114** to decode the codes and produce the corresponding data bits. The phase detector **114** detects the phase of the complex correlation output to decode an extra **2** bits per code symbol for QPSK or an extra 3 bits per code symbol for 8-PSK.

In addition to the embodiment described above, alternative configurations of the digital (de)modulation system according to the principles of the present invention are possible which omit and/or add components and/or use variations or portions of the described system. For example, the above applications use a Quadrature Phase Shift Keying (QPSK) phase shift modulation scheme (FIGS. **1, 3, 4**) along with the digital (de)modulation scheme and a binary phase shift keying (BPSK) scheme (FIG. **6**), but the digital (de) modulation system can be used with other (de)modulation schemes, such as amplitude modulation including quadrature amplitude modulation (QAM) and other phase modulation schemes including 8-phase shift keying (8-PSK) as would be understood by one of ordinary skill in the art. Additionally, the digital (de)modulation system has been described as using codes of 1's and 0's which are modified by codes of 1's and 0's, but the digital (de)modulation system can be performed using codes of 1's and −1's or 1's and 0's depending on the embodiment. In the embodiments described above, codes of 1's and −1's are received at the receiver, and the correlation determinations are described in terms of 1's and −1's, but the (de)modulation system can use 1's and 0's or 1's and −1's depending on the embodiment. The (de)modulation system has also been specifically described as using extended code sets of 16 11-chip codes, but other extended code sets are possible according to the principles of the present invention.

Furthermore, the digital (de)modulation system has been described using a particular configuration of distinct components, but the digital (de)modulation system can be performed in different configurations and in conjunction with other processes. Additionally, the various components making up the digital (de)modulation system and their respective operating parameters and characteristics should be properly matched up with the operating environment to provide proper operation. It should also be understood that the digital (de)modulation system and portions thereof can be implemented in application specific integrated circuits, software-driven processing circuitry, firmware, lookup-tables or other arrangements of discrete components as would be understood by one of ordinary skill in the art with the benefit of this disclosure. What has been described is merely illustrative of the application of the principles of the present invention. Those skilled in the art will readily recognize that these and various other modifications, arrangements and methods can be made to the present invention without strictly following the exemplary applications illustrated and described herein and without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method for modulating information bits over a radio frequency communication channel, comprising:

grouping a number of information bits,

based on the grouping, selecting a code having N chips from a code set that includes M codes, wherein M>N, and wherein the code set is derived from a comple-

mentary code that provides autocorrelation sidelobes suitable for multipath environments, and

modulating the phase of at least one carrier signal in accordance with the selected code.

2. The method of claim **1** further including:

applying a phase shift to modulate at least one additional information bit on the at least one carrier signal.

3. The method of claim **2**, wherein the number of information bits is six and the number of additional information bits is two.

4. The method of claim **1**, wherein the phase of the at least one carrier signal is QPSK modulated in accordance with the selected code.

5. The method of claim **1** further including:

scrambling the information bits prior to grouping.

6. The method of claim **1**, wherein modulating the phase of at least one carrier signal includes In-phase and Quadrature phase modulating the at least one carrier signal.

7. The method according to claim **1**, wherein the complementary code has a length of 2^X chips where X is a positive integer.

8. The method according to claim **1**, wherein the code set is stored in a look-up table.

9. The method according to claim **1**, wherein the complementary code provides for autocorrelation sidelobes in the code set which are equal to or less than one-half the length of the N chip code.

10. A method for modulating information bits over a radio frequency communication channel, comprising:

grouping a number of information bits,

based on the grouping, selecting a code having N chips from a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code, and

modulating the phase of at least one carrier signal in accordance with the selected code,

wherein the complementary code is defined by the sequence ABAB', such that A is a sequence of elements and B is a sequence of elements and wherein B' is derived by inverting all elements in the sequence B.

11. The method according to claim **10**, wherein A={11} and B={10} such that the sequence ABAB'={11101101}.

12. A method for modulating information bits over a radio frequency communication channel, comprising:

grouping a number of information bits,

based on the grouping, selecting a code having N chips from a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code, and

modulating the phase of at least one carrier signal in accordance with the selected code,

wherein the complementary code is characterized by the property that for shifts in the complementary code, the autocorrelation of the complementary codes sum to zero except for the main peak at zero shift.

13. A method for demodulating a received signal that conveys information bits over a radio frequency communication channel, comprising:

correlating the received signal against a code set that includes M codes, each code having N chips wherein M>N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments, and

decoding the information bits based upon the correlating step.

14. The method according to claim **13**, wherein the complementary code has a length of 2^X chips where X is a positive integer.

15. The method according to claim **13**, wherein the complementary code provides for autocorrelation sidelobes in the code set which are equal to or less than one-half the length of the N chip code.

16. The method according to claim **13**, wherein the decoding step decodes the information bits based upon the highest correlation magnitudes from the correlation step.

17. The method according to claim **13**, wherein the decoding step decodes the information bits based upon the highest correlation complex magnitude from the correlation step.

18. The method according to claim **13**, further comprising:

detecting the phase of the code in the code set that generates the highest correlation magnitude, and

decoding at least one bit per code based upon the detected phase.

19. A method for demodulating a received signal that conveys information bits over a radio frequency communication channel, comprising:

correlating the received signal against a code set that includes M codes, each code having N chips wherein M>N, and wherein the code set is derived from a complementary code, and

decoding the information bits based upon the correlating step,

wherein the complementary code is defined by the sequence ABAB', such that A is a sequence of elements and B is a sequence of elements and wherein B' is derived by inverting all elements in the sequence B.

20. The method according to claim **19**, wherein A={11} and B={10} such that the sequence ABAB'={111011101}.

21. A method for demodulating a received signal that conveys information bits over a radio frequency communication channel, comprising:

correlating the received signal against a code set that includes M codes, each code having N chips wherein M>N, and wherein the code set is derived from a complementary code, and

decoding the information bits based upon the correlating step,

wherein the complementary code is characterized by the property that for shifts in the complementary code the autocorrelations of the complementary codes sum to zero except for the main peak at zero shift.

22. A digital modulation system for modulating data bits, comprising:

a serial-to-parallel converter that groups the data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments.

23. The digital modulation system according to claim **22**, further comprising a mixer that modulates a carrier signal in accordance with the chosen code.

24. The digital modulation system according to claim **23**, wherein the mixer modulates the phase of at least one carrier signal in accordance with the selected code.

25. The digital modulation system according to claim **24**, wherein the phase of the at least one carrier signal is QPSK modulated in accordance with the selected code.

26. The digital modulation system according to claim 22, further comprising a scrambler for scrambling the group of data bits.

27. The digital modulation system according to claim 22, further comprising a look-up table for storing the code set.

28. The digital modulation system according to claim 22, wherein the complementary code provides for autocorrelation sidelobes in the code set which are equal to or less than one-half the length of the N chip code.

29. A digital modulation system for modulating data bits, comprising:

a serial-to-parallel converter that groups the data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is defined by the sequence ABAB', such that A is a sequence of elements and B is a sequence of elements and wherein B' is derived by inverting all elements in the sequence B.

30. The digital modulation system according to claim 29, wherein A={11} and B={10} such that the sequence ABAB'={11101101}.

31. A digital modulation system for modulating data bits, comprising:

a serial-to-parallel converter that groups the data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is characterized by the property that for shifts in the complementary code, the autocorrelations of the complementary codes sum to zero except for the main peak at zero shift.

32. A digital modulation system for modulating a group of data bits, comprising:

a scrambler for scrambling the group of data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M >N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments.

33. The digital modulation system according to claim 32, further comprising a look-up table for storing the code set.

34. The digital modulation system according to claim 32, wherein the complementary code provides for autocorrelation sidelobes in the code set which are equal to or less than one-half the length of the N chip code.

35. A digital modulation system for modulating a group of data bits, comprising:

a scrambler for scrambling the group of data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is defined by the sequence ABAB', such that A is a sequence of elements and B is a sequence of elements and wherein B' is derived by inverting all elements in the sequence B.

36. The digital modulation system according to claim 35, wherein A={11} and B={10} such that the sequence ABAB'={11101101}.

37. A digital modulation system for modulating a group of data bits, comprising:

a scrambler for scrambling the group of data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is characterized by the property that for shifts in the complementary code, the autocorrelations of the complementary codes sum to zero except for the main peak at zero shift.

38. A digital modulation system for modulating data bits, comprising:

a serial-to-parallel converter that groups the data bits, and

modulation means for choosing a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments.

39. The digital modulation system according to claim 38, further comprising mixing means for modulating a carrier signal in accordance with the chosen code.

40. The digital modulation system according to claim 38, further comprising a scrambling means for scrambling the group of data bits.

41. The digital modulation system according to claim 38, wherein the complementary code provides for autocorrelation sidelobes in the code set which are equal to or less than one-half the length of the N chip code.

42. A digital modulation system for modulating data bits, comprising;

a serial-to-parallel converter that groups the data bits, and

modulation means for choosing a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is defined by the sequence ABAB', such that A is a sequence of elements and B is a sequence of elements and wherein B' is derived by inverting all elements in the sequence B.

43. A digital modulation system for modulating data bits, comprising:

a serial-to-parallel converter that groups the data bits, and

modulation means for choosing a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is character by the property that for shits in the complementary code, the autocorrelations of the complementary codes sum to zero except for the main peak at zero shift.

44. A digital demodulator for demodulating a received signal that conveys information bits over a radio frequency communication channel, comprising:

a correlator block for correlating the received signal against a code set that includes M codes, each code having N chips wherein M>N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments, and

a find code block for decoding the information bits based upon the correlations of the received signal and the code set.

45. The digital demodulator according to claim 44, wherein the complementary code provides for autocorrelation sidelobes in the code set which are equal to or less than one-half the length of the N chip code.

46. The digital demodulator according to claim 44, further comprising a phase detector that detects the phase of the code in the code set that generates the highest correlation magnitude and that decodes an extra 2 bits per code based upon the detected phase.

47. A digital demodulator for demodulating a received signal that conveys information bits over a radio frequency communication channel, comprising:

a correlator block for correlating the received signal against a code set that includes M codes, each code having N chips wherein M>N, and wherein the code set is derived from a complementary code, and

a find code block for decoding the information bits based upon the correlations of the received signal and the code set,

wherein the complementary code is defined by the sequence ABAB', such that A is a sequence of elements and B is a sequence of elements and wherein B' is derived by inverting all elements in the sequence B.

48. The digital demodulator according to claim 47, wherein A={11} and B={10} such that the sequence ABAB'={11101101}.

49. A digital demodulator for demodulating a received signal that conveys information bits over a radio frequency communication channel, comprising:

a correlator block for correlating the received signal against a code set that includes M codes, each code having N chips wherein M>N, and wherein the code set is derived from a complementary code, and

a find code block for decoding the information bits based upon the correlations of the received signal and the code set,

wherein the complementary code is characterized by the property that for shifts in the complementary code the autocorrelations of the complementary codes sum to zero except for the main peak at zero shift.

* * * * *

EXHIBIT D

US006707867B2

(12) **United States Patent**
Diepstraten et al.

(10) **Patent No.: US 6,707,867 B2**
(45) **Date of Patent: Mar. 16, 2004**

(54) **WIRELESS LOCAL AREA NETWORK APPARATUS**

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(73) Assignee: **Agere Systems, Inc.**, Allentown, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 93 days.

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(22) Filed: **Mar. 7, 2002**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **H04L 7/00**; H04J 3/06

(52) **U.S. Cl.** **375/354**; 375/356; 370/503

(58) **Field of Search** 375/354, 356, 375/362–366, 371; 370/503, 508, 509, 510, 511, 512, 513, 514

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Primary Examiner—Tesfaldet Bocure
(74) *Attorney, Agent, or Firm*—Harness, Dickey & Pierce, P.L.C.

(57) **ABSTRACT**

A wireless local area network apparatus includes a transmitter and a receiver in which operation of the receiver is accurately synchronized with periodic signals from the transmitter. The periodic signals contain timing data indicating the state of a timer in the transmitter at the time the signal containing that data was transmitted and this timing data is retrieved from the signal when received by the receiver and loaded in a timer for controlling operation of the receiver.

74 Claims, 4 Drawing Sheets

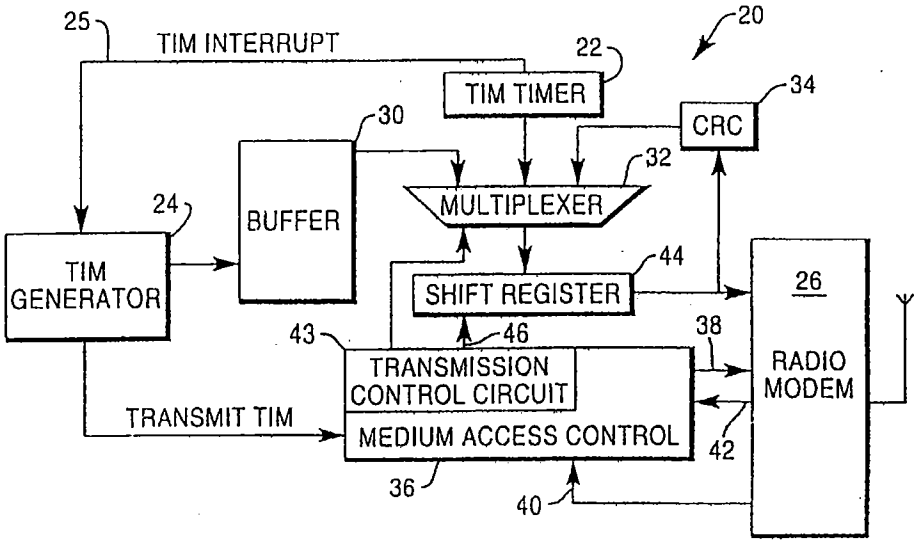


FIG. 1

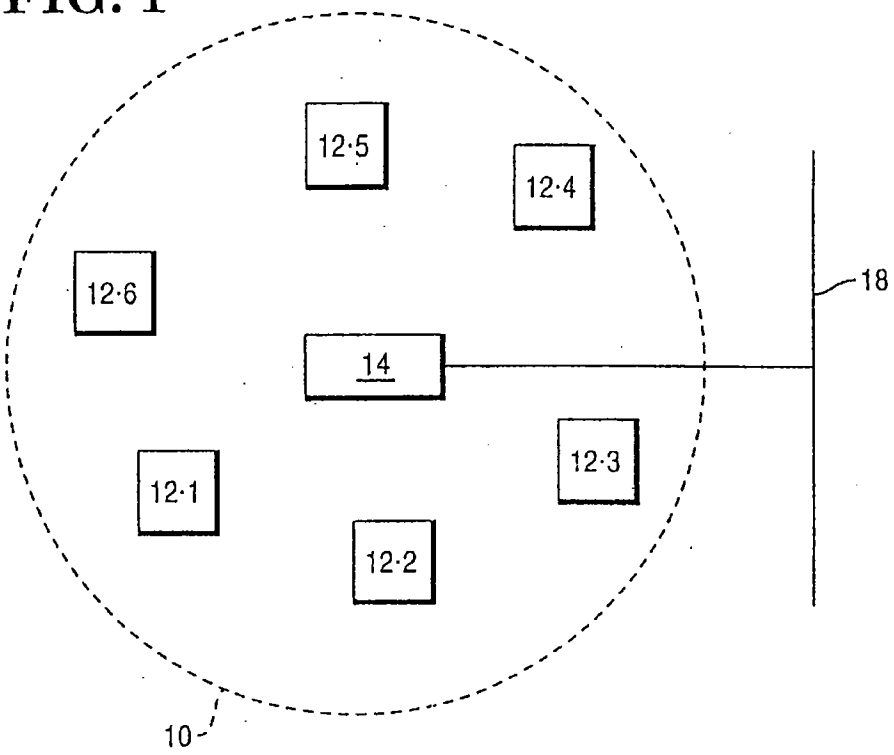
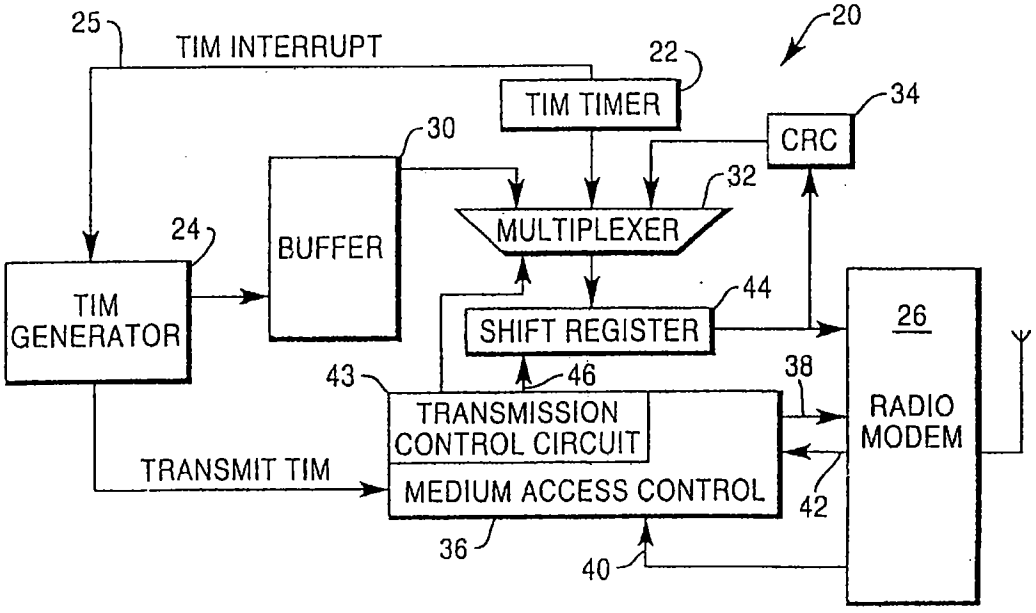

12·5
12·4
12·6
18
14
12·3
12·1
12·2
10

FIG. 2


25
TIM INTERRUPT
22
20
TIM TIMER
34
CRC
30
32
MULTIPLEXER
24
BUFFER
TIM GENERATOR
44
SHIFT REGISTER
26
43
46
38
TRANSMISSION CONTROL CIRCUIT
RADIO MODEM
TRANSMIT TIM
MEDIUM ACCESS CONTROL
42
36
40

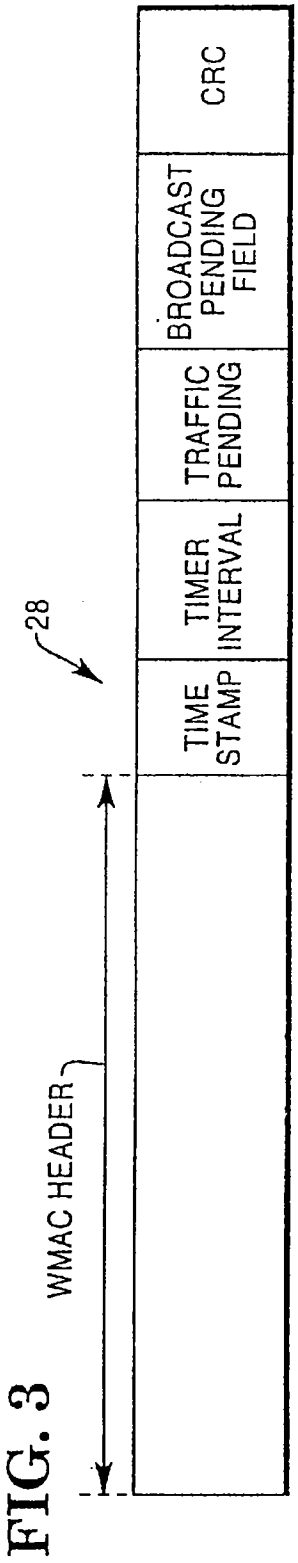

28
WMAC HEADER
TIME STAMP
TIMER INTERVAL
TRAFFIC PENDING
BROADCAST PENDING FIELD
CRC

FIG. 3

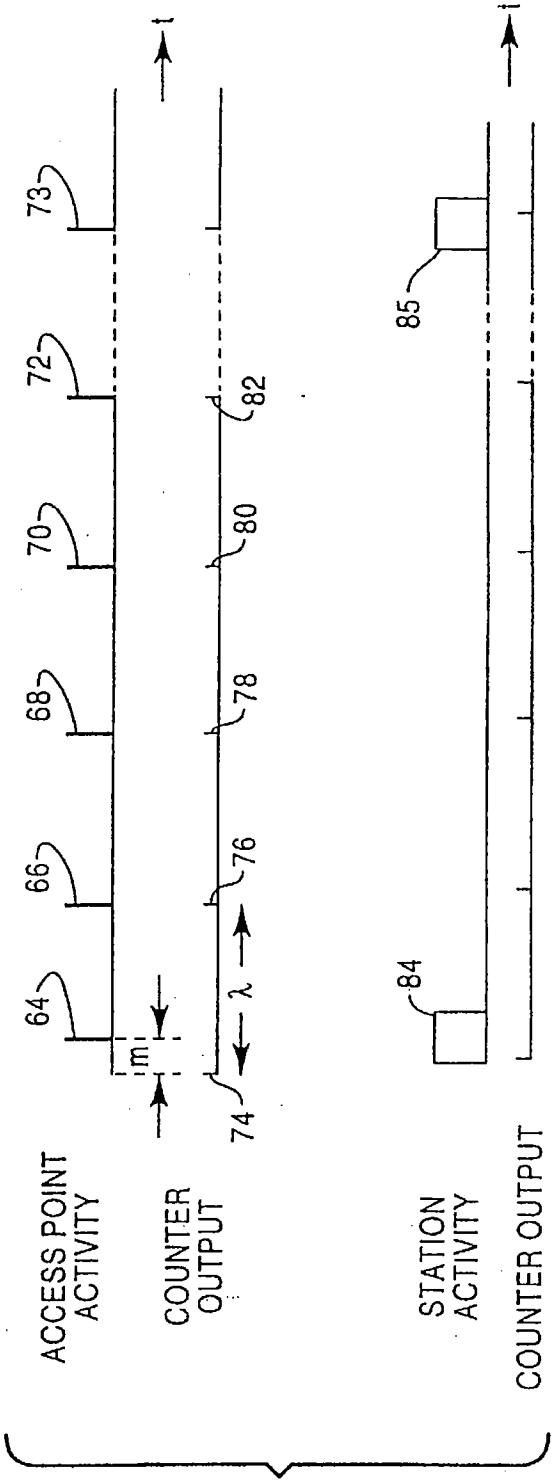

ACCESS POINT ACTIVITY
COUNTER OUTPUT
STATION ACTIVITY
COUNTER OUTPUT
t
64
66
68
70
72
73
74
76
78
80
82
84
85
m
λ

FIG. 7

FIG. 4

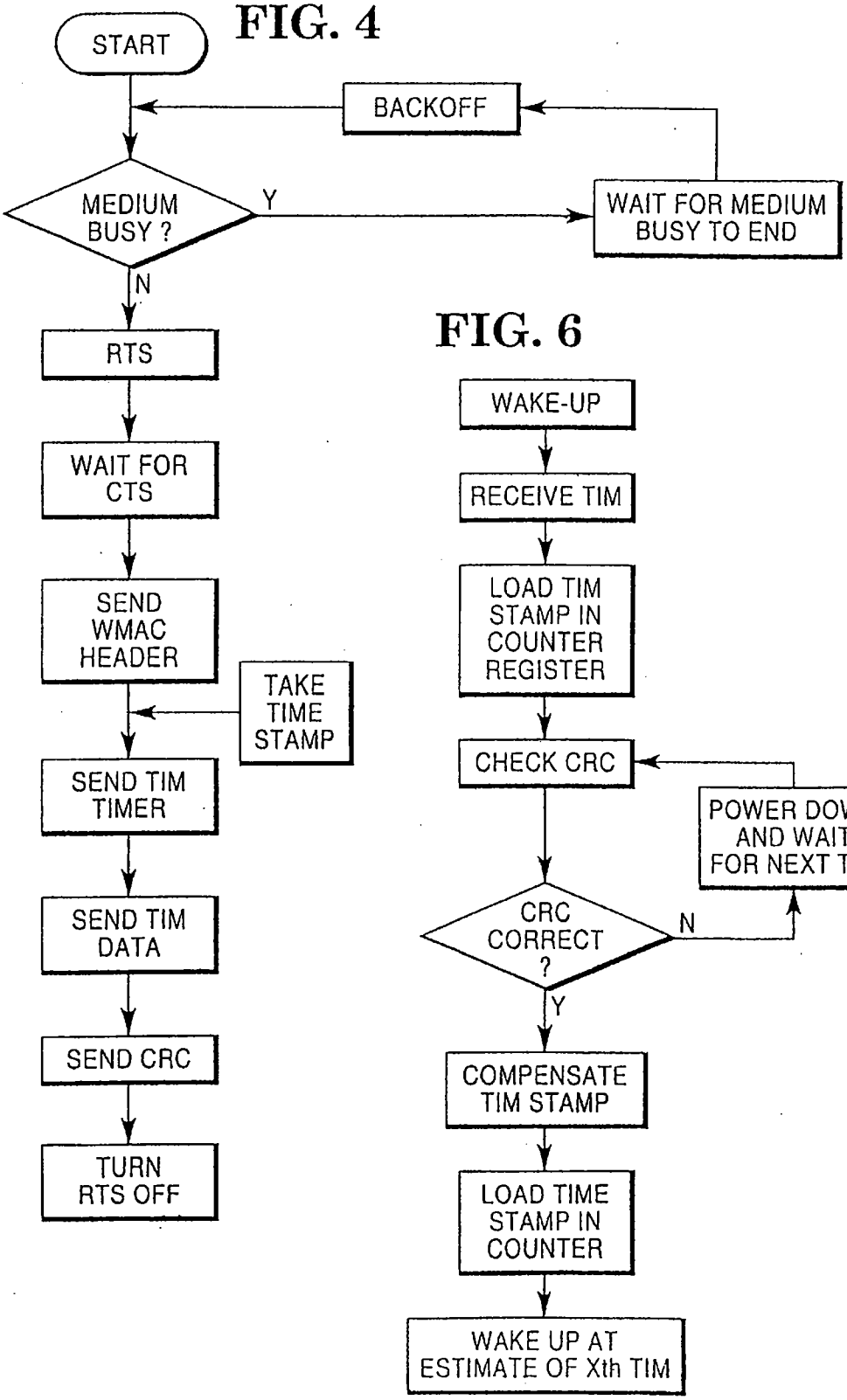

START
BACKOFF
MEDIUM BUSY ?
Y
WAIT FOR MEDIUM BUSY TO END
N
RTS
WAIT FOR CTS
SEND WMAC HEADER
TAKE TIME STAMP
SEND TIM TIMER
SEND TIM DATA
SEND CRC
TURN RTS OFF

FIG. 6

WAKE-UP
RECEIVE TIM
LOAD TIM STAMP IN COUNTER REGISTER
CHECK CRC
POWER DOWN AND WAIT FOR NEXT TIM
CRC CORRECT ?
N
Y
COMPENSATE TIM STAMP
LOAD TIME STAMP IN COUNTER
WAKE UP AT ESTIMATE OF Xth TIM

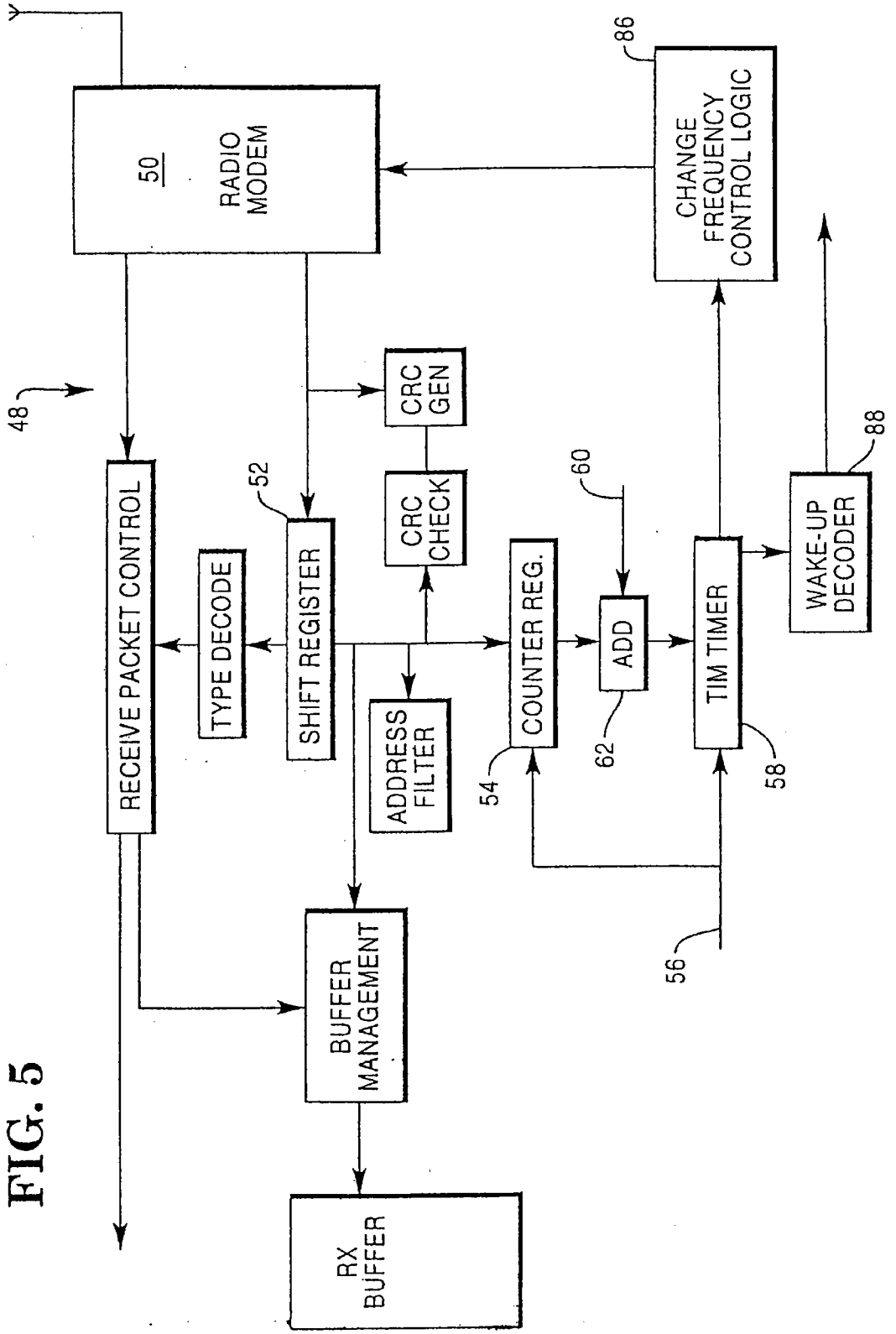

50
RADIO MODEM
86
CHANGE FREQUENCY CONTROL LOGIC
48
CRC GEN
CRC CHECK
52
60
88
WAKE-UP DECODER
RECEIVE PACKET CONTROL
TYPE DECODE
SHIFT REGISTER
COUNTER REG.
ADD
TIM TIMER
ADDRESS FILTER
54
62
58
56
BUFFER MANAGEMENT
RX BUFFER

FIG. 5

WIRELESS LOCAL AREA NETWORK APPARATUS

This is a continuation of application Ser. No. 08/155,661 filed on Nov. 22, 1993.

BACKGROUND OF THE INVENTION

The present invention relates to wireless local area network apparatus.

A wireless local area network commonly comprises a plurality of communication stations located in a Basic Service Area (BSA). The stations can send and receive communication signals via a base station and, in this manner, the base station receives the signals from a station in the BSA and re-transmits the signals to the intended recipient station.

The BSA can be provided as one of a plurality of BSAs which together form an Extended Service Area. In this case, the base station of each BSA may comprise an access point for a backbone infrastructure for connecting the BSAs for allowing communication between stations in different BSAs within the Extended Service Area.

Communication between stations, whether by way of a base station or otherwise, can require synchronization between a transmitter of one station or an access point and a receiver of another station. Disadvantageously, accurate synchronization between a transmitter and a receiver in a BSA cannot be readily achieved due, in particular, to operational limitations such as transmission and reception delays and delays in accessing the wireless medium.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide wireless local area network apparatus having improved synchronization between the transmitters and the receivers in the network.

According to the present invention there is provided wireless local area network apparatus comprising transmitter means and receiver means, characterized in that said transmitter means includes transmitter timer means for controlling periodic generation of transmission signals, said receiver means includes receiver timer means, and said transmitter means has means for including transmitter timer data in said signals for synchronizing said receiver timer means with said transmitter timer means, said transmitter timer data representing the state of said transmitter timer means at the time of transmission of the signal in which it is included.

The wireless local area network apparatus of the present invention is particularly advantageous for power management applications in which low power portable wireless stations are employed in the BSA. The stations periodically switch between a low power consumption state, in which their transceivers are de-energized, and a high power consumption state, in which their transceivers are energized, and can thereby receive periodic signals transmitted from some other station. The synchronization between the signals transmitted from some other station and the switching of the power-consumption state of the receiver stations is advantageously achieved by the apparatus of the present invention. The improved synchronization of the present invention allows for operation of the stations in a wireless local area network with reduced power-consumption, which is particularly important for stations having an on-board power supply.

The apparatus of the present invention can be advantageously employed to control other timing relationships between a transmitter and a receiver in a wireless local area network. For example, in so-called frequency-hopping devices, the transmission frequency employed by a transmitter is periodically changed and so a receiver has to adapt to this change in communication-signal frequency. The apparatus of the present invention allows for accurate synchronization between the operational changes in the transmitter and receiver during such frequency hopping.

BRIEF DESCRIPTION OF THE DRAWINGS

One embodiment of the invention is described further hereinafter, with reference to the accompanying drawings in which:

FIG. **1** shows a wireless local area network which forms part of an extended service area;

FIG. **2** is a block diagram of a transmitter for use in apparatus embodying the present invention;

FIG. **3** shows the structure of a Traffic Indication Message constructed in the transmitter of FIG. **2**;

FIG. **4** is a flow diagram of the operation of the transmitter of FIG. **2**;

FIG. **5** is a block diagram of a receiver for use in apparatus embodying the present invention;

FIG. **6** is a flow diagram of the operation of the receiver of FIG. **5**; and

FIG. **7** is a timing diagram illustrating operation of the transmitter of FIG. **2** and the receiver of FIG. **5**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the invention is susceptible to various modifications and alternative forms, a specific embodiment thereof has been shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that it is not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

As mentioned above, the apparatus of the present invention can be used in a power management system for a wireless local area network.

Such a local area network is shown in FIG. **1** and comprises a basic service area (BSA) **10** having six mobile stations **12.1–12.6** located therein. In the illustrated embodiment each of the stations **12.1–12.6** is powered by an on-board d.c. supply (not shown) although some of the stations could be supplied by connection to an a.c. source. An access point **14** is also located in the BSA **10** and is typically connected to an a.c. power supply (not shown) and is connected to a backbone structure **18** linking the access point **14** to access points of other BSAs (not shown). The stations **12.1–12.6** communicate with each other via the access point **14**. Thus, a communication signal from one station **12.1** to another station **12.2** will not be received directly by the station **12.2** but will first be received by the access point **14** and then transmitted to the station **12.2**.

In order to reduce the power consumption of the stations **12.1–12.6**, and thereby increase the operational life-time before the on-board d.c. power supply needs to be recharged or replaced, the stations **12.1–12.6** are operated in a power-save-mode in which their transceivers are periodically

de-energized and the station is then in a so-called doze state. In order to operate the station **12.1–12.6** in a power-save-mode without losing any transmitted data packets, a data packet that is intended for a station that is in a doze state is buffered in the access point **14** until such time as the station wakes-up from its doze state into a so-called awake state and energizes its transceiver to receive the buffered data.

Traffic Indication Message (TIM) packets are transmitted at regular intervals from the access point **14** and indicate for which stations **12.1–12.6** in the BSA **10** data packets are buffered in the access point **14**. The transceivers in the stations **12.1–12.6** are periodically energized at regular intervals such that the stations **12.1–12.6** wake up from a doze state to receive the TIM packets transmitted by the access point **14**. If a TIM packet received indicates that a data packet is buffered in the access point **14** for one of the stations **12.1–12.6**, the transceiver of that station either waits to receive the data packet which is arranged to automatically follow the TIM packet, or the station transmits a poll packet to the access point **14** to request that the data packet be transmitted. In both of the above situations, the transceiver in the station remains in an energized state once it has received a TIM packet indicating that data is buffered for that station. Once the data packet has been received, the station returns to a doze state until it awakes to receive another TIM packet.

Accordingly, with the exception of the periodic waking to receive the TIM packets, a station **12.1–12.6** remains in a power saving doze state unless a TIM packet indicates a data packet is buffered for that station. In this manner, the power consumption of each station **12.1–12.6** is reduced and the operational life-time, i.e. the time before recharging or replacement of the d.c. power source is necessary, of the station is increased. The improved synchronization provided by the present invention provides for improved synchronization between the access point **14** and the stations **12.1–12.6** operating in a power-save mode so as to achieve advantageously reduced power consumption in the stations **12.1–12.6**.

Further power consumption reductions can be achieved by operation of the stations **12.1–12.6** in a so-called extended-power-save mode. The improved synchronization provided by the present invention advantageously supports operation of the stations **12.1–12.6** in the extended-power-save mode. In this mode, the station is controlled to wake up from a doze state to receive only every xth TIM packet transmitted by the access point **14**. For example, if x=150 then the station awakes to receive only every 150th TIM packet transmitted by the access point **14** and so the station remains in a doze state for a longer period than if it wakes to receive every TIM packet transmitted by the access point **14**. Power consumption in the station is thereby further reduced. Since, in the above example, a station awakes only every 150 TIM packets, accurate synchronization between the access point **14** and the station is required so that the station wakes up at an appropriate time to receive every 150th TIM packet. The present invention provides for such accurate synchronization.

It should be noted that although the access point **14** may have a data packet buffered therein to transmit to a station operating in an extended-power-save mode, the data packet remains buffered in the access point **14** until the station **12** wakes up upon receipt of the xth TIM packet after which the station will poll the access point **14** to transmit the buffered packet and so data is not lost.

The energization of the transceivers in the stations **12.1–12.6** and in the access point **14** can be controlled by timers which include crystal oscillators. Synchronization between the timers in the stations **12.1–12.6** and the access point **14** is achieved by apparatus embodying the present invention and an indication of the reduced power consumption of a station having such a timer and operating in an extended-power-save mode is given below in which:

The time interval between successive TIM packets transmitted from the access point **14** is 200 msec; the station's transceiver has a power-up delay of 1 msec; the timing drift of the oscillator in the station is 100 micro sec/sec; the timing drift of the oscillator in the access point **14** is 100 micro sec/sec; the TIM packet medium access delay is between 0 and 5 msec; and the station is required to wake up to receive every 150th TIM packet from the access point **14**.

Using the above values as examples:

$$\text{The station doze interval} = 150 \times 200\,\text{msec} = 30\,\text{sec}$$

The maximum drift of each oscillator in the

$$\text{doze interval} = 100\ \text{micro sec/sec} \times 30 = 3\,\text{msec}$$

The maximum drift for both oscillators therefore =6 msec

Thus, in view of the station's 1 msec power-up delay, the station should wake up 7 msec before the expected TIM packet to compensate for the oscillator drift and the power-up delay.

With a TIM access delay of 5 msec as an example, the period during which the station is in an awake state to receive a TIM packet is between 1 msec (when there is no crystal drift and the TIM access delay is 0 msec) and 1 msec+6 msec+5 msec=12 msec (when the total crystal drift is experienced and the TIM interval delay is 5 msec).

Assuming that the TIM packet has a duration of 0.5 msec, the average duration of the awake state of the station is 1+½+½+0.5=7 msec.

Thus, in this example, the station will be in an awake state, i.e., with its transceiver energized, for, on average, only 7 msec every 30 sec which provides for a particularly advantageous power consumption reduction.

By way of comparison, and assuming the same values as above, if the station wakes-up at every TIM, thereby requiring an average "on-time" of 1+½=3.5 msec per 200 msec TIM interval, the station is then awake for 525 msec every 30 sec.

FIG. **2** illustrates a transmitter **20** for use in the access point **14**. The transmitter **20** includes a modulo n counter **22** which, in operation, is free running and synchronized with a similar modulo n counter **58** in a station's receiver (see FIG. **5**).

The modulo n counter **22** functions as a timer and when the count value reaches n, a TIM function generator **24** is triggered by way of an interrupt signal **25** indicating that the next TIM packet should be constructed, and transmitted by way of a radio modem **26**.

The TIM packet **28** is constructed in a transmitter buffer **30** and an example of a TIM packet is illustrated in FIG. **3**. The TIM packet comprises a wireless medium access (WMAC) header and a data field format. The WMAC header includes, amongst other fields, a Type field that identifies the packet as a TIM packet.

The data field format includes:

A TIME STAMP FIELD in which is loaded a so-called time stamp of the value of the modulo n counter in the transmitter **20** at the time of transmission of the TIM;

A TIMER INTERVAL FIELD which indicates the value of n of the modulo n counter in the transmitter **20**;

A TRAFFIC PENDING FIELD which indicates for which stations data packets are buffered; and

A TRAFFIC BROADCAST PENDING FIELD which indicates the number of outstanding broadcast data packets buffered for the stations.

Referring again to FIG. **2**, once the TIM packet **28** has been constructed, it is delivered to a multiplexer **32** where the time stamp, and cyclic redundancy check (CRC) data from a CRC generator **34**, are loaded into the TIM packet **28**. A WMAC control **36** controls access to the medium via the modem **26** so that the TIM packet **28** is not transmitted from the access point **14** immediately upon generation of the interrupt signal **25**. The WMAC control **36** follows a medium access protocol such as Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). According to the CSMA/CA protocol, the energy level on the wireless medium is sensed by the modem **26** to determine if there is any existing network activity, and if the sensed energy level is above a threshold value, a medium busy signal **40** is delivered from the modem **26** to the WMAC Control **36**. If no medium busy is issued, so the medium is sensed "free", the WMAC control **36** turns on the transmitter of the modem **26** by issuing a request to send (RTS) signal. The modem **26** will then start to send a training sequence and will issue a clear-to-send signal (CTS) once the training sequence is complete. The modem **26** then sends the serialized data that arrives from the buffer via the multiplexer **32** and a shift register **44**. If the medium is sensed as "busy", the WMAC control **36** waits until the medium becomes free and then generates a random backoff delay after which the medium is again sensed. If the medium is sensed as "free" at this point then the control **36** follows the RTS, CTS procedure above.

When accessing the medium and once the training sequence has ended, the modem **26** provides the CTS **42** and the TIM packet stored in the buffer **30** is loaded into the shift register **44** via the multiplexer **32**. Once transmission of the header has started, the time stamp is loaded from the timer **22** into the shift register **44** via the multiplexer **32** and under the control of a transmit control circuit **43** in the WMAC control **36**. The transmit control circuit **43** also controls the start of the transmission of the header. As mentioned above, the modulo n counter **22** in the access point **14** of transmitter **20** is free running and so by the time the CSMA/CA protocol has been completed, and particularly if a medium busy signal **40** was received by the WMAC control **36**, the counter **22** is already into its next count sequence, i.e. at a value between 0 and n, by the time that the clear-to-send signal **42** is received by the WMAC control **36**. At a predetermined time relative to the clear-to-send signal **42**, which predetermined time is an accurate estimation of the exact time at which the TIM packet will be transmitted having regard to delays in the modem **26**, the so-called "time stamp" i.e. the value of the modulo n counter **22** at that predetermined time, will be loaded in the TIM packet **28** stored in the buffer **30**. The TIM packet **28** is loaded into a shift register **44** upon generation of a load signal **46** from the WMAC control **36**, and then transmitted by way of the modem **26**.

FIG. **4** further illustrates the operation of the transmitter **20** outlined above.

FIG. **5** illustrates a receiver **48** of one of the stations **12.1**–**12.6** in the BSA which is arranged to receive a TIM packet **28** and a data packet (not shown) from the access point **14**.

The operation of the receiver **48** is outlined below and further illustrated in FIG. **6**.

Energization of the receiver **48** is controlled by a modulo n counter **58** which functions as a timer to wake up the station **12.1** from a doze state to receive the TIM packet **28** transmitted from the access point **14**.

The TIM packet **28** is received by a receiver modem **50** and its time stamp value retrieved from the TIM TIME STAMP FIELD (FIG. **3**). The retrieved time stamp is delivered by way of a shift register **52** to a counter register **54** which commences a modulo n count starting from the point between 0 and n which corresponds to the time stamp value. The counter register **54** continues its modulo n count with the same clock signal **56** that controls the modulo n counter **58**. This modulo n count is stored in the counter register **54** until the TIM packet **28** is completely received and the CRC data checked. If the CRC is correct, the modulo n count is loaded from the counter register **54** into the modulo n counter **58**. The use of the counter register **54** is particularly advantageous in that it allows TIM packets of different lengths to be received. This arises since the modulo n count sequence, that commences at the time stamp value, is buffered in the register **54** while the TIM packet **28** is processed completely. The counter register **54** maintains the cyclic modulo n count for as long as is necessary to process the TIM packet.

If all the TIM packets are of the same known length, then a TIM-packet-processing compensation factor could be applied to the time stamp value to allow for the known time taken to process the TIM packet of known length. The compensated time stamp value would then be loaded directly into the modulo n counter **58** and so the intermediate counter register **54** would not be required.

Referring again to the embodiment illustrated in FIG. **5**, a delay compensation value **60** is added to the modulo n count by an adder **62** as the count is transferred from the counter register **54** to the modulo n counter **58**. The compensation value **60** compensates for the propagation delay of the receiver **48** and the transmitter **20**. Once the compensated modulo n counter value is transferred from the counter register **54** to the counter **58**, the counter **58** is then accurately synchronized with the modulo n counter **22** in the transmitter (FIG. **2**).

Once the modulo n counters **22**, **58** in the station **12.1** and the access point **14** are accurately synchronized, the counter **58** provides the station **12.1** with an accurate indication of the time at which the counter **22** in the access point **14** reaches its n value and generates a TIM packet for transmission. Since the counter **22** in the access point **14** remains free-running, and the counter **58** in the station **12.1** is accurately synchronized with the counter **22**, the station **12.1** can be controlled to accurately wake up in time to receive only every xth TIM packet without requiring the station **12.1** to wake up unnecessarily early as would be required to assure receipt of the TIM packet if accurate synchronization between the counters **22**, **58** was not available. The reduction in the need for early wake up of the station **12.1** advantageously reduces the power consumption of the station **12.1**.

It should be noted that each station **12.1**–**12.6** in the BSA **10** can operate with different doze intervals. For example one of the stations **12.1** can be controlled to wake up every 150 TIM packets while another station **12.2** wakes up every 200 TIM packets. Each time the station **12.1** wakes up to receive a TIM packet, the modulo n counter **58** is reset by the time stamp retrieved from the TIM packet so that continued accurate synchronization can be achieved.

FIG. **7** is a timing diagram that further illustrates the improved synchronization of the present invention as pro-

vided in a power management application. The access point **14** activity indicates the transmission of the first five TIM packets **64–72**, and the last TIM packet **73**, of a one hundred and fifty TIM packet series and the first five TIM generation signals **74–82** generated each time the modulo n counter **22** in the access point **14** reaches its value n. As shown, the transmission of the first TIM packet **64** is delayed due to a medium busy signal obtained from the CSMA/CA protocol. The first TIM packet **64** is therefore actually transmitted m counts of modulo n counter **22** into the first count sequence **74–76**. The station **12.1** has previously been synchronized to wake up at **84** to receive the first TIM packet **64**. The TIM packet **64** carries a time stamp value m representing the value of the modulo n counter **22** in the access point **14** at the actual time of transmission of the TIM packet **64**. As described above, the station **12.1** retrieves the time stamp from the TIM packet **64** and loads it into its own modulo n counter **58** which then commences its count sequence at value m. As shown in FIG. **7**, the two modulo n counters **22**, **58** remain in syncnronization as they cyclically count up to value n. This synchronization readily allows the station **12.1** to remain in a doze state until its modulo n counter **58** indicates that the 150th TIM packet **73** is to be generated in, and transmitted from, the access point **14**, and the station **12.1** wakes up at **85**. Only a minor amount of compensation is necessary to allow for the possible modem delay of the transmitter **20** and receiver **48**.

If a time stamp value of the access point counter **22** is not taken and instead the station counter **58** is reset to 0 by the actual receipt of the TIM packet **64**, the late arrival of the TIM packet **64** due to the CSMA/CA delay leads to unsynchronized operation of the counters **22**, **58** because when the access point counter **22** has reached a value m, the station counter **58** is being reset to 0 by receipt of the TIM PACKET **64**. The station counter **58** has therefore just recorded a TIM interval of n+m counts and if the station is then controlled to remain in a doze state until 150 TIM packets have been transmitted, i.e. until after 150 TIM intervals, the station erroneously dozes for 150×(m+n) intervals instead of 150×n intervals and further power consuming compensatory steps are necessary which disadvantageously reduces the power saved by energizing the station receiver only every 150 TIM packets.

Thus, by including a time stamp representing the state of the access point counter **22** at the exact time of transmission of the TIM packet, the power saving benefit of energizing the station only every 150 TIM packets can be increased.

The above describes a preferred embodiment of the integration of the synchronization function in the medium-access-control function. Other forms, in which the reference point in time, where the "time stamp" is sampled, is available to both the transmitter and the receiver, can utilize the start of the frame or the actual location of the time stamp field.

The invention is not restricted to the details of the foregoing power-management embodiment. For example, the apparatus of the present invention can be employed to provide synchronization of frequency channel selection in frequency-hopping devices. In such devices the base station, for example the access point, switches communication operating frequency at a precise moment, and it is required that the other stations in the network are synchronized so as to switch their operating frequency to the new frequency at that moment. In accordance with a further advantage provided by the invention, the access point does not need to transmit a separate frequency-hop signal each time the communication operating frequency is required to change but can include a timing signal for two or more successive frequency-hops which can therefore be delivered to the stations at intervals that are longer than the intervals between the required frequency-hops. Accordingly, the stations can operate in an extended-sleep-mode wherein each xth TIM packet that is received also includes timing information indicating when the station should switch its communication operating frequency. Thus, providing frequency change logic (**86** in FIG. **5**) remains operational during the extended sleep period, the required frequency hop, or hops, can occur during the sleep period so that when the station next wakes up, it is still operating with the same communication frequency as the access point. Advantageously, the synchronized timing control of a frequency hopping device can be combined with the power management function of such a device so that the frequency-change logic **86** and a station wake-up control **88** are controlled by the same timing source **58**.

We claim:

1. A method of synchronizing a receiver with a transmitter in a wireless local area network, comprising:

periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing a receiver timer with the transmitter timer, wherein the timestamp represents a value within a count sequence of a timer in the transmitter and wherein the timestamp accounts for delays due to a busy signal on a medium access protocol, and

synchronizing the receiver with the transmitter based on the timestamp.

2. The method of claim **1**, further comprising:

periodically waking the receiver from a sleep mode to receive transmissions based on output from the receiver timer.

3. The method of claim **1**, further comprising:

controlling a frequency hopping operation based on output from the receiver timer.

4. The method of claim **1**, wherein the step of synchronizing the receiver with the transmitter begins when the transmission signal is completely received.

5. The method of claim **4**, wherein the wherein the step of synchronizing the receiver with the transmitter begins after a CRC data in the received transmission signal is checked.

6. The method of claim **1**, wherein the transmission signal further includes a header field, which is transmitted before the timestamp field and the traffic pending field.

7. The method of claim **6**, wherein the header field includes type data indicating a type of the transmission signal.

8. The method of claim **1**, further comprising:

transmitting the transmission signal from the transmitter, the transmission signal including the timestamp in the timestamp field.

9. A method of synchronizing a receiver with a transmitter in a wireless local area network, comprising:

periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing a receiver timer with the transmitter timer, wherein the timestamp represents a value within a count sequence of a timer in the transmitter at the time of transmission of the transmission signal,

retrieving the timestamp from the transmission signal;

adjusting the value of the timestamp; and

commencing a synchronizing count sequence beginning at the value of the adjusted timestamp.

10. The method of claim **9**, wherein the adjusting step includes the step of adding a compensation factor to the value at which the count sequence begins.

11. The method of claim **10**, wherein the compensation factor compensates for propagation delay at the receiver.

12. The method of claim **10**, wherein the compensation factor allows for time taken to process the transmission signal at the receiver.

13. A method of synchronizing a receiver with a transmitter in a wireless local area network, comprising:

periodically receiving a transmission signal from a transmitter, the transmission signal including a traffic pending field and a timestamp field, the traffic pending field including data indicating stations for which the transmitter has data buffered, the timestamp field including a timestamp having a value m for synchronizing a receiver timer with the transmitter timer, wherein the timestamp represents a value within a count sequence of a timer in the transmitter at the time of transmission of the transmission signal, and

synchronizing the receiver with the transmitter based on the timestamp.

14. The method of claim **13**, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal.

15. The method of claim **13**, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

16. A method of synchronizing a receiver with a transmitter in a wireless local area network, comprising:

periodically receiving a transmission signal from a transmitter, the transmission signal including a a timer interval field and a timestamp field, the timer interval field including timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending fields, the timestamp field including a timestamp having a value m for synchronizing a receiver timer with the transmitter timer, wherein the timestamp represents a value within a count sequence of a timer in the transmitter at the time of transmission of the transmission signal, and

synchronizing the receiver with the transmitter based on the timestamp.

17. The method of claim **16**, wherein the transmission signal further includes a broadcast pending field indicating the presence of outstanding broadcast data packets.

18. The method of claim **16**, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal.

19. The method of claim **16**, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

20. A receiver, comprising:

a receiver counter that counts up to n counts, and

a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer, and wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

21. The receiver of claim **20**, further comprising:

a wake-up controller periodically waking the receiver from a sleep mode to receive transmissions based on output from the receiver counter.

22. The receiver of claim **20**, further comprising:

a frequency change controller controlling a frequency hopping operation based on output from the receiver counter.

23. The receiver of claim **20**, wherein the transmission signal further includes a header field, which is transmitted before the timestamp field and the traffic pending field.

24. The receiver of claim **23**, wherein the header field includes type data indicating a type of the transmission signal.

25. A system including the receiver of claim **20** and a transmitter, the transmitter comprising:

the transmitter timer,

a transmitting modem, and

a controller controlling operation of the transmitting modem to transmit the transmission signal including the timestamp in the timestamp field.

26. A receiver, comprising:

a receiver counter that counts up to n counts,

a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer, and

circuitry for adjusting a value, based on the timestamp, at which a count sequence begins at the receiver timer, wherein the receiver counter commences a synchronizing count sequence beginning at the adjusted value.

27. The receiver of claim **26**, further comprising:

circuitry for commencing the synchronizing count sequence after the transmission signal is completely received.

28. The receiver of claim **27**, further comprising circuitry for commencing the synchronizing count sequence after a CRC data in the received transmission signal is checked.

29. The receiver of claim **26**, further comprising an adder for adding a compensation factor to the value at which the count sequence begins.

30. The receiver of claim **29**, wherein the compensation factor compensates for propagation delay at the receiver.

31. The receiver of claim **29**, wherein the compensation factor allows for time taken to process the transmission signal at the receiver.

32. The receiver of claim **26**, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal.

33. The receiver of claim **26**, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

34. A receiver, comprising:

a receiver counter that counts up to n counts, and

a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a traffic pending field and a timestamp field the traffic pending field including data indicating stations for which the transmitter has data buffered, the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a trans-

mitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer at the time of transmission of the transmission signal.

35. The receiver of claim **34**, wherein the transmission signal further includes a timer interval field, and-the timer interval field includes timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending field.

36. The receiver of claim **35**, wherein the transmission signal further includes a broadcast pending field including broadcast pending data indicating whether data is buffered at an access point including the transmitter.

37. The receiver of claim **35**, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal.

38. The receiver of claim **35**, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

39. The receiver of claim **34**, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal.

40. The receiver of claim **34**, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

41. A system including the receiver of claim **34**, and a transmitter, the transmitter comprising:

the transmitter timer,

a transmitting modem, and

a controller controlling operation of the transmitting modem to transmit the transmission signal including the timestamp in the timestamp field.

42. A method of synchronizing a receiver with a transmitter in a wireless local area network, comprising:

periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing a receiver timer with the transmitter timer, the timestamp representing a value within a count sequence of a timer in the transmitter, wherein the timestamp is loaded into the timestamp field at a given time that, with regard to delays in a modem of the transmitter, is an estimate of the time at which the transmission signal will be transmitted, and

synchronizing the receiver with the transmitter based on the timestamp.

43. The method of claim **42**, further comprising:

transmitting the transmission signal from the transmitter, the transmission signal including the timestamp in the timestamp field.

44. A method of synchronizing a receiver with a transmitter in a wireless local area network, comprising:

periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing a receiver timer with the transmitter timer, the timestamp representing a value within a count sequence of a timer in the transmitter at the time of transmission of the transmission signal, the timestamp accounting for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal, and

synchronizing the receiver with the transmitter based on the timestamp.

45. The method of claim **44**, further comprising:

transmitting the transmission signal from the transmitter, the transmission signal including the timestamp in the timestamp field.

46. A receiver, comprising:

a receiver counter that counts up to n counts, and

a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer, wherein the timestamp is loaded into the timestamp field at a given time that, with regard to delays in a modem of the transmitter, is an estimate of the time at which the transmission signal will be transmitted.

47. A receiver comprising:

a receiver counter that counts up to n counts, and

a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer, and wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal.

48. A system including the receiver of claim **47** and a transmitter, the transmitter comprising:

the transmitter timer,

a transmitting modem, and

a controller controlling operation of the transmitting modem to transmit the transmission signal including the timestamp in the timestamp field.

49. A wireless local area network receiver, comprising:

a receiver timer that counts up to n counts, and

a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp for synchronizing the receiver timer with a transmitter timer that counts up to n counts, the timestamp being a value m which accounts for a delay between a start of a process to transmit the transmission signal from the transmitter and an actual time of transmitting the transmission signal,

wherein the receiver retrieves the timestamp and the receiver timer commences a count sequence based on the value m as to synchronize the receiver timer with the transmitter timer.

50. The receiver of claim **49**, wherein the timestamp accounts for delays in a modem of the transmitter.

51. The receiver of claim **49**, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

52. The receiver of claim **49**, wherein the receiver timer commences a synchronizing count sequence beginning at a value based on the timestamp.

53. The receiver of claim **52**, further comprising circuitry for adjusting the value at which the count sequence begins.

54. The receiver of claim **53**, further comprising an adder for adding a compensation factor to the value at which the count sequence begins.

55. The receiver of claim **54**, wherein the compensation factor compensates for propagation delay at the receiver.

56. The receiver of claim 54, wherein the compensation factor allows for time taken to process the transmission signal at the receiver.

57. The receiver of claim 49, further comprising:

a wake-up controller periodically waking the receiver from a sleep mode to receive transmissions based on output from the receiver timer.

58. The receiver of claim 49, further comprising circuitry for commencing the synchronizing count sequence after the transmission signal is completely received.

59. The receiver of claim 58, further comprising circuitry for commencing the synchronizing count sequence after a CRC data in the received transmission signal is checked.

60. The receiver of claim 49, wherein the transmission signal further includes a traffic pending field that indicates stations for which the transmitter has data buffered.

61. The receiver of claim 60, wherein the transmission signal further includes a timer interval field, and the timer interval field includes timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending fields.

62. A method of synchronizing a timer of a receiver in a first station with a timer of a transmitter in a second station, each timer counting up to n counts, comprising the steps of:

receiving at the receiver a transmission signal containing a timestamp, and

synchronizing the receiver timer with the transmitter timer based on the timestamp, the timestamp being a value m that accounts for a delay between a start of a process to transmit the transmission signal from the transmitter and an actual time of transmitting the transmission signal, the step of synchronizing further including the receiver retrieving the timestamp and the receiver timer commencing a count sequence based on the value m so as to synchronize the receiver timer with the transmitter timer.

63. The method of claim 62, wherein the timestamp accounts for delays in a modem in the transmitter.

64. The method of claim 62, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

65. The method of claim 62, wherein the synchronizing step comprises:

commencing a synchronizing count sequence beginning at a value based upon the timestamp.

66. The method of claim 65, further including the step of adjusting the value at which the count sequence begins.

67. The method of claim 66, further including the step of adding a compensation factor to the value at which the count sequence begins.

68. The method of claim 67, wherein the compensation factor compensates for propagation delay at the receiver.

69. The method of claim 67, wherein the compensation factor allows for time taken to process the transmission signal at the receiver.

70. The method of claim 62, wherein the step of synchronizing the receiver with the transmitter begins when the transmission signal is completely received.

71. The method of claim 70, wherein the wherein the step of synchronizing the receiver with the transmitter begins after a CRC data in the received transmission signal is checked.

72. The method of claim 62, wherein the transmission signal further includes a traffic pending field that indicates stations for which the transmitter has data buffered.

73. The method of claim 72, wherein the transmission signal further includes a timer interval field, and the timer interval field includes timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending fields.

74. The method of claim 73, wherein the transmission signal further includes a broadcast pending field including broadcast pending data indicating whether data is buffered at an access point.

* * * * *

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

NOTICE OF ASSIGNMENT TO UNITED STATES MAGISTRATE JUDGE FOR DISCOVERY

This case has been assigned to District Judge Manuel Real and the assigned discovery Magistrate Judge is Carla Woehrle.

The case number on all documents filed with the Court should read as follows:

CV12- 2047 R (CWx)

Pursuant to General Order 05-07 of the United States District Court for the Central District of California, the Magistrate Judge has been designated to hear discovery related motions.

Unless otherwise ordered, the United States District Judge assigned to this case will hear and determine all discovery related motions.

NOTICE TO COUNSEL

A copy of this notice must be served with the summons and complaint on all defendants (if a removal action is filed, a copy of this notice must be served on all plaintiffs).

Subsequent documents must be filed at the following location:

[X] Western Division
312 N. Spring St., Rm. G-8
Los Angeles, CA 90012

[ ] Southern Division
411 West Fourth St., Rm. 1-053
Santa Ana, CA 92701-4516

[ ] Eastern Division
3470 Twelfth St., Rm. 134
Riverside, CA 92501

Failure to file at the proper location will result in your documents being returned to you.

Name & Address: David E. Sipiora
Kilpatrick Townsend & Stockton, LLP
1400 Wewatta Street, Suite 600
Denver, CO 80202
Telephone: (303) 571-4000
Email: dsipiora@kilpatricktownsend.com

COPY

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

LSI CORPORATION AND AGERE SYSTEMS INC. PLAINTIFF(S) v. FUNAI ELECTRIC COMPANY LTD.; FUNAI CORPORATION, INC.; FUNAI SERVICE CORPORATION; AND P&F USA, INC. DEFENDANT(S).	CASE NUMBER CV 12 2047 -R (CWx) **SUMMONS**

TO: DEFENDANT(S):

A lawsuit has been filed against you.

Within 21 days after service of this summons on you (not counting the day you received it), you must serve on the plaintiff an answer to the attached ☑ complaint ☐ _____ amended complaint ☐ counterclaim ☐ cross-claim or a motion under Rule 12 of the Federal Rules of Civil Procedure. The answer or motion must be served on the plaintiff's attorney, David E. Sipiora, whose address is Kilpatrick Townsend & Stockton, LLP 1400 Wewatta Street, #600 Denver, CO 80202. If you fail to do so, judgment by default will be entered against you for the relief demanded in the complaint. You also must file your answer or motion with the court.

Clerk, U.S. District Court

Dated: MAR 12 2012

By: SEAL MARILYN DAVIS
Deputy Clerk

(Seal of the Court)

[Use 60 days if the defendant is the United States or a United States agency, or is an officer or employee of the United States. Allowed 60 days by Rule 12(a)(3)].

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

I (a) PLAINTIFFS (Check box if you are representing yourself ☐)
LSI CORPORATION and AGERE SYSTEMS INC.

DEFENDANTS
FUNAI ELECTRIC COMPANY, LTD.; FUNAI CORPORATION, INC.; FUNAI SERVICE CORPORATION; P&F USA, INC.

(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.)

David E. Sipiora (SBN 124951) Email: dsipiora@kilpatricktownsend.com
KILPATRICK TOWNSEND & STOCKTON LLP
1400 Wewatta Street, Suite 600, Denver, CO 80202 (303) 571-4000

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an X in one box only.)

☐ 1 U.S. Government Plaintiff ☑ 3 Federal Question (U.S. Government Not a Party)
☐ 2 U.S. Government Defendant ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES - For Diversity Cases Only (Place an X in one box for plaintiff and one for defendant.)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business in this State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business in Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. ORIGIN (Place an X in one box only.)

☑ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify): ☐ 6 Multi-District Litigation ☐ 7 Appeal to District Judge from Magistrate Judge

V. REQUESTED IN COMPLAINT: **JURY DEMAND:** ☑ Yes ☐ No (Check 'Yes' only if demanded in complaint.)

CLASS ACTION under F.R.C.P. 23: ☐ Yes ☑ No ☐ **MONEY DEMANDED IN COMPLAINT: $**

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write a brief statement of cause. Do not cite jurisdictional statutes unless diversity.)
35 U.S.C §§ 271, 283, 284, 285

VII. NATURE OF SUIT (Place an X in one box only.)

OTHER STATUTES
☐ 400 State Reapportionment
☐ 410 Antitrust
☐ 430 Banks and Banking
☐ 450 Commerce/ICC Rates/etc.
☐ 460 Deportation
☐ 470 Racketeer Influenced and Corrupt Organizations
☐ 480 Consumer Credit
☐ 490 Cable/Sat TV
☐ 810 Selective Service
☐ 850 Securities/Commodities/ Exchange
☐ 875 Customer Challenge 12 USC 3410
☐ 890 Other Statutory Actions
☐ 891 Agricultural Act
☐ 892 Economic Stabilization Act
☐ 893 Environmental Matters
☐ 894 Energy Allocation Act
☐ 895 Freedom of Info. Act
☐ 900 Appeal of Fee Determination Under Equal Access to Justice
☐ 950 Constitutionality of State Statutes

CONTRACT
☐ 110 Insurance
☐ 120 Marine
☐ 130 Miller Act
☐ 140 Negotiable Instrument
☐ 150 Recovery of Overpayment & Enforcement of Judgment
☐ 151 Medicare Act
☐ 152 Recovery of Defaulted Student Loan (Excl. Veterans)
☐ 153 Recovery of Overpayment of Veteran's Benefits
☐ 160 Stockholders' Suits
☐ 190 Other Contract
☐ 195 Contract Product Liability
☐ 196 Franchise

REAL PROPERTY
☐ 210 Land Condemnation
☐ 220 Foreclosure
☐ 230 Rent Lease & Ejectment
☐ 240 Torts to Land
☐ 245 Tort Product Liability
☐ 290 All Other Real Property

TORTS PERSONAL INJURY
☐ 310 Airplane
☐ 315 Airplane Product Liability
☐ 320 Assault, Libel & Slander
☐ 330 Fed. Employers' Liability
☐ 340 Marine
☐ 345 Marine Product Liability
☐ 350 Motor Vehicle
☐ 355 Motor Vehicle Product Liability
☐ 360 Other Personal Injury
☐ 362 Personal Injury-Med Malpractice
☐ 365 Personal Injury-Product Liability
☐ 368 Asbestos Personal Injury Product Liability

IMMIGRATION
☐ 462 Naturalization Application
☐ 463 Habeas Corpus-Alien Detainee
☐ 465 Other Immigration Actions

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☐ 371 Truth in Lending
☐ 380 Other Personal Property Damage
☐ 385 Property Damage Product Liability

BANKRUPTCY
☐ 422 Appeal 28 USC 158
☐ 423 Withdrawal 28 USC 157

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☐ 441 Voting
☐ 442 Employment
☐ 443 Housing/Accommodations
☐ 444 Welfare
☐ 445 American with Disabilities - Employment
☐ 446 American with Disabilities - Other
☐ 440 Other Civil Rights

PRISONER PETITIONS
☐ 510 Motions to Vacate Sentence Habeas Corpus
☐ 530 General
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☐ 555 Prison Condition

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☐ 610 Agriculture
☐ 620 Other Food & Drug
☐ 625 Drug Related Seizure of Property 21 USC 881
☐ 630 Liquor Laws
☐ 640 R.R. & Truck
☐ 650 Airline Regs
☐ 660 Occupational Safety /Health
☐ 690 Other

LABOR
☐ 710 Fair Labor Standards Act
☐ 720 Labor/Mgmt. Relations
☐ 730 Labor/Mgmt. Reporting & Disclosure Act
☐ 740 Railway Labor Act
☐ 790 Other Labor Litigation
☐ 791 Empl. Ret. Inc. Security Act

PROPERTY RIGHTS
☐ 820 Copyrights
☑ 830 Patent
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SOCIAL SECURITY
☐ 861 HIA (1395ff)
☐ 862 Black Lung (923)
☐ 863 DIWC/DIWW (405(g))
☐ 864 SSID Title XVI
☐ 865 RSI (405(g))

FEDERAL TAX SUITS
☐ 870 Taxes (U.S. Plaintiff or Defendant)
☐ 871 IRS-Third Party 26 USC 7609

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FOR OFFICE USE ONLY: Case Number: _____

AFTER COMPLETING THE FRONT SIDE OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED BELOW.

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has this action been previously filed in this court and dismissed, remanded or closed? ☑ No ☐ Yes
If yes, list case number(s): _____

VIII(b). RELATED CASES: Have any cases been previously filed in this court that are related to the present case? ☑ No ☐ Yes
If yes, list case number(s): _____

Civil cases are deemed related if a previously filed case and the present case:
(Check all boxes that apply) ☐ A. Arise from the same or closely related transactions, happenings, or events; or
☐ B. Call for determination of the same or substantially related or similar questions of law and fact; or
☐ C. For other reasons would entail substantial duplication of labor if heard by different judges; or
☐ D. Involve the same patent, trademark or copyright, and one of the factors identified above in a, b or c also is present.

IX. VENUE: (When completing the following information, use an additional sheet if necessary.)

(a) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named plaintiff resides.
☐ Check here if the government, its agencies or employees is a named plaintiff. If this box is checked, go to item (b).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
	LSI Corporation (Santa Clara County) Agere Systems Inc. (Pennsylvania)

(b) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named defendant resides.
☐ Check here if the government, its agencies or employees is a named defendant. If this box is checked, go to item (c).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
	Funai Electric Company, Ltd. (Japan); Funai Corporation, Inc. (New Jersey); Funai Service Corporation (Ohio); P&F USA, Inc. (Georgia)

(c) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** claim arose.
Note: In land condemnation cases, use the location of the tract of land involved.

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Los Angeles County	

*** Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, or San Luis Obispo Counties**
Note: In land condemnation cases, use the location of the tract of land involved

X. SIGNATURE OF ATTORNEY (OR PRO PER): _____ Date March 12, 2012

Notice to Counsel/Parties: The CV-71 (JS-44) Civil Cover Sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law. This form, approved by the Judicial Conference of the United States in September 1974, is required pursuant to Local Rule 3-1 is not filed but is used by the Clerk of the Court for the purpose of statistics, venue and initiating the civil docket sheet. (For more detailed instructions, see separate instructions sheet.)

Key to Statistical codes relating to Social Security Cases:

Nature of Suit Code	Abbreviation	Substantive Statement of Cause of Action
861	HIA	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405(g))
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405(g))
864	SSID	All claims for supplemental security income payments based upon disability filed under Title 16 of the Social Security Act, as amended.
865	RSI	All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended. (42 U.S.C. (g))