ORIGINAL

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

REALTEK SEMICONDUCTOR CORPORATION, a Taiwanese corporation,

Plaintiff,

vs.

LSI CORPORATION, a Delaware corporation,

Defendant.

Case No. CV 12 3437

ORIGINAL COMPLAINT

DEMAND FOR JURY TRIAL

ORIGINAL COMPLAINT

Plaintiff Realtek Semiconductor Corporation ("Realtek") brings this action for patent infringement of United States Patent Nos. 6,787,928 and 6,963,226 (collectively, "Patents-In-Suit") and alleges as follows:

PARTIES

1. Plaintiff Realtek is a corporation organized under the laws of Taiwan with its principal place of business at No.2 Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan.

2. Upon information and belief, Defendant LSI Corporation ("Defendant" or "LSI") is a corporation organized and existing under the laws of Delaware, with its principal place of business at 1621 Barber Lane, Milpitas, California 95035.

JURISDICTION

3. This Court has subject matter jurisdiction over this dispute under 28 U.S.C. §§ 1331 and 1338(a).

4. This Court has personal jurisdiction over Defendant, which has conducted and continues to conduct business in the State of California and in this Judicial District. Defendant has committed acts of patent infringement alleged herein within the State of California and, more particularly, within this Judicial District. Moreover, Defendant purposefully and voluntarily placed infringing products into the stream of commerce with the expectation that they will be purchased by consumers in this Judicial District. These infringing products have been and continue to be purchased by consumers in this Judicial District.

VENUE

5. Venue is proper in the Northern District of California under 28 U.S.C. §§ 1391(b) and 1400(b) because, upon information and belief, acts and transactions constituting at least a subset of the violations alleged herein occurred in this Judicial District and because one or more of the defendants reside and transact business in this Judicial District. Venue is also proper in this Judicial District under 28 U.S.C. § 1391(c) because Defendant is subject to personal jurisdiction in this District.

INTRADISTRICT ASSIGNMENT

6. Because this case is an Intellectual Property Action, it is not subject to assignment to a particular location or division of the Court under Local Rule 3-2(c).

COUNT ONE: PATENT INFRINGEMENT

(U. S. Patent No. 6,787,928)

7. Realtek incorporates by reference the allegations in each of the foregoing paragraphs as if fully set forth herein.

8. On September 7, 2004, United States Patent No. 6,787,928 ("the '928 patent"), entitled "Integrated Circuit Device Having Pads Structure Formed Thereon and Method For Forming The Same," duly and legally issued. A true and correct copy of the '928 patent is attached hereto as "Exhibit A" and made a part hereof.

9. Realtek is the owner of all rights and title to the '928 patent and has the right to enforce the '928 patent with respect to Defendant LSI.

10. On information and belief, LSI has and continues to make, use, offer to sell, and/or import semiconductor chips that infringe one or more claims of the '928 patent, specifically including but not limited to LSI's B64002, SF-2281VB1-SDC and FW643E 1394B OHCI chips.

11. On information and belief, LSI has been and still is infringing one or more of the claims of the '928 patent by actively inducing others to infringe and contributing to the infringement by others of the '928 patent. As a result, LSI has been and still is infringing one or more of the claims of the '928 patent as defined by 35 U.S.C. § 271 (a), (b), and/or (c).

12. Realtek has suffered damage by reason of LSI's infringement and will continue to suffer additional damage until this Court enjoins the infringing conduct.

13. Realtek is informed and believes and thereon alleges that LSI's infringement of the '928 patent has been willful, including to the extent that LSI has continued or does continue its infringing activities after receiving notice of the '928 patent, thereby entitling Realtek to the recovery of increased damages under 35 U.S.C. § 284.

14. By the aforesaid actions, LSI has violated the patent laws of the United States, 35 U.S.C. Section 271, *et al.*, and will continue to do so unless permanently enjoined by the Court.

15. This is an "exceptional case" justifying an award of attorneys' fees and costs to Realtek under 35 U.S.C. § 285.

16. Realtek believes that LSI will continue to infringe the '928 patent unless enjoined

by this Court. Such infringing activity causes Realtek irreparable harm for which there is no adequate remedy at law, and will continue to cause such harm without the issuance of an injunction.

COUNT TWO: PATENT INFRINGEMENT

(U. S. Patent No. 6,963,226)

17. Realtek incorporates by reference the allegations in each of the foregoing paragraphs as if fully set forth herein.

18. On November 8, 2005, United States Patent No. 6,963,226 ("the '226 patent"), entitled "Low-To-High Level Shifter," duly and legally issued. A true and correct copy of the '226 patent is attached hereto as "Exhibit B" and made a part hereof.

19. Realtek is the owner of all right and title to the '226 patent and has the right to enforce the '226 patent with respect to Defendant LSI.

20. On information and belief, LSI has and continues to make, use, offer to sell, sell and/or import semiconductor chips that infringe one or more claims of the '226 patent, specifically including but not limited to LSI's ET1011C2-C and LSISAS1078 chips.

21. On information and belief, LSI has been and still is infringing one or more of the claims of the '226 patent by actively inducing others to infringe and contributing to the infringement by others of the '226 patent. As a result, LSI has been and still is infringing one or more of the claims of the '226 patent as defined by 35 U.S.C. § 271 (a), (b), and/or (c).

22. Realtek has suffered damage by reason of LSI's infringement and will continue to suffer additional damage until this Court enjoins the infringing conduct.

23. Realtek is informed and believes and thereon alleges that LSI's infringement of the '928 patent has been willful, including to the extent that LSI has continued or does continue its infringing activities after receiving notice of the '226 patent, thereby entitling Realtek to the recovery of increased damages under 35 U.S.C. § 284.

24. By the aforesaid actions, LSI has violated the patent laws of the United States, 35 U.S.C. Section 271, *et al.*, and will continue to do so unless permanently enjoined by the Court.

25. This is an "exceptional case" justifying an award of attorneys' fees and costs to

25. This is an "exceptional case" justifying an award of attorneys' fees and costs to Realtek under 35 U.S.C. § 285.

26. Realtek believes that LSI will continue to infringe the '226 patent unless enjoined by this Court. Such infringing activity causes Realtek irreparable harm for which there is no adequate remedy at law and will continue to cause such harm without the issuance of an injunction.

PRAYER FOR RELIEF

WHEREFORE, Realtek prays for relief as follows:

A. Judgment that one or more of the claims of each of the Patents-In-Suit have been infringed, either literally and/or under the doctrine of equivalents, by LSI;

B. Judgment in favor of Realtek awarding damages adequate to compensate Realtek for LSI's acts of infringement, contributory infringement, and active inducement of infringement of the Patents-in-Suit, including but not limited to monetary damages of no less than a reasonable royalty;

C. Judgment for increased damages for willful infringement under 35 U.S.C. § 284;

D. Judgment that this is an "exceptional case" and awarding Realtek its reasonable attorneys' fees and costs under 35 U.S.C. § 285;

E. A permanent injunction restraining LSI, its officers, directors, employees, agents, attorneys, subsidiaries, affiliates, successors and assigns, and all others in active concert or participation with LSI or under LSI's authority, from making, using, offering for sale, selling and/or importing infringing products, and from otherwise infringing, contributing to the infringement of, or actively inducing infringement of, each of the Patents-In-Suit;

F. An award of pre-judgment and post-judgment interest at the maximum rate allowed by law on the above damages awards;

G. Judgment awarding Realtek its expenses, costs, and attorneys fees in accordance with Rule 54(d) of the Federal Rules of Civil Procedure; and

H. For such other and further relief as the Court deems just and proper.

Date: June 29, 2012

By: _____
Adrian Sue Shin
Attorneys for Plaintiff
REALTEK SEMICONDUCTOR CORPORATION

DEMAND FOR JURY TRIAL

Realtek hereby demands a jury trial on all issues so triable.

Date: June 29, 2012

By:_____
Adrian Sue Shin
Attorneys for Plaintiff
REALTEK SEMICONDUCTOR CORPORATION

Exhibit A

US006787928B1

(12) **United States Patent**
Lin

(10) **Patent No.: US 6,787,928 B1**
(45) **Date of Patent: Sep. 7, 2004**

(54) **INTEGRATED CIRCUIT DEVICE HAVING PADS STRUCTURE FORMED THEREON AND METHOD FOR FORMING THE SAME**

(75) Inventor: **Ying-Hsi Lin**, Hsinchu (TW)

(73) Assignee: **Realtek Semiconductor Corp.**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/425,973**

(22) Filed: **Apr. 30, 2003**

(30) **Foreign Application Priority Data**

Feb. 26, 2003 (TW) ..... 92104606 A

(51) **Int. Cl.**[7] **H01L 29/40**

(52) **U.S. Cl.** **257/786**; 257/701; 257/758; 257/774; 257/773

(58) **Field of Search** 257/208, 211, 257/701, 758, 759, 762, 760, 774, 773, 786

(56) **References Cited**

U.S. PATENT DOCUMENTS

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5,736,791	A *	4/1998	Fujiki et al.	257/781
5,923,088	A *	7/1999	Shiue et al.	257/758
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6,163,074	A *	12/2000	Lee et al.	257/734
6,313,537	B1 *	11/2001	Lee et al.	257/758
6,465,337	B1 *	10/2002	Lee et al.	438/612
2001/0000928	A1 *	5/2001	Lee et al.	257/786

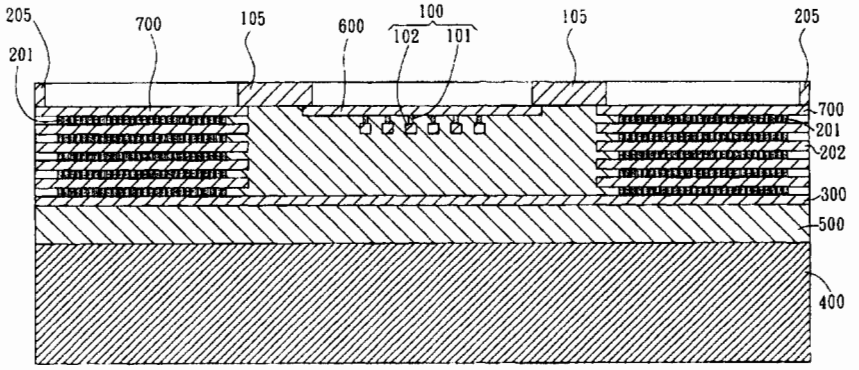
* cited by examiner

Primary Examiner—Nathan J. Flynn
Assistant Examiner—Pershelle Greene
(74) *Attorney, Agent, or Firm*—Troxell Law Office PLLC

(57) **ABSTRACT**

The invention is to provide a structure of IC pad and its forming method. The structure is arranged in an insulation layer and is comprised of a lower electric-conduction layer, a compound layer structure and a pad layer. The lower electric-conduction layer is arranged at an appropriate position in the insulation layer and is connected to an electric potential. The compound layer structure is arranged on the insulation layer and is composed of at least one electric-conduction layer and at least one electric-conduction connecting layer, both are inter-overlapped to each other. The pad layer is arranged on the compound layer structure.

22 Claims, 5 Drawing Sheets



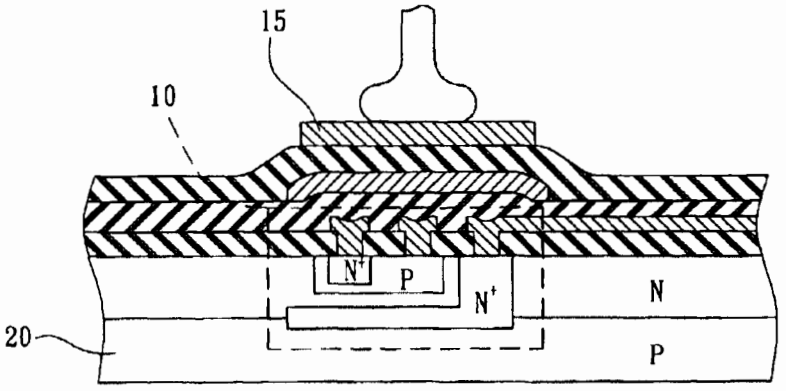


FIG. 1
(PRIOR ART)

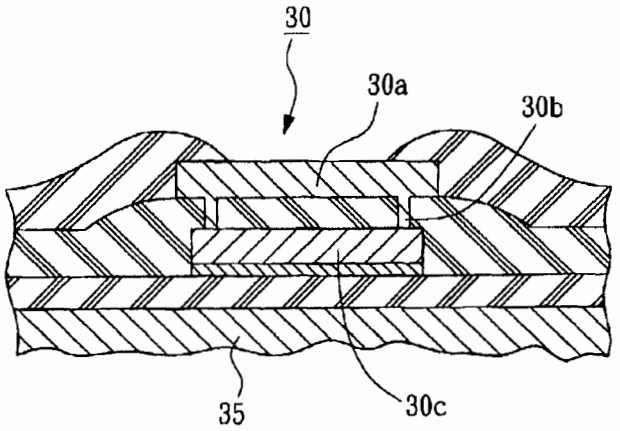


FIG. 2
(PRIOR ART)

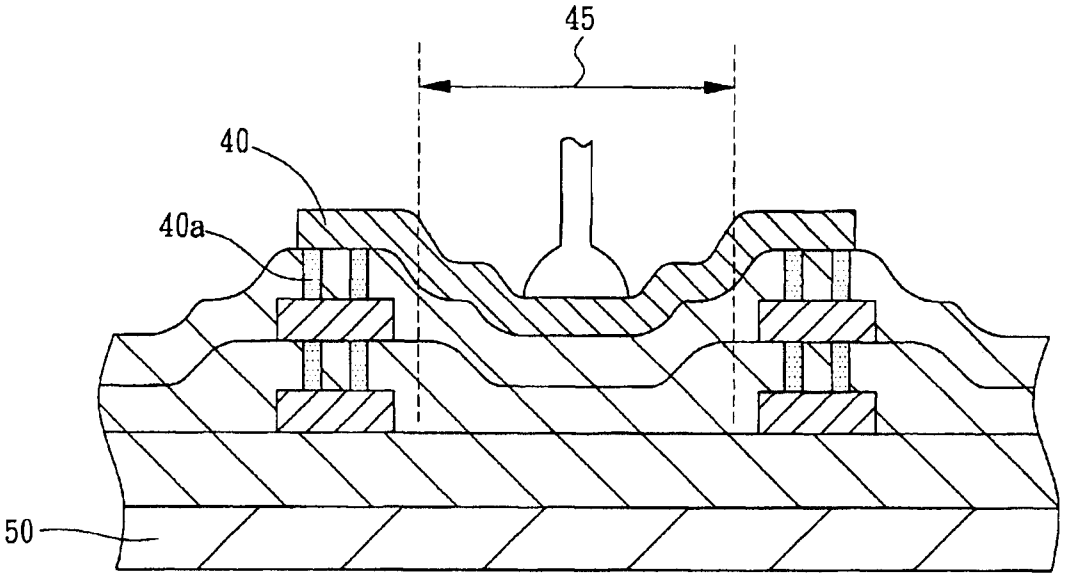


FIG. 3
(PRIOR ART)

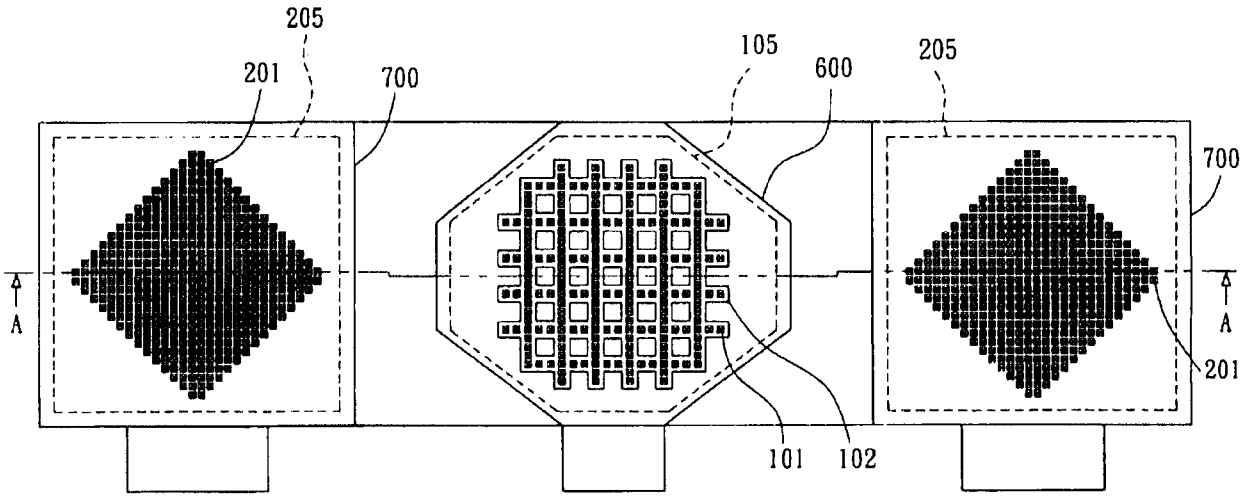


FIG. 4

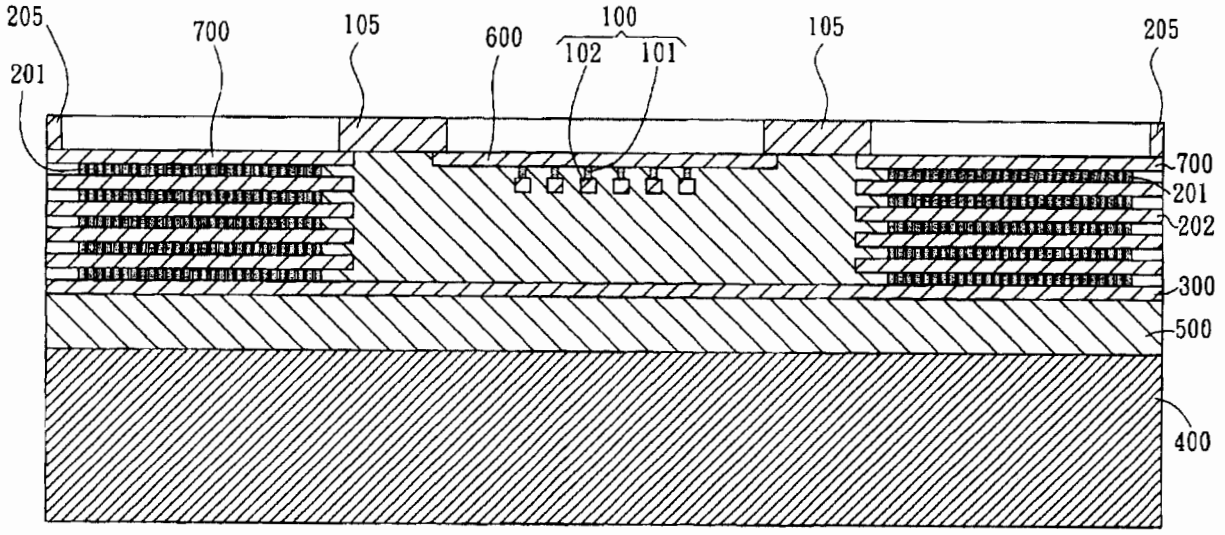


FIG. 5

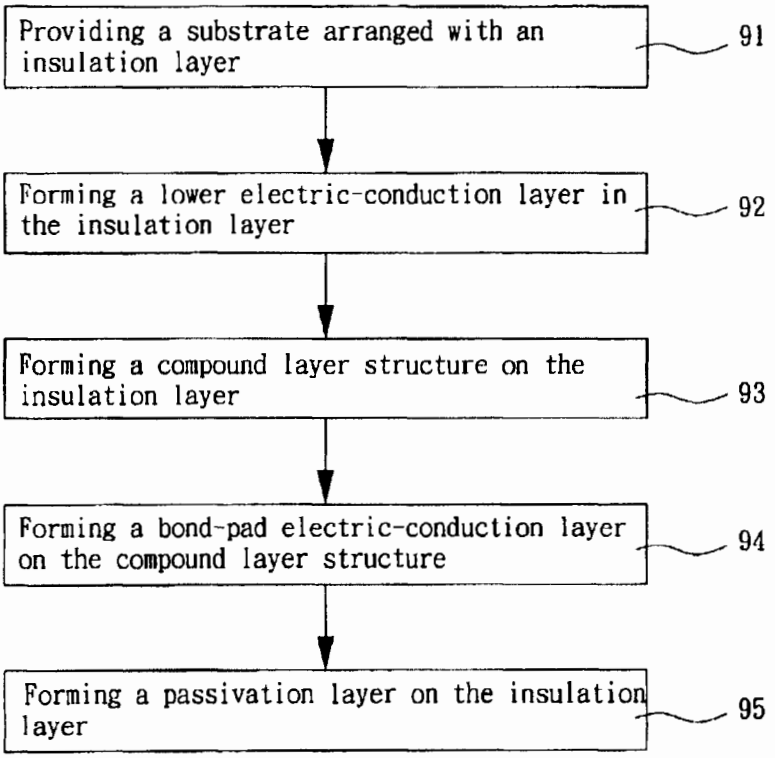

Providing a substrate arranged with an insulation layer
91
Forming a lower electric-conduction layer in the insulation layer
92
Forming a compound layer structure on the insulation layer
93
Forming a bond-pad electric-conduction layer on the compound layer structure
94
Forming a passivation layer on the insulation layer
95

FIG. 6

INTEGRATED CIRCUIT DEVICE HAVING PADS STRUCTURE FORMED THEREON AND METHOD FOR FORMING THE SAME

FIELD OF THE INVENTION

The invention relates to a structure of IC pad and its forming method, in particular to a structure and method that are adapted to form a pad of integrated circuit of high frequency and low noise; not only the noise from the semiconductor substrate be separated effectively and the value of equivalent electric capacitance of the pad be lowered, but also the bonding adherence be further enhanced.

BACKGROUND OF THE INVENTION

Recently, since the requirement of transceiver of low power and low cost is steadily on the increase, so the technology of mainstream IC competitively concentrates on how to realize further more functions of radio frequency on one single chip. Except making integrated circuit be able to arrange on the package substrate, the external circuit connected by the external legs of package substrate must be electrically connected to the integrated circuit. So, when packaging the integrated circuit, the technology of pad has become an important factor that influences the yield and quality of a product. This pad adapted for providing electric connection between the integrated circuit and the external circuit is usually arranged in the metal zone around the IC die. When the pad is formed, the metal connecting wire must contact with the pad accurately and connect to the external legs of the IC packaging substrate. Because of the limitation of the prior arts and the characteristics of metal connecting wire and pad, the area of pad is sometimes too large to occupy too much area of chip. Furthermore, during high frequency, the performance of the integrated circuit is influenced because the equivalent electric capacitance is too large.

Additionally, because of the market growth of communication IC recently, the operational frequency of integrated circuit is also growing in indexing type. The low noise and low loss of high frequency signal are always the pursuing goals for communication IC.

In 1987, the U.S. Pat. No. 4,636,832 "Semiconductor device with an improved bonding section" proposed a design method of the pad of integrated circuit. Please refer to FIG. **1**, which is a cross-sectional diagram of the IC device disclosed in the U.S. Pat. No. 4,636,832. The characteristic of this prior art is that the semiconductor element **10** is arranged below the pad **15**. Although it may reduce the area of layout, this kind of pad can not be adapted to high frequency circuit with low noise because the noise coming from the semiconductor substrate **20** will directly influence the signal of high frequency when it passes through the pad.

To overcome the tensile and tension of bonding, the U.S. Pat. No. 5,248,903 "Composite pads for semiconductor devices" proposed a kind of pad. Please refer to FIG. **2**, which is the cross-sectional diagram of the IC device disclosed in the U.S. Pat. No. 5,248,903. Wherein, the pad **30** has at least two layers of electric-conduction layer **30*a*** and **30*c*** and a connection layer **30*b***. But, this kind of pad is not adapted for the signals of high frequency and low noise because the noise of semiconductor substrate **35** will directly influence the quality of signal.

The U.S. Pat. No. 5,502,337 "Semiconductor device structure including multiple intereonnection layers with

interlayer insulating films" proposed a different designing method for pad. Please refer to FIG. **3**, which is a cross-sectional diagram for the IC device disclosed in the U.S. Pat. No. 5,502,337, which arranges the connection layer **40*a*** in the pad **40** around the bonding zone **45**. When the integrated circuit is manufactured, a bonding zone of arc shape will be formed on the pad **40** to thereby enhance the bonding adherence. However, the technology of current integrated circuit has stepped into the levels of sub micrometer or deep sub micrometer, and CMP (Chemical-Mechanical Polish) is already a standard procedure for current semiconductor process. So, this kind of prior art no longer generates original effectiveness in current semiconductor process, besides this technique has the same drawback as that of previous techniques; i.e., it can not separate the noise coming from the semiconductor substrate **50**.

From above discussion, we know that the prior arts described there are unable to propose an effective solution that aims for the high frequency, low noise and bonding adherence. Therefore, the emphasis of the invention is to provide a pad structure adapted for a integrated circuit of high frequency and low noise to lower down the equivalent electric capacitance and enhance the bonding adherence, such that it can prevent the entire pad from being drawn out of the semiconductor chip by the tension generated in the bonding procedure.

SUMMARY OF THE INVENTION

The main objective of the present invention is to provide a structure of IC pad and its forming method, which are adapted for the structure of the pad of an integrated circuit of high frequency and low noise, such that the effective area of the pad may be reduced effectively to thereby reduce its value of equivalent electric capacitance.

The second objective of the present invention is to provide a structure of IC pad and its forming method effectively separate the noise coming from the semiconductor substrate.

The further objective of the present invention is to provide a structure of IC pad and its forming method effectively enhance the bonding adherence, such that it prevent the entire pad from being drawn out of the semiconductor chip by the tension generated in the bonding procedure.

To achieve above objectives, the invention provides an IC pad structure arranged in an insulation layer comprises a lower electric-conduction layer, a compound layer structure and a pad layer.

The lower electric-conduction layer is arranged in the insulation layer and is connected to an electric potential.

The compound layer structure arranged on the insulation layer comprises at least one electric-conduction layer and at least one electric-conduction connecting layer, each of the electric-conduction layer are connected to each other.

The pad layer is arranged on the compound layer structure.

To achieve above objectives, the invention further presents method for forming IC pad structure, comprising the following steps of:

Step (a): providing a substrate arranged with an insulation layer.

Step (b): forming a lower electric-conduction layer which prepared connect to an electric potential.

Step (c): forming a compound layer structure composed by inter-overlapping or connect at least one electric-conduction layer and at least one electric-conduction connecting layer on the insulation layer.

Step (d): forming a pad layer on the compound layer structure, of which area is larger than that of the electric-conduction layer of the compound layer structure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional diagram for the IC device disclosed in the U.S. Pat. No. 4,636,832.

FIG. **2** is a cross-sectional diagram for the IC device disclosed in the U.S. Pat. No. 5,248,903.

FIG. **3** is a cross-sectional diagram for the IC device disclosed in the U.S. Pat. No. 5,502,337.

FIG. **4** is an upper side view for the structural illustration of a preferable embodiment of the IC pad according to the invention.

FIG. **5** is a cross-sectional view along the A-A line cutting through FIG. **4** illustrating the preferable embodiment of the IC pad according to the invention.

FIG. **6** is a flowchart illustrating the preferable embodiment of the method forming the IC pad according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

For your esteemed member of reviewing committee to further recognize and understand the characteristics, objectives, and functions of the present invention, a detailed description together with corresponding drawings are presented thereinafter.

The invention discloses a structure of IC pad and its forming method. Its embodiments are described according to referential drawings, in which similar referential numbers represent similar elements.

Please refer to FIG. **4** and FIG. **5**, which are structural illustrations for the preferable embodiments of the IC pad according to the present invention. The IC pad structure includes a lower electric-conduction layer **300**, a compound layer structure **100**, and a first pad layer **600**. The lower electric-conduction layer **300** formed at an appropriate position in the insulation layer **500** is coupled with plural electric-conduction layers **202** and plural electric-conduction connecting layers **201**, shown in FIG. **5**, such that the lower electric-conduction layer **300** may a voltage signal from a second pad layer **700** formed on the upper surface exposing on the insulation layer **500** through provide electric-conduction layers **202** and electric-conduction connecting layers **201** shown in FIG. **5**, which further provides a connection to a device providing the voltage signal (not shown in the drawings). The second pad layer **700** further forms a bonding zone with a chip passivation layer **205** and **105**. The noise transferred from the substrate **40** will be kept away by the lower electric-conduction layer **300** which may be connected to a power source or voltage signal by the second pad layer **700**.

The compound layer structure **100** is arranged on the insulation layer **500** and is composed of at least one electric-conduction layer **102** and at least one electric-conduction connecting layer **101**, both which are inter-overlapped to each other. The pad layer **600** is arranged on the compound layer structure **100** and is adjacent to the top face side of the insulation layer **500**. In the preferable embodiments according to the invention and in order to lower down the value of the effective capacitance of the entire pad, the pad layer **600** is realized by the structuring method of polygon shape and the area of the electric-conduction layer **102** is designed to be smaller than that of the pad layer **600**, such that the value of the equivalent electric capacitance to the lower electric-conduction layer **300** may be further effectively lowered down. The electric-conduction layer **102** may be realized by the methods of railing structure or honeycomb structure that may reduce the area of electric-conduction layer **102**. The electric-conduction connecting layer **101** further includes plural vias and plural via plugs. The structure of this electric-conduction connecting layer **101** may be modified and implemented by those who are skilled in such art according to above disclosure, but it still possesses the merits of the invention and is also within the spirit and scope of the invention, so repetitious description is not presented herein.

In the preferable embodiments according to the invention, the IC pad structure further includes a passivation layer **105**, which is arranged on the insulation layer **500** and is partially connected to the pad layer **600**. From above design, the compound layer structure **100** is signally connected and structured to the pad layer **600**, and a steady bonding zone is thereby formed, such that it may enhance the boding tension and effectively raise the bonding adherence. Therefore, the tension generated during the bonding procedure to draw the entire structure of the IC pad out of the semiconductor chip may be prevented.

In order to further recognize and understand the characteristics, objectives and functions of the present invention, please refer to FIG. **6**, which is a flowchart illustrating the preferable embodiment of the method forming the IC pad according to the invention, wherein the numbers **91**, **92**, **93**, **94** and **95** shown in the drawing respectively illustrate the steps from (a) to (e) of the method forming the IC pad according to the invention.

Step (a): providing a substrate that is arranged with an insulation layer thereon.

Step (b): forming a lower electric-conduction layer at an appropriate position in the insulation layer; the lower electric-conduction layer is composed of plural electric-conduction layers and plural electric-conduction connecting layers. In this embodiment, each of the electric-conduction layer is interlaced-connected to the corresponding electric-conduction connecting layers, as shown in FIG. **5**, such that a signal connection may be provided to a bond-pad electric-connection layer, which further forms a bonding zone with a passivation layer, such that the pad layer may be connected to a potential of cleaner power source or electric potential.

Step (c): a compound layer structure formed on the insulation layer is composed of at least one electric-conduction layer and at least one electric-conduction connecting layer, each of the electric-conduction layer is interlaced-connected to the corresponding electric-conduction connecting layers, as shown in FIG. **5**, and the area of the electric-conduction layer can be reduced by the methods of railing structure or honeycomb structure, and the electric-conduction connecting layer further includes the structure of plural vias and plural via plugs.

Step (d): forming a pad layer on the compound layer structure, wherein the area of the former is larger than that of the electric-conduction layer of the latter, and the pad layer is structured as a polygon shape.

Step (e): forming a passivation layer on the insulation layer, such that the pad layer may form a bonding zone with the passivation layer.

Accordingly, the structure of an IC pad and its forming method according to the invention may indeed reduce the value of equivalent electric capacitance of the entire pad, separate the noise coming from the semiconductor substrate,

and increase the bonding adherence, so this kind of designing method may be adapted to integrated circuit of high frequency and fulfill the requirement of high frequency and low noise.

What is claimed is:

1. An integrated circuit (IC) device having a pad structure formed thereon, the IC device comprising:

a) a substrate;

b) an insulation layer formed on the substrate;

c) a lower electric-conduction layer formed in the insulation layer;

d) a compound layer structure formed in the insulation layer;

e) a first pad layer formed on the insulation layer and coupled to the compound layer structure, wherein the first pad layer and the compound layer structure are spaced apart from the lower electric-conduction layer; and

f) a second pad layer formed on the insulation layer and coupled to the lower electric-conduction layer.

2. The IC device according to claim **1**, wherein the compound layer structure comprises a first electric-conduction layer and a first connecting layer to couple the first electric-conduction layer to the first pad layer.

3. The IC device according to claim **2**, wherein the first connecting layer comprises a plurality of via plugs.

4. The IC device according to claim **2**, wherein the first electric-conduction layer is shaped like a webbed railing.

5. The IC device according to claim **2**, wherein the area of the first electric-conduction layer is smaller than that of the first pad layer.

6. The IC device according to claim **1**, wherein the first pad layer is shaped like a polygon.

7. The IC device according to claim **1**, further comprising a passivation layer formed on the insulation layer to cover a part of the outer rim of at least one of the first and second pad layers.

8. The IC device according to claim **1**, further comprising at least one second connecting layer for coupling the second pad layer to the lower electric-conduction layer.

9. The IC device according to claim **8**, further comprising at least one second electric-conduction layer coupled between the second pad layer and the lower electric-conduction layer with the second connecting layer.

10. The IC device according to claim **1**, wherein a noise from the substrate is kept away from the first pad layer by the lower electric-conduction layer.

11. An integrated circuit (IC) device having a pad structure formed thereon, the IC device comprising:

a) a substrate;

b) an insulation layer formed on the substrate;

c) a lower electric-conduction layer formed in the insulation layer;

d) a compound layer structure formed in the insulation layer; and

e) a first pad layer formed on the insulation layer and coupled to the compound layer structure, wherein the first pad layer and the compound layer structure are spaced apart from the lower electric-conduction layer.

12. The IC device according to claim **11**, wherein the compound layer structure comprises a first electric-conduction layer and a first connecting layer to couple the first electric-conduction layer to the first pad layer.

13. The IC device according to claim **11**, further comprising a second pad layer formed on the insulation layer and coupled to the lower electric-conduction layer.

14. The IC device according to claim **13**, further comprising at least one second connecting layer for coupling the second pad layer to the lower electric-conduction layer; and at least one second electric-conduction layer coupled between the second pad layer and the lower electric-conduction layer with the second connecting layer.

15. The IC device according to claim **14**, wherein, the area of the first electric-conduction layer is smaller than that of the first pad layer.

16. The IC device according to claim **11**, wherein the first pad layer is shaped like a polygon.

17. The IC device according to claim **11**, further comprising a passivation layer formed on the insulation layer to cover a part of the outer rim of at least one of the first and second pad layers.

18. The IC device according to claim **11**, wherein a noise from the substrate is kept away from the first pad layer by the lower electric-conduction layer.

19. A method for fabricating an IC device having a pad structure formed thereon, the method comprising:

a) providing a substrate;

b) forming an insulation layer formed on the substrate;

c) forming a lower electric-conduction layer formed in the insulation layer, at least a part of the lower electric-conduction layer being covered by the insulation layer;

d) forming a compound layer structure formed in the insulation layer, the compound layer structure being spaced apart from and not connected to the lower electric-conduction layer; and

e) forming a first pad layer formed on the insulation layer, the first pad layer being coupled to the compound layer,

wherein in the forming a first pad layer step e) the first pad layer and the compound layer are spaced apart from the lower electric-conduction layer.

20. The method according to claim **19**, wherein a noise from the substrate is kept away form the first pad layer by the lower electric-conduction layer.

21. The method according to claim **19**, wherein the forming a compound layer structure step d) further comprises the steps of:

forming at least one first electric-conduction layer on the insulation layer; and

forming at least one first connecting layer on the insulation layer, wherein the first connecting layer is to couple the first electric-conduction layer to the first pad layer.

22. The method according to claim **21**, wherein the area of the first electric-conduction layer is smaller than that of the first pad layer.

* * * * *

Exhibit B

US006963226B2

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Chiang

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(54) **LOW-TO-HIGH LEVEL SHIFTER**

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(51) **Int. Cl.**[7] **H03K 19/0175**
(52) **U.S. Cl.** **326/68**; 326/81
(58) **Field of Search** 326/63–74, 80–83

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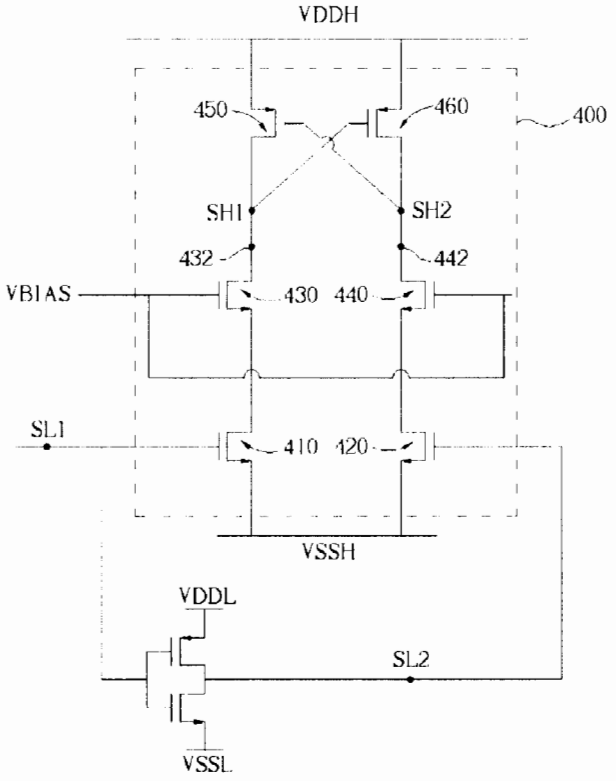
(57) **ABSTRACT**

A low-to-high level shifter operating under a first supply voltage is disclosed. The low-to-high level shifter includes a pull-down circuit coupled to an input signal, the pull-down circuit having a plurality of low-voltage devices, the input signal corresponding to a second supply voltage; and a pull-up circuit coupled to the pull-down circuit, the pull-up circuit having a plurality of high-voltage devices. The low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply voltage is larger than the second supply voltage.

22 Claims, 2 Drawing Sheets



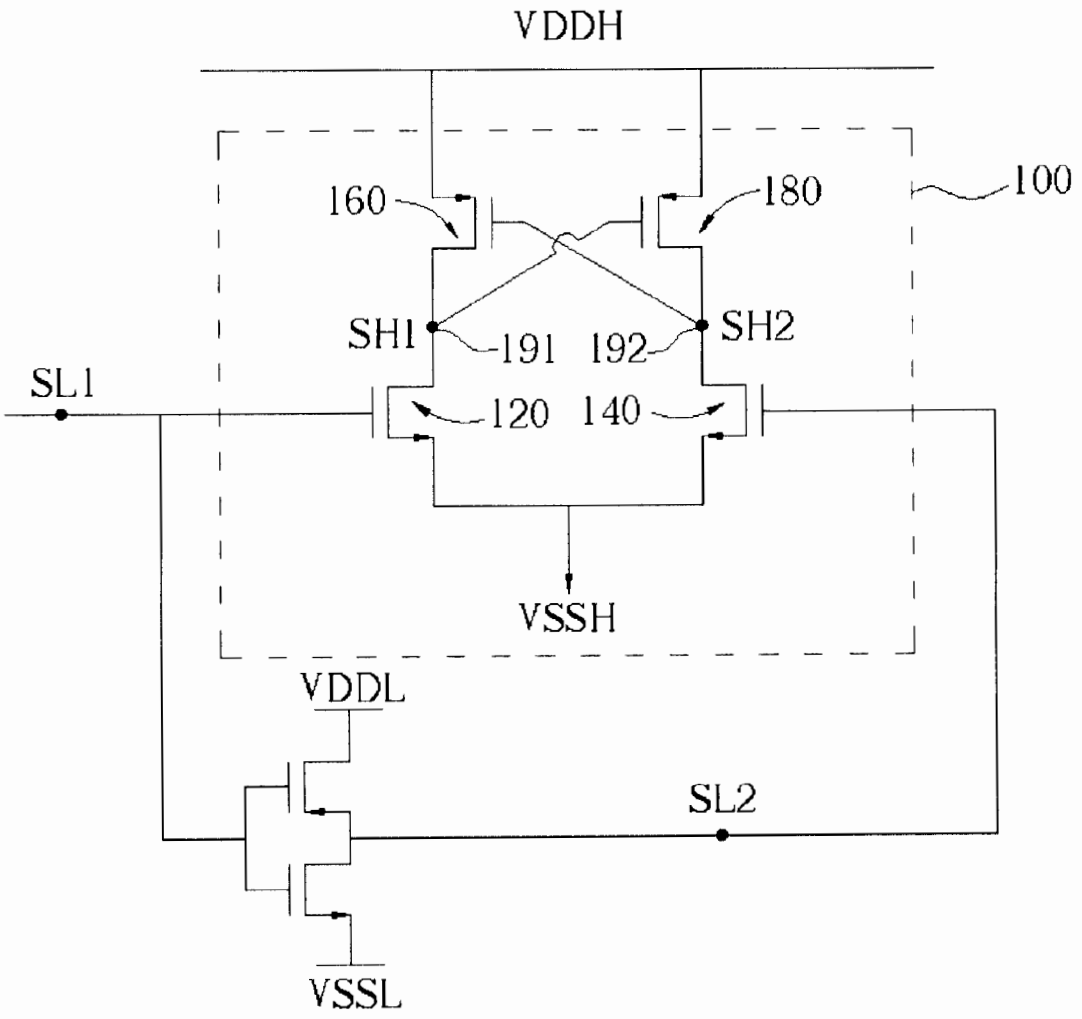


Fig. 1 Prior Art

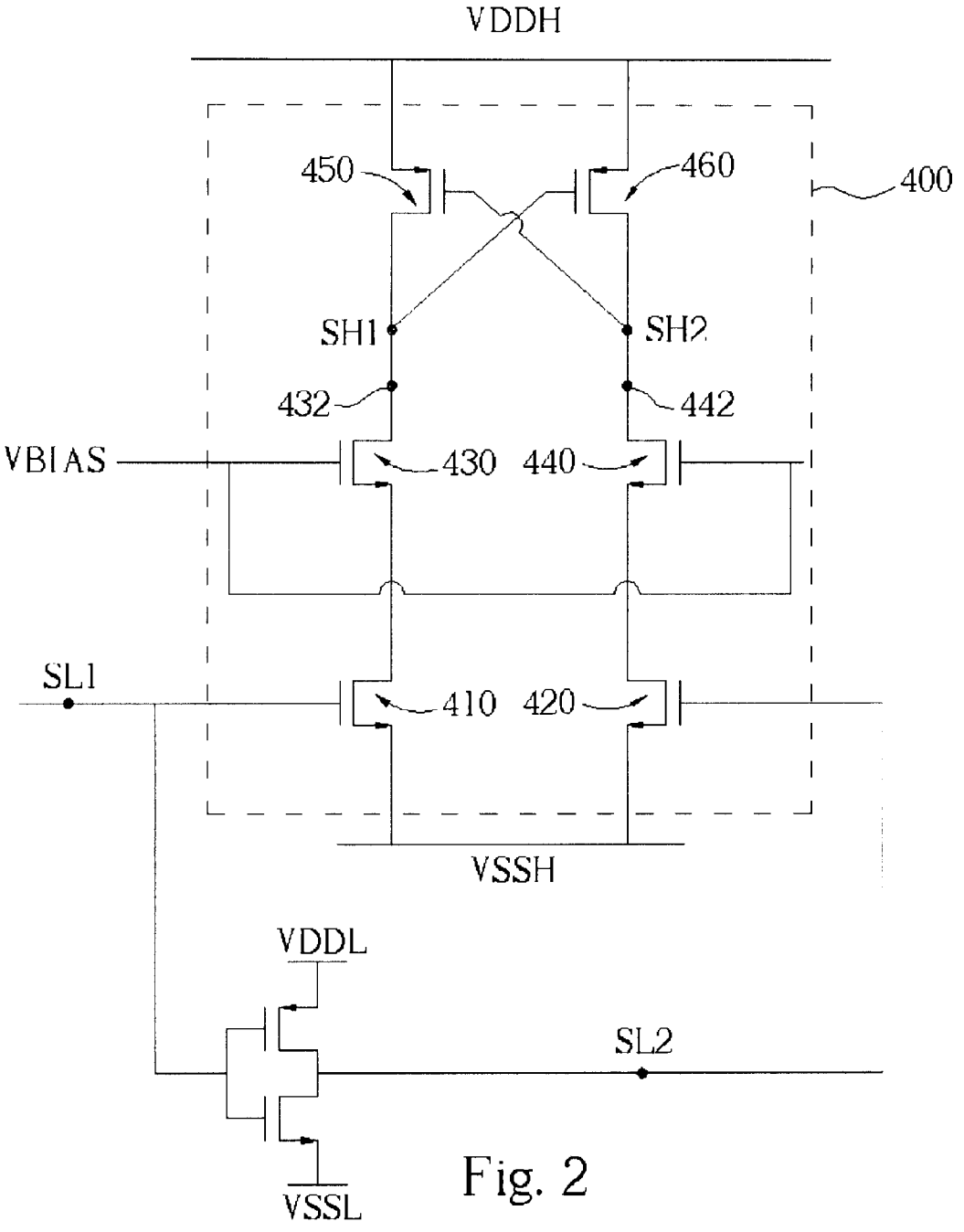

VDDH
450
460
400
SH1
SH2
432
442
VBIAS
430
440
SL1
410
420
VSSH
VDDL
SL2
VSSL

Fig. 2

LOW-TO-HIGH LEVEL SHIFTER

BACKGROUND OF INVENTION

1. Field of the Invention

The invention relates to a level shifter, and more particularly, to a level shifter for shifting the voltage level of a logic signal from a low operating voltage to a high operating voltage.

2. Description of the Prior Art

In an integrated circuit, because of the concerns of power and integration, the operating voltage of the integrated circuit is usually smaller than the operating voltage of an external system. Take an integrated circuit using 1.2V as the operating voltages to be an example, 1.2V and 0V are used to represent logic value 1 and 0 respectively. But an external circuit usually uses higher voltage as the operating voltage than the integrated circuit. For example, the operating voltage of circuit elements on a motherboard is normally 5V or 3.3V, that is, 5V or 3.3V is used to represent logic value 1, while 0V is used to represent logic value 0. Accordingly, in an integrated circuit, a device must be set for shifting the level of a logic signal switching between 1.2V and 0V into a logic signal switching between 5V(or 3.3V) and 0V, which is termed "low-to-high level shifter" hereinafter.

In an integrated circuit, a component operating at 5V/3.3V is called high-voltage element; a component operating at 1.2V is called low-voltage element. Take metal-oxide-semiconductor transistors (MOS transistor) for example, being a high-voltage element or a low-voltage element is determined by the thickness of the oxide-layer of the MOS transistor. Generally speaking, a high-voltage MOS transistor has a thicker oxide-layer than a low-voltage MOS transistor. Consequently, the threshold voltage of the high-voltage MOS transistor is higher than the threshold voltage of the low-voltage MOS transistor. Normally a high-voltage MOS transistor has a nominal threshold voltage of 0.9V.

Please refer to FIG. **1**, a circuit diagram of a conventional low-to-high level shifter is illustrated. The low-to-high level shifter **100** includes: a high-voltage NMOS transistor **120**, a high-voltage NMOS transistor **140**, a high-voltage PMOS transistor **160** and a high-voltage PMOS transistor **180**. When the four transistors are turned on or off, a first output end **191** and a second output end **192** will be charged or discharged, and the goal of level shifting will be achieved as a result.

Assume that in FIG. **1**, VDDH=3.3V, VSSH=0V, VDDL=1.2V, VSSL=0V. When the potential of a first input signal SL1 changes from VSSL to VDDL, at first the high-voltage NMOS transistor **120** will be turned on, while the high-voltage NMOS transistor **140** will be turned off, the potential of a first output signal SH1 on the first output end **191** will become VSSH. Next, because the potential of the first output signal SH1 equals VSSH, the high-voltage PMOS transistor **180** will be turned on, in turn the potential of the second output signal SH2 on the second output end **192** will become VDDH.

But with advanced technology on integrated circuit processes, the operating voltage of the integrated circuit becomes smaller and smaller. For example, an integrated circuit produced through advanced technology can have an operating voltage lower than 1.2, such as 0.9V or even lower. Under such circumstances the low-to-high level shifter **100** in FIG. **1** will probably pass logic signals wrongly.

Now consider the situation when VDDL equals 1V (assume that other parameters are unchanged). When the potential of the first input signal SL1 changes from VSSL to VDDL, because VDDL is only a bit higher than the threshold voltage of the high-voltage NMOS transistor **120**, the falling speed of the potential of the first output signal SH1 will be slow, in turn the raising speed of the potential of the second output signal SH2 will also be slow. The consequence is that the switching time for the integrated circuit becomes longer, the jitter problem of logic signals becomes more serious, and as a result the whole circuit becomes unreliable. If the operating frequency of the first input signal SL1 rises, the potential of the first output signal SH1 may not have enough time to switch correctly. An extreme case is that when VDDL equals 0.9V or is lower than 0.9V, when the potential at the gate of the high-voltage NMOS transistor **120** or the high-voltage NMOS transistor **140** equals VDDL, the two transistors may not be turned on, and the low-to-high level shifter can not function correctly at all.

As depicted above, one problem the prior art low-to-high level shifter faces is that logic signals probably can not pass through the low-to-high level shifter correctly, when the operating voltage of the integrated circuit becomes smaller and smaller

SUMMARY OF INVENTION

It is therefore one of the many objectives of the claimed invention to provide a low-to-high level shifter using low-voltage elements as pull-down elements and including a clamping circuit.

According to embodiments of the invention, a low-to-high level shifter operating under a first supply voltage is disclosed. The low-to-high level shifter comprises a pull-down circuit coupled to an input signal, the input signal corresponding to a second supply voltage; a pull-up circuit coupled to the pull-down circuit; and a clamping circuit coupled to the pull-down circuit, for clamping an operating voltage of the pull-down circuit. The low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply voltage is larger than the second supply voltage.

According to embodiments of the invention, a low-to-high level shifter operating under a first supply voltage is disclosed. The low-to-high level shifter comprises a pull-down circuit coupled to an input signal, the pull-down circuit comprising a plurality of low-voltage devices, the input signal corresponding to a second supply voltage; and a pull-up circuit coupled to the pull-down circuit, the pull-up circuit comprising a plurality of high-voltage devices. The low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply voltage is larger than the second supply voltage.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a circuit diagram of a conventional low-to-high level shifter.

FIG. **2** is a circuit diagram of a low-to-high level shifter according to an embodiment of the present invention.

DETAILED DESCRIPTION

Please refer to FIG. **2**, a circuit diagram of a low-to-high level shifter according to an embodiment of the present invention is illustrated. A low-to-high level shifter **400** includes a pull-down circuit, a pull-up circuit, and a clamping circuit. In this embodiment, the pull-down circuit includes a first pull-down unit, that is a low-voltage NMOS transistor **410**; and a second pull-down unit, that is a low-voltage NMOS transistor **420**. The pull-up circuit includes a first pull-up unit, that is a high-voltage PMOS transistor **450**; and a second pull-up unit, that is a high-voltage PMOS transistor **460**. The clamping circuit includes a first clamping unit, that is a high-voltage NMOS transistor **430**; and a second clamping unit, that is a high-voltage NMOS transistor **440**. Please note that herein MOS transistors are divided into high-voltage MOS transistors and low-voltage MOS transistors, where they have different thickness on their oxide-layer, they can operate at different voltage range, and they have different threshold voltage.

In FIG. **1** the low-to-high level shifter **100** uses high-voltage elements (that is, the high-voltage NMOS transistor **120** and the high-voltage NMOS transistor **140**) as pull-down elements, while in this embodiment, low-voltage elements (that is, the low-voltage NMOS transistor **410** and the low-voltage NMOS transistor **420**) are used. Because low-voltage elements have lower threshold voltage than high-voltage elements (for example, the threshold voltages of high-voltage elements and low-voltage elements are 0.9V and 0.5V respectively), when VDDL is used as the gate voltage of the low-voltage NMOS transistor **410** or the low-voltage NMOS transistor **420**, the channel between the drain and source of the transistor can be turned on correctly, then the potential at its drain can be discharged to VSSH very fast. It should be noted that being low voltage elements, the potential at the drain of the low-voltage NMOS transistor **410** or the low-voltage NMOS transistor **420** should not be of too high a value (such as VDDH), or the element will probably be damaged. So in this embodiment, two clamping units are used to guarantee the potential at the drain of the low-voltage NMOS transistor **410** or the low-voltage NMOS transistor **420** will not be too high to damage these low-voltage elements.

The gate of the high-voltage NMOS transistor **430** couples to a bias voltage VBIAS, for making sure that the potential at the drain of the low-voltage NMOS transistor **410** will not exceed VBIAS subtracting the threshold voltage Vt of the high-voltage transistor **430**. So if the maximum potential the low-voltage NMOS transistor **410** can tolerate at its drain is 1.5V, a simple design choice is to use 2.4V as VBIAS (at this time VBIAS−Vt=1.5V). The function of the high-voltage NMOS transistor **440** is similar to that of the high-voltage NMOS transistor **430**.

The gate of the high-voltage PMOS transistor **450** couples to a second output end **442**, the drain couples to a first output end **432**, and the source couples to a high-voltage bias having potential equals VDDH. The function of the high-voltage PMOS transistor **450** is to pull up the potential of the first output signal SH1 at the first output end **432** to become VDDH when the potential of the second output signal SH2 at the second output end **442** substantially equals VSSH. The function of the high-voltage PMOS transistor **460** is similar to that of the high-voltage PMOS transistor **450**.

Please note that although in this embodiment the gates of the high-voltage NMOS transistor **430** and the high-voltage NMOS transistor **440** use only one bias voltage VBIAS, in other embodiments these two transistors can use different bias voltages with different potentials. The way to generate the bias voltage is a design choice of the circuit designer.

The low-to-high level shifter according to embodiments of the present invention uses low-voltage elements as pull-down elements, while uses clamping elements to protect the low-voltage elements. As a result, the low-to-high level shifter according to embodiments of the present invention can pass logical signals correctly even with the operating voltage of the integrated circuit becoming smaller and smaller.

Those skilled in the art will readily observe that numerous modification and alternation of the device may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A low-to-high level shifter operating under a first supply voltage, the low-to-high level shifter comprising:

a pull-down circuit coupled to an input signal, the input signal corresponding to a second supply voltage;

a pull-up circuit coupled to the pull-down circuit; and

a clamping circuit coupled to the pull-down circuit, for clamping an operating voltage of the pull-down circuit;

wherein the low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply is larger than the second supply voltage;

wherein the pull-down circuit comprises a plurality of low-voltage devices, and the pull-up circuit comprises a plurality of high-voltage devices.

2. The low-to-high level shifter of claim **1** wherein the low-voltage devices have a lower turn-on characteristic than the high-voltage devices.

3. The low-to-high level shifter of claim **1** wherein the pull-down circuit comprises a first pull-down transistor and a second pull-down transistor, control terminals of the first and the second pull-down transistors are coupled to the input signal.

4. The low-to-high level shifter of claim **1** wherein the pull-up circuit comprises a first pull-up transistor and a second pull-up transistor, a control terminal of the first pull-up transistor is coupled to a first terminal of the second pull-up transistor, and a control terminal of the second pull-up transistor is coupled to a first terminal of the first pull-up transistor.

5. The low-to-high level shifter of claim **4** wherein the output signal is extracted from the first terminal of the first pull-up transistor.

6. The low-to-high level shifter of claim **4** wherein the first terminals of the first and the second pull-up transistors are coupled to the pull-down circuit.

7. The low-to-high level shifter of claim **1** wherein the clamping circuit comprises a first clamping transistor and a second clamping transistor, control terminals of the first and the second clamping transistors are coupled to a bias voltage.

8. The low-to-high level shifter of claim **1** wherein the input signal is coupled to the pull-down circuit via an inverter operating under the second supply voltage.

9. A low-to-high level shifter operating under a first supply voltage, the low-to-high level shifter comprising:

a pull-down circuit coupled to an input signal, the pull-down circuit comprising a plurality of low-voltage devices, the input signal corresponding to a second supply voltage; and

a pull-up circuit coupled to the pull-down circuit, the pull-up circuit comprising a plurality of high-voltage devices;

wherein the low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply voltage is larger than the second supply voltage.

10. The low-to-high level shifter of claim **9** further comprising:

a clamping circuit coupled to the pull-down circuit, for clamping an operating voltage of the pull-down circuit.

11. The low-to-high level shifter of claim **10** wherein the clamping circuit comprises a first clamping transistor and a second clamping transistor, control terminals of the first and the second clamping transistors are coupled to a bias voltage.

12. The low-to-high level shifter of claim **9** wherein the pull-down circuit comprises a first pull-down transistor and a second pull-down transistor, control terminals of the first and the second pull-down transistors are coupled to the input signal.

13. The low-to-high level shifter of claim **9** wherein the pull-up circuit comprises a first pull-up transistor and a second pull-up transistor, a control terminal of the first pull-up transistor is coupled to a first terminal of the second pull-up transistor, and a control terminal of the second pull-up transistor is coupled to a first terminal of the first pull-up transistor.

14. The low-to-high level shifter of claim **13** wherein the output signal is extracted from the first terminal of the first pull-up transistor.

15. The low-to-high level shifter of claim **13** wherein the first terminals of the first and the second pull-up transistors are coupled to the pull-down circuit.

16. The low-to-high level shifter of claim **9** wherein the input signal is coupled to the pull-down circuit via an inverter operating under the second supply voltage.

17. The low-to-high level shifter of claim **9** wherein the low-voltage devices have a lower turn-on characteristic than the high-voltage devices.

18. A low-to-high level shifter operating under a first supply voltage, the low-to-high level shifter comprising:

a pull-down circuit coupled to an input signal, the pull-down circuit comprising a plurality of first-voltage devices, the input signal corresponding to a second supply voltage; and

a pull-up circuit coupled to the pull-down circuit, the pull-up circuit comprising a plurality of second-voltage devices;

wherein the low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply voltage is larger than the second supply voltage;

wherein the first-voltage devices and the second-voltage devices have different threshold voltages.

19. The low-to-high level shifter of claim **18** further comprising:

a clamping circuit coupled to the pull-down circuit, for clamping an operating voltage of the pull-down circuit.

20. The low-to-high level shifter of claim **19** wherein the clamping circuit comprises a first clamping transistor and a second clamping transistor, control terminals of the first and the second clamping transistors are coupled to a bias voltage.

21. The low-to-high level shifter of claim **18** wherein the first-voltage devices comprise a first pull-down transistor and a second pull-down transistor, control terminals of the first and the second pull-down transistors are coupled to the input signal.

22. The low-to-high level shifter of claim **18** wherein the second-voltage devices comprise a first pull-up transistor and a second pull-up transistor, a control terminal of the first pull-up transistor is coupled to a first terminal of the second pull-up transistor, and a control terminal of the second pull-up transistor is coupled to a first terminal of the first pull-up transistor.

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