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Attorneys for Plaintiff
SONY CORPORATION

UNITED STATES DISTRICT COURT

FOR THE CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION, SANTA ANA

SACV13-00546 JVS (ANx)

SONY CORPORATION, a Japanese corporation,

Plaintiff,

v.

RED.COM, INC., dba Red Digital Cinema, a Washington corporation,

Defendant.

CIVIL ACTION NO. _____

COMPLAINT FOR PATENT INFRINGEMENT

JURY TRIAL DEMANDED

Plaintiff Sony Corporation ("Sony") files this Complaint against Red.com, Inc. dba Red Digital Cinema ("Red") pursuant to the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*, and alleges as follows:

THE PARTIES

1. Sony is a corporation organized and existing under the laws of Japan with offices at 1-7-1 Konan, Minato-ku, Tokyo, 108-0075, Japan.

2. On information and belief, Red is a corporation organized and existing under the laws of Washington, having its principal place of business at 34 Parker, Irvine, California 92618, and doing business within this judicial district. Upon information and belief, Red makes, imports into the United States, offers for sale, sells, and/or uses in the United States digital cinematography products, including, without limitation, the RED ONE, EPIC, and SCARLET cameras; various Digital Still & Motion Camera ("DSMC") modules such as the SSD MODULE, the DSMC SIDE HANDLE, and the REDMOTE; and various displays such as the RED TOUCH 5.0'' LCD and the RED TOUCH 9.0'' LCD.

JURISDICTION AND VENUE

3. This lawsuit is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338.

4. Red is subject to personal jurisdiction in this Court because, on information and belief, it does and has done substantial business in this judicial District, including: (i) designating an agent for service of process in the State of California; (ii) committing acts of patent infringement in this District and elsewhere in California and the United States; and (iii) regularly doing business or soliciting business, engaging in other persistent courses of conduct, and/or deriving substantial revenue from products and/or services provided to individuals in this District and in this State. On information and belief, Red's place of business in Irvine includes manufacturing, repair, data recovery, technical support, direct sales,

and product demonstration facilities. Further, on information and belief, Red has an additional place of business at 846 North Cahuenga Boulevard, Los Angeles, California 90038. On information and belief, Red's place of business in Los Angeles includes a retail store as well as repair, data recovery, technical support, product demonstration, and studio services facilities.

5. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400(b) because Red regularly conducts business in this judicial district, has a regular and established place of business in this judicial district, and/or because certain of the acts complained of herein occurred in this judicial district.

THE PATENTS-IN-SUIT

6. On August 15, 1995, the United States Patent and Trademark Office ("USPTO") issued U.S. Patent No. 5,442,718 ("the '718 patent"), entitled "Apparatus and Method for Storing and Reproducing Digital Image Data Yielding High Resolution and High Quality Video Image Data," naming Hideki Kobayashi and Yasuo Ido as inventors. A true and correct copy of the '718 patent is attached hereto as Exhibit A.

7. On June 4, 1996, the USPTO issued U.S. Patent No. 5,523,795 ("the '795 patent"), entitled "Method and Apparatus for Serial Transmission and/or Reception of Nonsynchronous, Multiplexed signals," naming Mamoru Ueda as inventor. A true and correct copy of the '795 patent is attached hereto as Exhibit B.

8. On December 7, 1999, the USPTO issued U.S. Patent No. 5,999,213 ("the '213 patent"), entitled "Method of and Apparatus for Setting up Electronic Device," naming Katsuhiko Tsushima, Kazuyoshi Miyamoto, Taku Kihara, and Yoshio Chiba as inventors. A true and correct copy of the '213 patent is attached hereto as Exhibit C.

9. On December 28, 1999, the USPTO issued U.S. Patent No. 6,009,233 ("the '233 patent), entitled "Apparatus and Method for Recording and Reproducing a Video Signal With Camera Setting Data," naming Takashi Tsujimura, Terumasa

Funabashi, and Chihiro Kaihatsu (now known as Chihiro Motono) as inventors. A true and correct copy of the '233 patent is attached hereto as Exhibit D.

10. On July 23, 2002, the USPTO issued U.S. Patent No. 6,423,993 ("the '993 patent"), entitled "Solid-state Image-sensing Device and Method for Producing the Same," naming Ryoji Suzuki, Takahisa Ueno, Hirofumi Sumi, and Keiji Mabuchi as inventors. A true and correct copy of the '993 patent is attached hereto as Exhibit E.

11. On November 21, 2006, the USPTO issued U.S. Patent No. 7,138,617 ("the '617 patent"), entitled "Solid-state Image Pickup Device and Output Method Thereof," naming Keiji Mabuchi as inventor. A true and correct copy of the '617 patent is attached hereto as Exhibit F.

12. On December 4, 2007, the USPTO issued U.S. Patent No. 7,304,287 ("the '287 patent"), entitled "Solid-state Image Pickup Device and Output Method Thereof," naming Keiji Mabuchi as inventor. On May 20, 2008, the USPTO issued a Certificate of Correction for the '287 patent. A true and correct copy of the '287 patent with the certificate of correction is attached hereto as Exhibit G.

13. The '718 patent, the '795 patent, the '213 patent, the '233 patent, the '993 patent, the '617 patent, and the '287 patent are collectively and henceforth referred to as the "patents-in-suit."

14. Sony owns by assignment the entire right, title and interest in and to each of the patents-in-suit with full and exclusive right to sue for past, present, and future infringements thereof.

CAUSES OF ACTION

COUNT I: INFRINGEMENT OF THE '718 PATENT

15. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

16. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of

equivalents, the '718 patent by practicing one or more claims of the '718 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the RED ONE, EPIC, and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '718 patent.

17. Red's activities have been without Sony's authorization.

18. As a result of Red's infringement of the '718 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

COUNT II: INFRINGEMENT OF THE '795 PATENT

19. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

20. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of equivalents, the '795 patent by practicing one or more claims of the '795 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the RED ONE, EPIC, and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '795 patent.

21. Red's activities have been without Sony's authorization.

22. As a result of Red's infringement of the '795 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

COUNT III: INFRINGEMENT OF THE '213 PATENT

23. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

24. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of

equivalents, the '213 patent by practicing one or more claims of the '213 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the REDMOTE, as well as the EPIC and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '213 patent.

25. Red's activities have been without Sony's authorization.

26. As a result of Red's infringement of the '213 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

COUNT IV: INFRINGEMENT OF THE '233 PATENT

27. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

28. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of equivalents, the '233 patent by practicing one or more claims of the '233 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the SSD MODULE, DSMC SIDE HANDLE, and RED TOUCH LCD as well as the RED ONE, EPIC, and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '233 patent.

29. Red's activities have been without Sony's authorization.

30. As a result of Red's infringement of the '233 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

COUNT V: INFRINGEMENT OF THE '993 PATENT

31. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

32. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of equivalents, the '993 patent by practicing one or more claims of the '993 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the EPIC and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '993 patent.

33. Red's activities have been without Sony's authorization.

34. As a result of Red's infringement of the '993 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

COUNT VI: INFRINGEMENT OF THE '617 PATENT

35. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

36. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of equivalents, the '617 patent by practicing one or more claims of the '617 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the EPIC and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '617 patent.

37. Red's activities have been without Sony's authorization.

38. As a result of Red's infringement of the '617 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

COUNT VII: INFRINGEMENT OF THE '287 PATENT

39. Sony repeats and re-alleges the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

40. Upon information and belief, in violation of 35 U.S.C. § 271, Red has infringed and is continuing to infringe, literally and/or under the doctrine of equivalents, the '287 patent by practicing one or more claims of the '287 patent in the manufacture, use, offering for sale, sale, and/or importation of multiple Red products, including the EPIC and SCARLET cameras. Sony reserves the right to contend that additional Red products infringe the '287 patent.

41. Red's activities have been without Sony's authorization.

42. As a result of Red's infringement of the '287 patent, Sony has been damaged, and will be further damaged, and is entitled to be compensated for such damages pursuant to 35 U.S.C. § 284 in an amount that presently cannot be ascertained, but that will be determined at trial.

PRAYER FOR RELIEF

WHEREFORE, Sony prays for the following relief:

(a) That the Court enter judgment that Red has infringed each and every one of the patents-in-suit under 35 U.S.C. § 271 *et seq*;

(b) That the Court enter judgment that Sony has suffered irreparable harm as a result of Red's infringement, for which there is no adequate remedy at law;

(c) That Red, its officers, agents, servants, employees, and those persons acting in active concert or in participation with them be preliminarily and thereafter permanently enjoined pursuant to 35 U.S.C. § 283 from making, using, importing, offering to sell, or selling any products that infringe one or more of the patents-in-suit, including but not limited to the RED ONE, EPIC, or SCARLET cameras, the SSD MODULE, the DSMC SIDE HANDLE, the REDMOTE, the RED TOUCH 5.0'' LCD, or the RED TOUCH 9.0'' LCD, or otherwise further infringing one or more of the patents-in-suit pursuant to 35 U.S.C. § 283;

(d) That Red be required to provide to Sony an accounting of all gains, profits, and advantages derived by Red as a result of its infringement of the patents-

in-suit, and that Sony be awarded damages adequate to compensate Sony for the wrongful infringing acts by Red, in accordance with 35 U.S.C. § 284;

(e) That Red be ordered to pay prejudgment and postjudgment interest;

(f) That Red be ordered to pay all costs associated with this action;

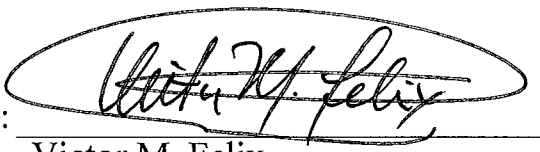
(g) That Red be directed to deliver up and destroy all infringing products, including but not limited to all RED ONE, EPIC, and SCARLET cameras; and

(h) That Sony be granted such other and additional relief as the Court deems just and proper.

DATED: April 5, 2013

Respectfully submitted,

PROCOPIO CORY, HARGREAVES & SAVITCH LLP

By: 

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csteenburg@wolfgreenfield.com; jmiller@wolfgreenfield.com

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiff hereby demands a trial by jury as to all issues so triable.

DATED: April 5, 2013

Respectfully submitted,

PROCOPIO CORY, HARGREAVES & SAVITCH LLP

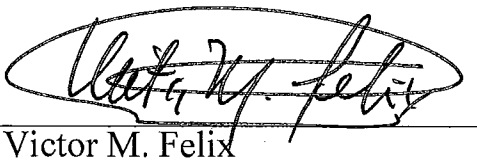
By: 

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EXHIBIT A

US005442718A

United States Patent [19]

Kobayashi et al.

[11] **Patent Number: 5,442,718**

[45] **Date of Patent: Aug. 15, 1995**

[54] **APPARATUS AND METHOD FOR STORING AND REPRODUCING DIGITAL IMAGE DATA YIELDING HIGH RESOLUTION AND HIGH QUALITY VIDEO IMAGE DATA**

[75] Inventors: **Hideki Kobayashi; Yasuo Ido,** both of Kanagawa, Japan

[73] Assignee: **Sony Corporation,** Tokyo, Japan

[21] Appl. No.: **114,168**

[22] Filed: **Sep. 1, 1993**

[30] **Foreign Application Priority Data**

Sep. 7, 1992 [JP] Japan 4-264231

[51] **Int. Cl.**[6] **G06K 9/00**

[52] **U.S. Cl.** **382/166;** 348/393; 358/525; 358/539; 382/233; 382/300

[58] **Field of Search** 382/56, 47; 358/512, 358/525, 539; 395/128, 131; 348/393, 395, 403

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,660,081	4/1987	Heerah	358/160
4,823,201	4/1989	Simon et al.	358/133
5,053,861	10/1991	Tsai et al.	358/525
5,065,229	11/1991	Tsai et al.	358/525
5,172,227	12/1992	Tsai et al.	358/539
5,287,188	2/1994	Saeger et al.	348/565

Primary Examiner—Leo H. Boudreau

Attorney, Agent, or Firm—William S. Frommer; Alvin Sinderbrand

[57] **ABSTRACT**

An apparatus for processing image data. The apparatus converts analog green image data signals, analog red image data signals, and analog blue image data signals generated by imaging an object. The third image generation elements, representing the green image data, are arranged at positions shifted by a half pitch to the first and second image generation elements. The analog image data signals are converted into digital image data signals and are then compressed at a predetermined compression rate and stored in a recording medium by a storage means. In reproducing the image data, the recorded image data is read from the recording medium and expanded at a predetermined expansion rate to generate data substantially the same as the image data signals before compression. The expanded data is interpolated in a predetermined interpolation manner.

53 Claims, 7 Drawing Sheets

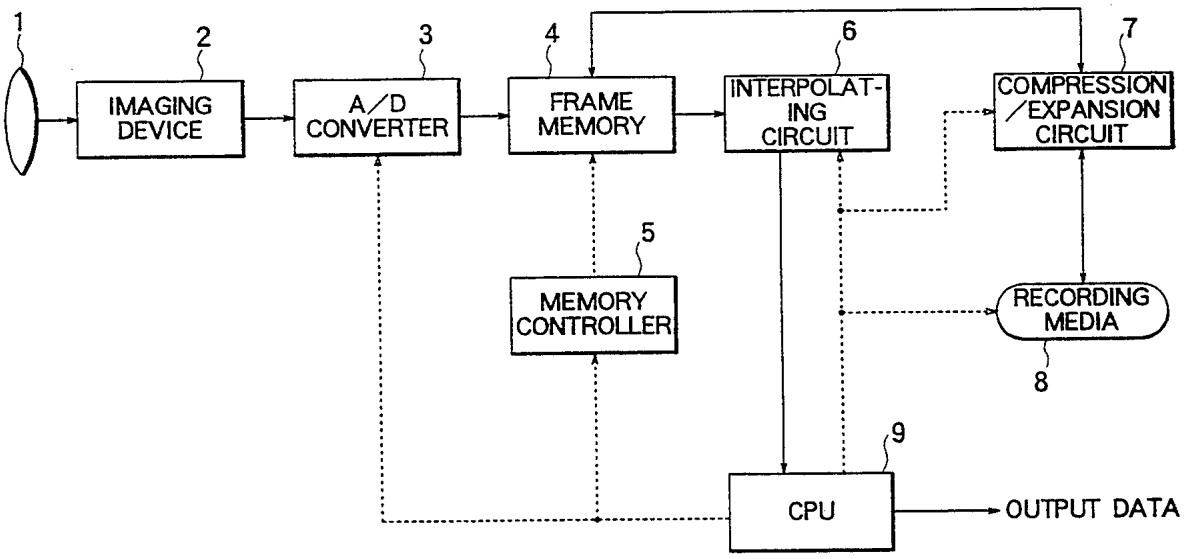


FIG. 1

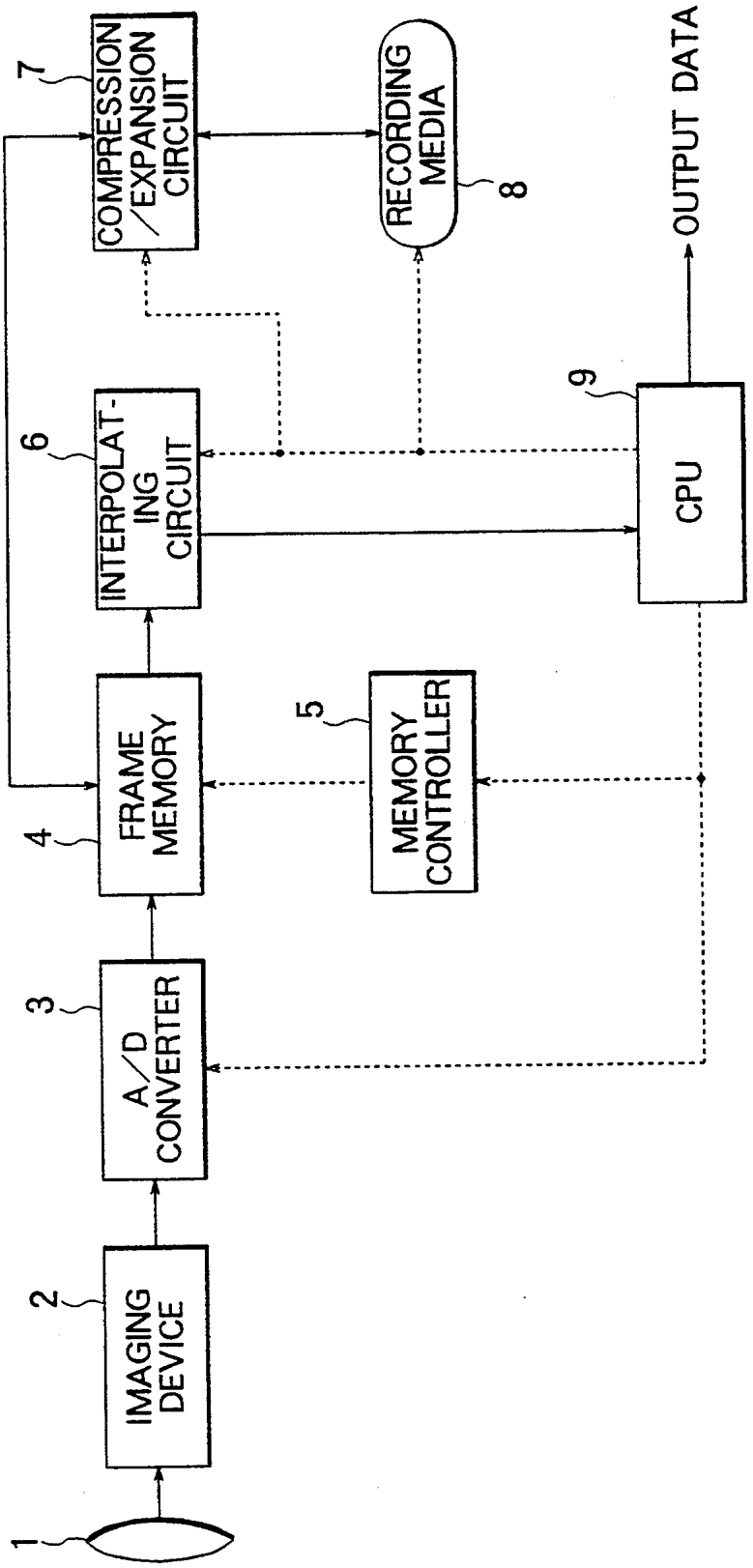

1
2
IMAGING DEVICE
3
A/D CONVERTER
4
FRAME MEMORY
5
MEMORY CONTROLLER
6
INTERPOLAT-ING CIRCUIT
7
COMPRESSION /EXPANSION CIRCUIT
8
RECORDING MEDIA
9
CPU
OUTPUT DATA

FIG. 2

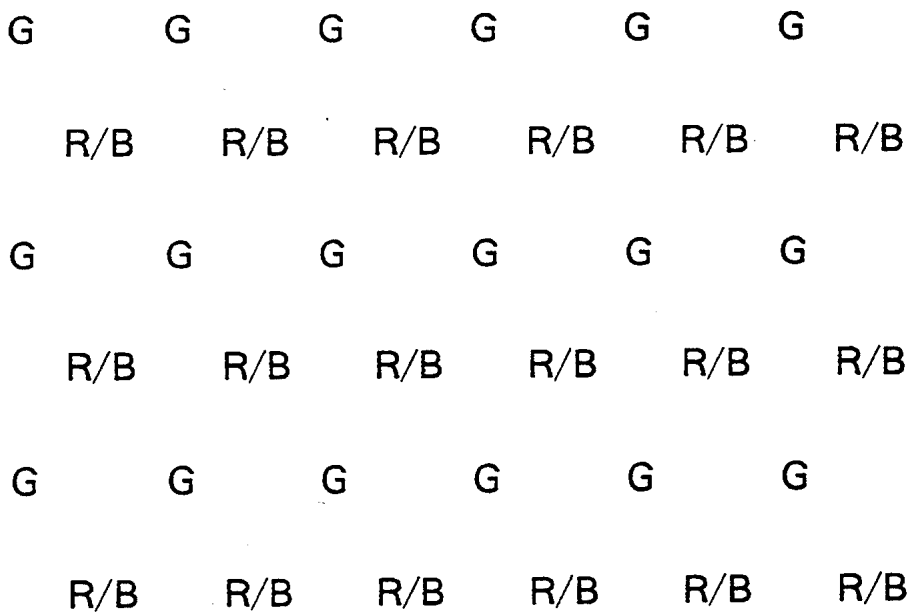

G G G G G G
R/B R/B R/B R/B R/B R/B
G G G G G G
R/B R/B R/B R/B R/B R/B
G G G G G G
R/B R/B R/B R/B R/B R/B

FIG. 3

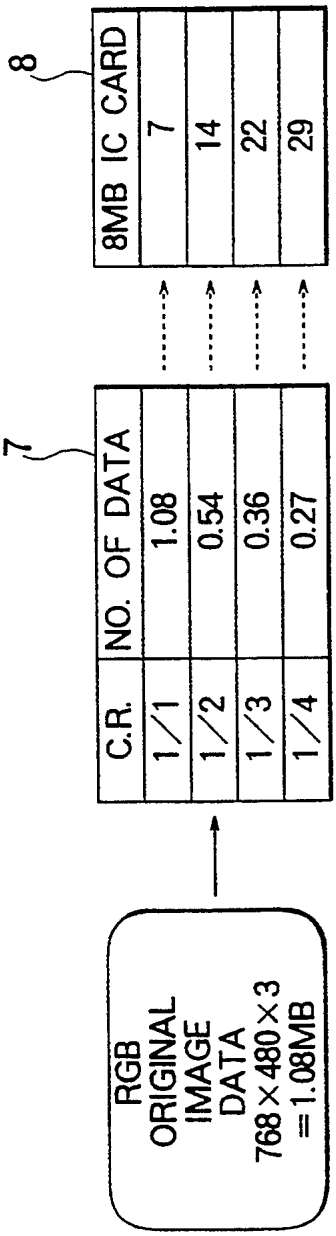

8
8MB IC CARD
7
14
22
29
7
C.R.
NO. OF DATA
1/1
1.08
1/2
0.54
1/3
0.36
1/4
0.27
RGB ORIGINAL IMAGE DATA 768×480×3 =1.08MB

FIG. 4

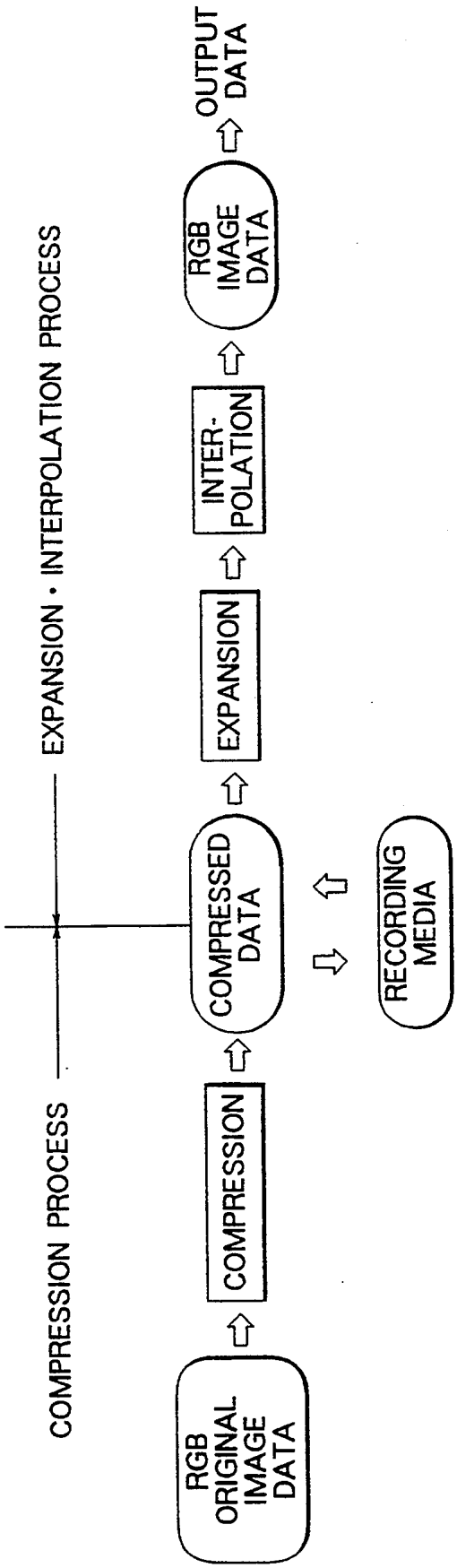

COMPRESSION PROCESS
EXPANSION • INTERPOLATION PROCESS
RGB ORIGINAL IMAGE DATA
COMPRESSION
COMPRESSED DATA
RECORDING MEDIA
EXPANSION
INTER-POLATION
RGB IMAGE DATA
OUTPUT DATA

FIG. 5

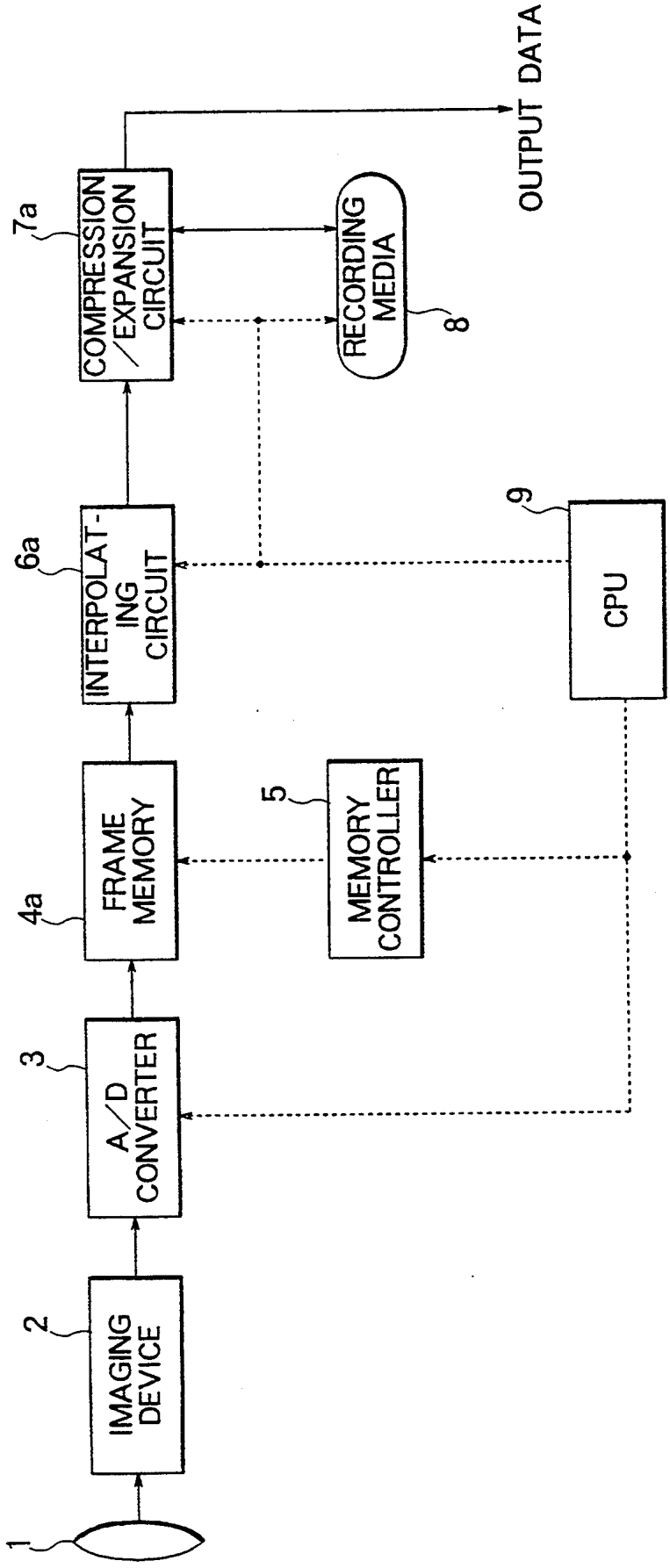

1
IMAGING DEVICE
2
A/D CONVERTER
3
FRAME MEMORY
4a
MEMORY CONTROLLER
5
INTERPOLAT-ING CIRCUIT
6a
COMPRESSION /EXPANSION CIRCUIT
7a
RECORDING MEDIA
8
CPU
9
OUTPUT DATA

FIG. 6

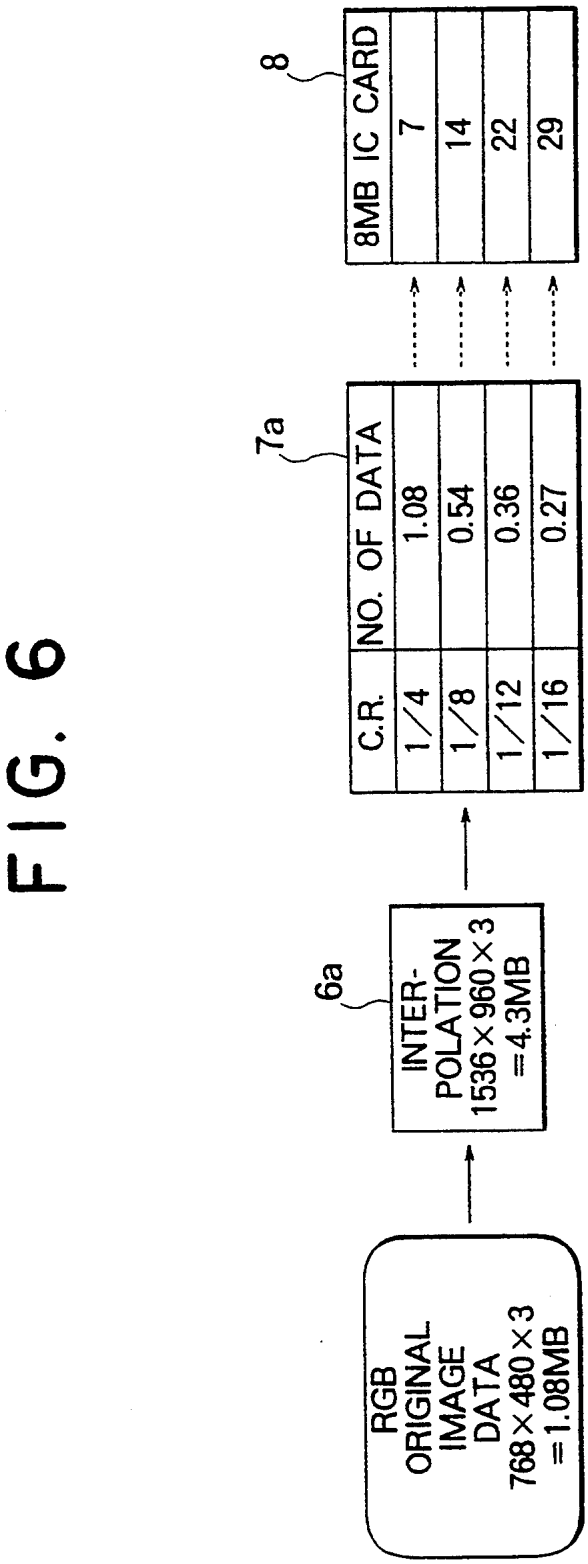
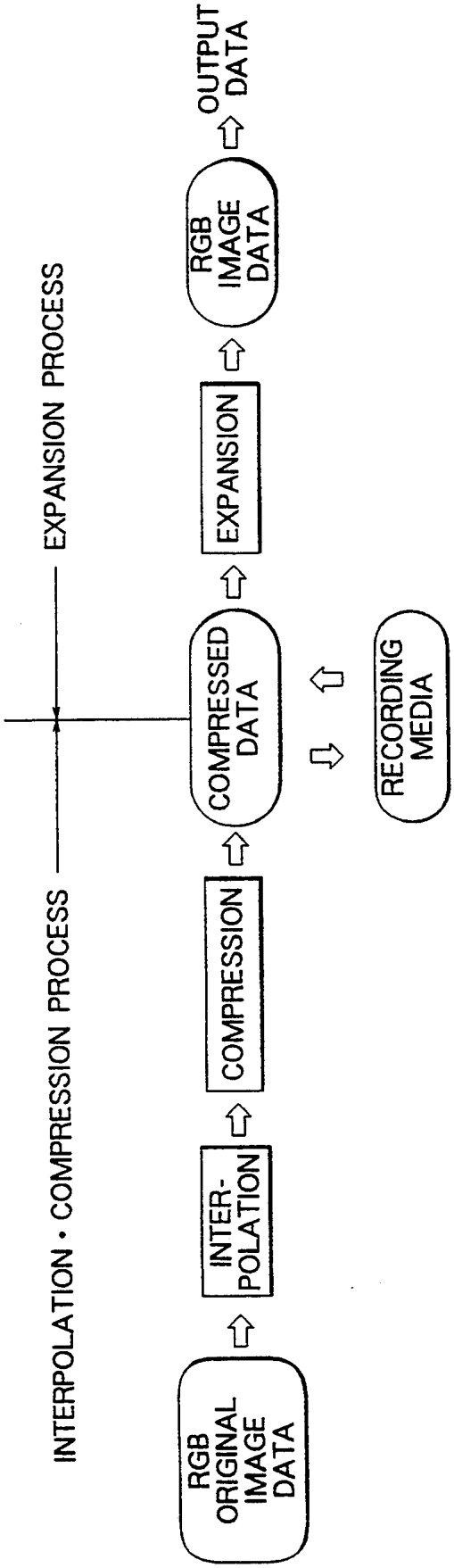

RGB ORIGINAL IMAGE DATA 768×480×3 =1.08MB
6a
INTER-POLATION 1536×960×3 =4.3MB
7a
C.R.
NO. OF DATA
1/4
1.08
1/8
0.54
1/12
0.36
1/16
0.27
8
8MB IC CARD
7
14
22
29

FIG. 7


INTERPOLATION • COMPRESSION PROCESS
EXPANSION PROCESS
RGB ORIGINAL IMAGE DATA
INTER-POLATION
COMPRESSION
COMPRESSED DATA
RECORDING MEDIA
EXPANSION
RGB IMAGE DATA
OUTPUT DATA

APPARATUS AND METHOD FOR STORING AND REPRODUCING DIGITAL IMAGE DATA YIELDING HIGH RESOLUTION AND HIGH QUALITY VIDEO IMAGE DATA

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of processing image data obtained by an imaging device and to an image data processing apparatus thereof. More particularly the present invention relates to an image data processing apparatus wherein image data is digitally processed and the resultant image data is stored in a recording medium, and to a method thereof.

2. Description of the Related Art

U.S. Pat. No. 4,541,016 discloses an electronic still camera in which an imaging device such as a solid state image sensor generates analog image data and the generated analog image data is recorded on a magnetic disc in an analog signal form. Such electronic still cameras provide a picture of the same as quality that in silver-halide-photography type cameras. Since the image data is recorded on a magnetic disc, the imagery produced by the electronic still camera inevitably suffers from jitter and resultant color stain (mixture). As a result, the reproduced image it suffers from the disadvantages of a low resolution and a low quality of the picture. Also, it suffers from the disadvantage of a large memory capacity required for storing the analog image data.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method of processing image data by which generation of jitter in processed image data and the resultant color stain (mixture) in the picture are prevented and to thereby to provide pictures of a high resolution and a high quality.

Another object of the present invention is to provide a method of processing image data which enables storage of a large amount of original image data with a small memory.

Still another object of the present invention is to provide an image processing apparatus using the above methods.

According to the present invention, there is provided an apparatus for processing an image data signal formed by at least three color components, including a conversion unit for converting analog intensities of the color component data of the image data signal to digital intensity color component data, a compression unit for compressing the digital color component data of the image data signal converted by the conversion unit at a predetermined rate including a compression rate of 1/1, and a storage unit for storing the compressed digital color component data of the image data signal by the compression means in a digital recording medium.

Further, according to the present invention, there is provided an apparatus for processing image data signal which has moreover a data reading unit for reading the digital color component data of the image data signal from the recording medium, an expansion unit for expanding the digital color component data of the image data signal read from the recording medium at a predetermined expansion rate, to reproduce expansion data substantially the same as the data before the compression, and an interpolating unit for generating data interpolating the digital color component data of the image data signal expanded by the expansion unit in a predetermined interpolation manner, to thereby provide reproduction image picture data having a predetermined resolution.

Further, according to the present invention, there is provided an apparatus for processing image data signal formed by at least three color components including a conversion unit for converting analog intensities of the color component data of the image data signal to digital intensity color component data, an interpolating unit for interpolating the digital color component data of the image data signal converted by the conversion unit by a predetermined interpolation manner, a compression unit for compressing the digital color component data of the image data signal interpolated by the interpolating unit at a predetermined rate including a compression rate of 1/1, and a storage means for storing the compressed digital color component data of the image data signal by the compression unit in a digital recording medium.

Further, according to the present invention, there is provided an apparatus for processing image data signal which has moreover a data reading unit for reading the digital color component data of the image data signal from the recording medium, and an expansion unit for expanding the digital color component data of the image data signal read from the recording medium at a predetermined expansion rate, to reproduce expansion data substantially the same as the data before the compression, to thereby provide reproduction image picture data having a predetermined resolution.

Further, according to the present invention, there is provided a method of processing an image data signal formed by at least three color components, which include the steps of converting analog intensities of the color component data of the image data signal to digital intensity color component data, compressing the digital color component data of the converted image data signal at a predetermined rate including a compression rate of 1/1, and storing the compressed digital color component of the image data signal by the compression means to a digital recording medium.

Further, according to the present invention, there is provided the method of processing an image data signal which includes moreover the steps of reading the digital color component data of the image data signal from the recording medium, expanding the digital color component data of the image data signal read from the recording medium at a predetermined expansion rate to reproduce expansion data substantially the same as the data before the compression, and generating data interpolating the expanded digital color component data of the image data signal in a predetermined interpolation manner, to thereby provide reproduction image picture data having a predetermined resolution.

Further, according to the present invention, there is provided a method of processing an image data signal formed by at least three color components, which includes the steps of converting analog intensities of the color component data of the image data signal to digital intensity color component data, generating data interpolating digital color component data on the basis of the converted digital color component data of the image data signal in a predetermined interpolation manner, compressing the interpolated digital color component data of the image data signal at a predetermined rate including a compression rate of 1/1, and storing the

compressed digital color component of the image data signal in a digital recording medium.

Further, according to the present invention, there is provided the method of processing an image data signal which includes moreover the steps of reading the digital color component data of the image data signal from the recording medium, and expanding the digital color component data of the image data signal read from the recording medium at a predetermined expansion rate, to reproduce expansion data substantially the same as the data before the compression, to thereby provide reproduction image picture having a predetermined resolution.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and features and other objects and features of the present invention will become clearer by the following description with reference to accompanying drawings, wherein:

FIG. **1** is a block diagram showing a first embodiment of an image data processing apparatus according to the present invention;

FIG. **2** is a view for explaining how three elementary colors can be generated by an imaging device of the image data processing apparatus in FIG. **1**;

FIG. **3** is a view for explaining the relationship among a compression rate, the amount of compressed data, and the number of pictures recorded in a recording medium in the image data processing apparatus in FIG. **1**;

FIG. **4** is a view for explaining operations of the image data processing apparatus in FIG. **1**;

FIG. **5** is a block diagram showing a second embodiment of an image data processing apparatus according to the present invention;

FIG. **6** is a view for explaining the relationship among a compression rate, the number of compressed data, and the amount of picture recorded in a recording media in the image data processing apparatus in FIG. **5**, and

FIG. **7** is a view for explaining operations of the image data processing apparatus in FIG. **5**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** is a block diagram showing a first embodiment of an image data processing apparatus, built in a digital electronic still camera, according to the present invention.

In FIG. **1**, **1** denotes an image formation lens, **2** an imaging device, **3** an analog/digital converter (A/D converter), **4** a frame memory, **5** a memory controller, **6** an interpolating circuit, **7** a data compression/expansion circuit, **8** a recording medium, and **9** a central processing unit (CPU).

The image formation lens **1** condenses light from an object not shown, and forms an image at an appropriate position of the imaging device **2**.

The imaging device **2**, for example, has a three plates type charge coupled device (CCD) which is provided with a plurality of R-CCDs, a plurality of G-CCDs, and plurality of B-CCDs, generates analog electric color signals of red(R), green(G), and blue(B), i.e., the three primary colors, according to a quantity (an intensity) of the received light, and outputs an analog image data on the basis of the intensity of the generated color signal.

As shown in FIG. **2**, in the three plate type CCD imaging device **2** of this embodiment, the G-CCDs are arranged at positions offset from the lattice of the R-CCDs and the B-CCDs. Specifically, the G-CCDs are arranged so that the pixel portions are shifted by a half pitch from the registration position of the R-CCDs and B-CCDs the in both horizontal and the vertical directions. In this embodiment, the R-CCDs and the B-CCDs are arranged at the same positions. This technology is disclosed in, for example, Japanese Unexamined Patent Publication (Kokai) 2(1990)-177672.

The A/D converter **3** converts red color analog intensities of the image data signal, blue color analog intensities of the image data signal, and green color analog intensities of the image data signal which are obtained from the imaging device **2**, to digital intensity signals.

The frame memory **4** stores the image data which is converted to the digital signals by the A/D converter **3**. The data is subjected to an expansion process in the data compression/expansion circuit **7**, under the control of the memory controller **5**.

The interpolating circuit **6** performs interpolation on the basis of the shift of the digital image data G which had been offset in the horizontal and vertical directions, which was output from the data compression/expansion circuit **7** and stored in the frame memory **4**. For example, when original image data of (768×480×3) pixels and a memory size thereof is 1.08 megabytes, according to the interpolation, high definition image data of (1536×960×3) pixels are obtained and a memory size thereof is 4.3 megabytes.

As shown in FIG. **2**, the interpolating circuit **6** performs interpolation of the image data to produce image data arranged in spaces, each positioned between the red and blue image data position, and the green image data position.

In the compression process, the data compression/expansion circuit **7** compresses the original image data of (768×480×3) pixels of 1.08 megabytes stored in the frame memory **4** in compression process, at a predetermined compression rate, for example 1/1 (no compression), 1/2, 1/3, 1/4 . . . The compressed image data is stored in the recording medium **8** under control of the CPU **9**.

The compression in the compression/expansion circuit **7** uses, for example, a two-dimensional discrete cosine transformation (DCT).

In the DCT method, for example, the digital image data in the frame memory **4** is divided into a plurality of blocks of N×N pixels. The data in the block is subjected to the two dimensional DCT, and the N×N pixel data is converted to N×N DCT transformed pixel data. The N×N DCT transformed data is quantized using a predetermined quantization table at a different step size for each coefficient position. The quantized data is coded to result in the compressed data.

Also, in the expansion-interpolation process, the data compression/expansion circuit **7** expands the compressed image data read from the recording medium **8** under the control of the CPU **9** at a predetermined expansion rate to restore the original image data. The compressed image data is converted to a picture signal of a predetermined format, and stores the picture signal is stored in the frame memory **4**.

The expansion process includes a process reverse of the above described DCT compression process.

The recording medium **8** records the image data compressed in the data compression/expansion circuit **7** under the control of the CPU **9** in the compression

process. And in the expansion-interpolation process, the recorded image data is read from the recording medium, and output to the data compression/expansion circuit 7 under the control of the CPU 9.

FIG. 3 shows the relationship among a compression rate, the amount of compressed data, and the number of pictures recorded in the recording mediums, for example, an integrated circuit (IC) card which includes a microprocessor for signal processing and a semiconductor memory for storing the compressed image data. If the IC card is portable, and then the IC card can be loaded on another apparatus for reproducing the image data.

As shown in FIG. 3, since the digital image data is compressed at a predetermined compression rate in the compression/expansion circuit 7, it is possible to store the reduced digital compression image data to the IC card.

In the embodiment, since the compression is performed prior to the predetermined interpolation process, it is possible to increase the compression rate compared with compression after interpolating. Also, it is also possible to increase the number of pictures able to be stored in the IC card by increasing the compression rate.

The CPU 9 controls the transmission and reception of data between the frame memory and the data compression/expansion circuit 7 and between the compression-/expansion circuit 7 and the recording medium 8. Also, the CPU 9 converts the image data output from the interpolating circuit 6 to a high definition picture signal having a predetermined format and outputs the picture signal as RGB image data.

Next, the operation by the above-described structure will by explained referring to FIG. 1 and FIG. 4.

Light from an object, not shown, is input to the image formation lens I and forms an image at an appropriate position of the imaging device 2. In the imaging device 2, a red color analog signal, blue color analog signal, and green color analog signal are generated according to the quantity (intensity) of the received light. These signals are subjected to a predetermined signal processing, and are output to the A/D converter 3 as the analog image data signal. As described above, the analog image data of the G-CCDs are shifted by a half pitch in the horizontal and vertical directions from a registration position of the R-CCDs and the B-CCDs.

In the A/D converter 3, the input red color analog image data, blue color analog image data, and green color analog image data are converted to red color digital image data, blue color digital image data, and green color digital image data, respectively. This digital image data is stored in the frame memory 4 as the RGB original image data.

The image data stored in the frame memory 4 of (768×480×3) pixels of 1.08 megabytes is read and output to the data compression/expansion circuit 7.

In the data compression/expansion circuit 7, the red color digital image data, the blue color digital image data, and the green color digital image data are subjected to a predetermined compression process at a predetermined compression rate, or are held as is, without compression when the compression rate is 1/1. The compressed or the non compressed image data are stored in the recording medium 8 under the control of the CPU 9.

When outputting the image data stored in the recording medium 8 to a display like a liquid crystal device or a printer, the desired red color digital image data, blue color image data, and green color image data are read from the appropriate recording areas of the recording medium 8 and output to the data compression/expansion circuit 7 under the control of the CPU 9.

In the data compression/expansion circuit 7, the compressed image data read from the recording medium 8 is expanded to restore it to the original image data at a predetermined expansion rate. The expanded image data is stored in the frame memory 4. The expanded image data stored in the frame memory 4 is read out and output to the interpolating circuit 6.

In the interpolating circuit 6, as the G data of the RGB original image data is shifted by a half pitch in the horizontal and vertical directions, the G data of the RGB original image data is subjected to interpolation on the basis of that shift, and then is output to the CPU 9 as image data of (1536×960×3) pixels of 4.3 megabytes.

In the CPU 9, the input image data is converted to picture signals having a predetermined format. The picture signals are output as RGB image data.

As explained above, according to the present embodiment, the electronic still camera obtains the analog pixel image data, converts the same to digital pixel image data, compresses the digital image data at a predetermined compression rate and stores the recording medium 8. In outputting the image data from the recording medium 8, the invention expands the stored image data, interpolate the expanded image data, and then output the interpolated image data. Due to this operation, it is possible to prevent the generation of jitter and the resultant color-stain and thus high resolution and high quality pictures are obtain.

Also, as the A/D converted image data is compressed directly, and the compressed image data is stored in the recording medium 8, therefore, when the IC card is used as the recording medium 8, it is possible to store a number of sets of image data on a single IC card and thus obtain a practical, broad-use apparatus.

Also, it is possible to perform interpolation of the digital image data, compress the interpolated digital image data, and then store the compressed image data in the recording medium 8. Alternatively, in the present embodiment, it is possible to increase the compression rate and, thereby reduce the time for the compression process, as compared with compression after interpolation.

It should be noted that, in the present embodiment, the imaging device required the the case of shifting of the positions of the pixels of three sets of CCD's in the horizontal and vertical directions as shown in FIG. 2 and the performing of a high definition signal process (interpolation process) to obtain high picture quality images. However, the present invention can be applied even to cameras with one or two set of CCD's by shifting the pixels in just one direction, such as the horizontal direction.

Also, in the present embodiment was explained using a DCT as the method at compression and an inverse DCT as the method of expansion. However, the present invention can also be applied to other a variety of coding and decoding methods for the compression and the expansion of data

Further, the present embodiment was explained through the use of the IC card as the recording medium. However, the present invention can also be applied to a

portable static memory card, a floppy disk, or other recording medium.

The present invention can also be applied even to the use of a portable recording medium, which can be loaded on another digital electronic still camera to move compressed digital image data and compression rate data thereon. When it is loaded in another electronic still camera, the compressed digital image data and compression rate data are read from the loaded recording medium. The read data is expanded in the data compression/expansion circuit at an expansion rate based on the stored compression rate data to reproduce expansion data substantially the same as the data before compression. The expanded data is interpolated in a predetermine interpolation manner to generate picture signals, and the picture signals are output as RGB image data.

FIG. **5** is a block diagram showing a second embodiment of an image data processing apparatus according to the present invention.

Note that, in FIG. **5**, the reference numerals are the same as shown in FIG. **1** and indicate the same component of the apparatus. Therefore, explanation of these components is omitted.

The frame memory **4***a* stores image data converted to digital signals by the A/D converter **3** under the control of the memory controller **5**.

The interpolating circuit **6***a* performs the interpolation to shift the digital image data G, output from the A/D converter **3** and stored in the frame memory **4***a*, the horizontal and vertical directions. Original image data of (768×480×3) pixels and 1.08 megabytes would thus obtain the high definition image data of (1536×960×3) pixels of 4.3 megabytes.

The interpolation in the interpolating circuit **6***a* is as same as in the interpolating circuit **6** in FIG. **1**.

The data compression/expansion circuit **7***a* compresses the 4.3 megabyte image data which is interpolated in the interpolating circuit **6***a*, at a predetermined compression rate, for example, 1/4, 1/8, 1/12, 1/16 . . . The compressed image data is stored in the recording medium **8**.

In the expansion process, the data compression/expansion circuit **7***a* expands the compressed image data read from the recording medium **8** under the control of the CPU **9** at a predetermined expansion rate to restore the original image data, converts the image data to picture signals of a predetermined format, and outputs the picture signals as the RGB image data.

The compression and expansion operation of the data compression/expansion circuit **7***a* is the same as the data compression/expansion circuit **7** in FIG. **1**.

The recording medium **8** records the image data compressed in the data compression/expansion circuit **7***a* under the control of the CPU **9**. In the expansion process, the recorded image data is read from the recording medium **8** and output to the data compression/expansion circuit **7***a* under the control of the CPU **9**.

FIG. **6** shows the relationship among a compression rate, the amount of compressed data and the number of pictures recorded in the recording medium **8**, e.g., an 8 megabyte IC card.

As shown in FIG. **6**, since the digital image data is compressed at a given compression rate in the compression/expansion circuit **7***a* and the compressed image data is recorded in the recording medium **8**, it is possible to store a plurality of the picture data on the IC card. Also, it is possible to expand the quantity of picture data stored on the IC card by more increasing the compression rate.

Next, the operation by the above-described structure will be explained referring to FIG. **5** and FIG. **7**.

Light from an object, not shown, is input to the image formation lens I and forms an image at an appropriate position of the imaging device **2**. In the imaging device **2**, a red color analog signal, blue color analog signal, and green color analog signal are generated according to the quantity (intensity) of light received. These signals are subjected to predetermined processing, and are output to the A/D converter **3** as the analog image data signal. As described above, these analog image data of the G-CCDs are shifted by a half pitch in the horizontal and vertical directions from the registration position of the R-CCDs and B-CCDs.

In A/D converter **3**, the input red color analog image data, blue color analog image data, and green color analog image data are converted to red color digital image data, blue color digital image data, and green color digital image data, respectively. This digital image data **13** stored in the frame memory **4***a* as the RGB original image data.

The image data stored in the frame memory **4***a* of (768×480×3) pixels of 1.08 megabytes is read, and output to the interpolating circuit **6***a*.

In the interpolating circuit **6***a*, as the G's of the RGB original image data are shifted in the horizontal and vertical directions, the G's of RGB original image data are subjected to interpolation on the basis of the position shift, and then output to the data compression/expansion circuit **7***a* as image data of (1536×960×3) pixels of 4.3 megabytes.

In the data compression/expansion circuit **7***a*, the red color digital image data, the blue color digital image data, and the green color digital image data are subjected to a predetermined compression process at a predetermined compression rate. The compressed image data is stored in the recording medium **8** under the control of the CPU **9**.

When outputting the image data stored in the recording medium **8** to a display like a liquid crystal device or a printer, the desired red color digital image data, blue color image data, and green color image data are read from the appropriate recording areas of the recording medium **8** and output to the data compression/expansion circuit **7***a* under the control of the CPU **9**.

In the data compression/expansion circuit **7***a*, the compressed image data read from the recording medium **8** **13** expanded to restore it to the original image data at a predetermined expansion rate. The expanded image data is converted to picture signals of a given format which are output as the RGB image data.

As explained above, according to the present embodiment, the electronic still camera produces the analog pixels image data, converts them to digital image data, interpolate the digital image data, and compresses the interpolated image data at a predetermined compression rate for storage. In the output operation, the invention expands the stored image data and then outputs it, Thereby, it is possible to prevent the generation of jitter and the resultant color-stain, and thus it is possible to obtain high resolution and high quality pictures.

Also, when the interpolated image data is compressed directly and the compressed image data is stored in the recording medium **8**, such as an IC card, it is possible to store a plurality of image data on the IC card and thus is possible to obtain a practical, broad-use apparatus.

Note that, in the present embodiment explained, wherein the imaging device required the shifting of the pixels of three sets of CCD's in the horizontal and vertical directions and the performing of a high definition signal process (interpolation process) to obtain the high picture quality images. However, the present invention can be applied even to cameras with one or two sets of CCD's by shifting the pixels in just one directional,such as the horizontal direction.

Also, because the interpolated image data is compressed directly, and the compressed image data is stored in the recording means, such as an IC card, it is possible to store a plurality of image data on a IC card and is thus possible to obtain a practical, broad-use apparatus.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not restricted to the specific embodiments described above.

What is claim is:

1. An apparatus for processing an image data signal formed of at least three color components, each having an analog intensity, produced by an imaging means having first image generation elements and second image generation elements arranged at the same registration positions on a two dimensional plane, said first image generation elements and said second image generation elements being spaced at a predetermined pitch in two orthogonal directions, and third image generation elements arranged at positions shifted by a half pitch from the registration position of said first and second image generation elements in said two orthogonal directions, comprising:

conversion means for converting the analog intensities of said color components of said image data signal to digital color component data;

compression means for compressing said digital color component data at a predetermined rate greater than 1/1, whereby when said predetermined rate is 1/1 said image data signal is not compressed;

storage means for storing said compressed digital color component data on a digital recording medium;

data reading means for reading said digital color component data from said digital recording medium;

expansion means for expanding said digital color component data read from said digital recording medium at a predetermined expansion rate, to produce expanded data substantially the same as the digital color component data before compression; and

interpolation means for interpolating at least one image data representing an intensity of an image generation element arranged between two adjacent image generation elements in a first direction and between two adjacent image generation elements in a second direction, said second direction being orthogonal to said first direction, by using said expanded digital color component data representing the intensities of said adjacent image generation elements to thereby provide reproduced image picture data having a predetermined resolution.

2. An apparatus according to claim **1**, further comprising timing adjusting means for adjusting a timing of said interpolated color component data as a function of the positions of said first, second and third image generation elements.

3. An apparatus according to claim **1**, further comprising picture reproduction means responsive to the interpolated image data for reproducing a picture substantially the same as an original picture.

4. An apparatus according to claim **1**, wherein said compression means compresses said digital color component data as a function of the quantity of said image data.

5. An apparatus according to claim **1**, wherein said compression means compresses said digital color component data as a function of the arrangement of said image generation elements.

6. An apparatus according to claim **1**, wherein said digital recording medium comprises a static memory.

7. An apparatus according to claim **1**, wherein said digital recording medium comprises a memory card.

8. An apparatus according to claim **1**, wherein said storage means and said digital recording medium are integrated as an integrated circuit card.

9. An apparatus according to claim **1**, wherein said expansion means expands said digital color component data as a function of the quantity of said image data.

10. An apparatus according to claim **1**, wherein said expansion means expands said digital color component data as a function of the arrangement of said image generation elements.

11. An apparatus according to claim **1**, wherein said three color components comprise red, green and blue color components.

12. An apparatus according to claim **11**, wherein said first image generation elements and said second image generation elements generate red image data and blue image data, respectively, and said third image generation elements generate green image data.

13. An apparatus according to claim **1**, wherein said apparatus is an electronic camera.

14. An apparatus according to claim **1**, wherein said apparatus is an electronic still camera for processing substantially still image data.

15. An apparatus for processing digital color component image data derived from at least three color components, each having an analog intensity, produced by an imaging means having first image generation elements and second image generation elements arranged at the same registration positions on a two dimensional plane, said first image generation elements and said second image generation elements being spaced at a predetermined pitch in two orthogonal directions, and third image generation elements arranged at positions shifted by a half pitch from the registration position of said first and second image generation elements in said two orthogonal directions, the digital color component image data being recorded in compressed form on a digital recording medium, comprising:

data reading means for reading said compressed digital color component image data from said digital recording medium;

expansion means for expanding said digital color component image data read from said recording medium at a predetermined expansion rate, to produce expanded data substantially the same as the digital color component image data before compression; and

interpolating means for interpolating at least one image data representing an intensity of an image generation element arranged between two adjacent image generation elements in a first direction and between two adjacent image generation elements

in a second direction, said second direction being orthogonal to said first direction, by using said expanded digital color component image data representing the intensities of said adjacent image generation elements to thereby provide reproduced image picture having a predetermined resolution.

16. An apparatus according to claim **15**, further comprising timing adjusting means for adjusting a timing of said interpolated color component data as a function of the positions of said first, second and third image generation elements.

17. An apparatus according to claim **15**, further comprising picture reproduction means responsive to the interpolated data for reproducing a picture substantially the same as an original picture.

18. An apparatus according to claim **15**, wherein said digital recording medium comprises a static memory.

19. An apparatus according to claim **15**, wherein said digital recording medium comprises a memory card.

20. An apparatus according to claim **15**, wherein said expansion means expands said digital color component image data as a function of the quantity of said image data.

21. An apparatus according to claim **15**, wherein said expansion means expands said digital color component image data as a function of the arrangement of said image generation elements.

22. An apparatus according to claim **15**, wherein said three color components comprise red, green and blue color components.

23. An apparatus according to claim **22**, wherein said first image generation elements and said second image generation elements generate red image data and blue image data, respectively, and said third image generation elements generate green image data.

24. An apparatus according to claim **15**, wherein compression rate data representing the compression of said recorded compressed digital color component image data are recorded on and read from said digital recording medium; and

wherein said expansion means expands said digital color component image data read from said digital recording medium at an expansion rate determined by said compression rate data read from said digital recording medium.

25. An apparatus for processing an image data signal formed of at least three color components, each having an analog intensity, produced by an imaging means having first image generation elements and second image generation elements arranged at the same registration positions on a two dimensional plane, said first image generation elements and said second image generation elements being spaced at a predetermined pitch in two orthogonal directions, and third image generation elements arranged at positions shifted by half a pitch from the registration position of said first and second image generation elements in said two orthogonal directions, comprising:

conversion means for converting the analog intensities of said color components of said image data signal to digital color component data;

interpolation means for interpolating at least one image data representing an intensity of an image generation element arranged between two adjacent image generation elements in a first direction and between two adjacent image generation elements in a second direction, said second direction being orthogonal to said first direction, by using said digital color component data representing the intensities of said adjacent image generation elements;

compression means for compressing said interpolated digital color component data at a predetermined rate greater than 1/1, whereby when said predetermined rate is 1/1 said image data signal is not compressed;

storage means for storing said compressed digital color component data on a digital recording medium;

data reading means for reading said digital color component data from said digital recording medium; and

expansion means for expanding said digital color component data read from said digital recording medium at a predetermined expansion rate, to produce expanded data substantially the same as the digital color component data before compression.

26. An apparatus according to claim **25**, further comprising timing adjusting means for adjusting a timing of said interpolated color component data as a function of the positions of said first, second and third image generation elements.

27. An apparatus according to claim **25**, further comprising picture production means responsive to the expanded data for reproducing a picture substantially the same as an original picture.

28. An apparatus according to claim **25**, wherein said compression means compresses said digital color component data as a function of the quantity of said image data.

29. An apparatus according to claim **25**, wherein said compression means compresses said digital color component data as a function of the arrangement of said image generation elements.

30. An apparatus according to claim **25**, wherein said digital recording medium comprises a static memory.

31. An apparatus according to claim **25**, wherein said digital recording medium comprises a memory card.

32. An apparatus according to claim **25**, wherein said storage means and said digital recording medium are integrated as an integrated circuit card.

33. An apparatus according to claim **25**, wherein said expansion means expands said digital color component data as a function of the quantity of said image data.

34. An apparatus according to claim **25**, wherein said expansion means expands said digital color component data as a function of the arrangement of said image generation elements.

35. An apparatus according to claim **25**, wherein said three color components comprise red, green and blue color components.

36. An apparatus according to claim **35**, wherein said first image generation elements and said second image generation elements generate red image data and blue image data, respectively, and said third image generation elements generate green image data.

37. An apparatus according to claim **25**, wherein said apparatus is an electronic camera.

38. An apparatus according to claim **25**, wherein said apparatus is an electronic still camera for processing substantially still image data.

39. An apparatus for processing an image data signal formed of at least three color components, each having an analog intensity, produced by an imaging means having first image generation elements and second image generation elements arranged at the same regis-

tration positions on a two dimensional plane, said first image generation elements and said second image generation elements being spaced at a predetermined pitch in two orthogonal directions, and third image generation elements arranged at positions shifted by a half pitch from the registration positions of said first and second image generation elements in said two orthogonal directions, comprising:

conversion means for converting the analog intensities of said color components of said image data signal to digital color component data;

interpolating means for interpolating at least one image data representing an intensity of an image generation element arranged between two adjacent image generation elements in a first direction and between two adjacent image generation elements in a second direction, said second direction being orthogonal to said first direction, by using said digital color component data representing the intensities of said adjacent image generation elements;

compression means for compressing said interpolated digital color component data at a predetermined rate greater than 1/1, whereby when said predetermined rate is 1/1 said image data signal is not compressed; and

storage means for storing said compressed digital color component data on a digital recording medium.

40. An apparatus according to claim **39**, further comprising timing adjusting means for adjusting a timing of said interpolated color component data as a function of the positions of said first, second and third image generation elements.

41. An apparatus according to claim **39**, wherein said compression means compresses said digital color component data as a function of the quantity of said image data.

42. An apparatus according to claim **39**, wherein said compression means compresses said digital color component data as a function of the arrangement of said image generation elements.

43. An apparatus according to claim **39**, wherein said digital recording medium comprises a static memory.

44. An apparatus according to claim **39**, wherein said digital recording medium comprises a memory card.

45. An apparatus according to claim **39**, wherein said storage means and said digital recording medium are integrated as an integrated circuit card.

46. An apparatus according to claim **39**, wherein said three color components comprise red, green and blue color components.

47. An apparatus according to claim **46**, wherein said first image generation elements and said second image generation elements generate red image data and blue image data, respectively, and said third image generation elements generate green image data.

48. A method of processing an image data signal formed of at least three color components, each having an analog intensity, produced by an imaging means having first image generation elements and second image generation elements arranged at the same registration positions on a two dimensional plane, said first image generation elements and said second image generation elements being spaced at a predetermined pitch in two orthogonal directions, and third image generation elements being arranged at positions shifted by a half pitch from the registration position of said first and second image generation elements in said two orthogonal directions, comprising the steps of:

converting the analog intensities of said color components of said image data signal to digital intensity color component data;

compressing said digital color component data at a predetermined rate greater than 1/1, whereby when said predetermined rate is 1/1 said image data signal is not compressed;

storing said compressed digital color component on a digital recording medium;

reading said digital color component data from said digital recording medium;

expanding said digital color component data read from said digital recording medium at a predetermined expansion rate, to produce expanded data substantially the same as the digital color component data before compression; and

interpolating at least one image data representing an intensity of an image generation element arranged between two adjacent image generation elements in a first direction and between two adjacent image generation elements in a second direction, said second direction being orthogonal to said first direction, by using said expanded digital color component data representing the intensities of said adjacent image generation elements to thereby provide reproduced image picture data having a predetermined resolution.

49. A method according to claim **48**, further including the step of adjusting a timing of said interpolated color component data as a function of the positions of said first, second and third image generation elements.

50. A method according to claim **48**, further including the step of responding to the interpolated image data to reproduce a picture substantially the same as an original picture.

51. A method of processing an image data signal formed of at least three color components, each having an analog intensity, produced by an imaging means having first image generation elements and second image generation elements arranged at the same registration positions on a two dimensional plane, said first image generation elements and said second image generation elements being spaced at a predetermined pitch in two orthogonal directions, and third image generation elements arranged at positions shifted by a half pitch from the registration position of said first and second image generation elements in said two orthogonal directions, comprising the steps of:

converting the analog intensities of said color components of said image data signal to digital color component data;

interpolating at least one image data representing an intensity of an image generation element arranged between two adjacent image data generation elements in a first direction and between two adjacent image generation elements in a second direction, said second direction being orthogonal to said first direction, by using said digital color component data representing the intensities of said adjacent image generation elements;

compressing said interpolated digital color component data at a predetermined rate greater than 1/1, whereby when said predetermined rate is 1/1 said image data signal is not compressed;

storing said compressed digital color component data on a digital recording medium;

reading said digital color component data from said recording medium; and

expanding said digital color component data read from said digital recording medium at a predetermined expansion rate, to produce expanded data substantially the same as the digital color component data before compression, thereby providing image picture data having a predetermined resolution.

52. A method according to claim **51**, further including the step of adjusting a timing of said interpolated color component data as a function of the positions of first, second and third image generation elements.

53. A method according to claim **51**, further including the step of responding to said image picture data to produce a picture substantially the same as an original picture.

* * * * *

EXHIBIT B

US005523795A

United States Patent [19]

Ueda

[11] Patent Number: 5,523,795

[45] Date of Patent: Jun. 4, 1996

[54] **METHOD AND APPARATUS FOR SERIAL TRANSMISSION AND/OR RECEPTION OF NONSYNCHRONOUS, MULTIPLEXED SIGNALS**

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[73] Assignee: **Sony Corporation**, Tokyo, Japan

[21] Appl. No.: **291,194**

[22] Filed: **Aug. 16, 1994**

[30] **Foreign Application Priority Data**

Aug. 24, 1993 [JP] Japan 5-231019

[51] **Int. Cl.**[6] **H04N 7/52**; H04N 7/54

[52] **U.S. Cl.** **348/480**; 348/472; 348/489; 348/434; 348/423; 348/515

[58] **Field of Search** 348/423, 434, 348/435, 480, 481, 482, 483, 484, 485, 479, 478, 477, 472, 462, 465, 464, 467, 512, 515, 516, 537, 432, 474, 473, 489, 495, 496, 517–519, 520, 524, 521, 546, 540, 536; 358/320, 339, 343; 370/112, 110.1, 111, 77, 100.1, 105.1; 375/354, 362; H04N 7/52, 7/54, 7/56, 7/60, 7/62, 7/04, 7/015

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,755,624	8/1973	Sekimoto	348/479
3,988,528	10/1976	Yanagimachi et al.	348/481
4,542,406	9/1985	Shimoyama et al.	348/484
4,544,950	10/1985	Tu	348/485
4,706,109	11/1987	Murray	348/481
4,851,909	7/1989	Noske et al.	348/512
5,113,242	5/1992	Tsinberg et al.	348/489
5,138,440	8/1992	Radice	358/13
5,199,030	3/1993	Ueda	370/68
5,231,492	7/1993	Dangi et al.	348/423
5,287,182	2/1994	Haskell et al.	348/484

FOREIGN PATENT DOCUMENTS

0488225A2	11/1991	European Pat. Off.	H04J 3/06
0598295A1	11/1993	European Pat. Off.	H04N 7/13

OTHER PUBLICATIONS

SMPTE Journal, vol. 102, No. 10, Oct. 1993, Scarsdale, New York, U.S.A., pp. 905–909; K. Y. Reynolds, et al., "Multiplexing and Demultiplexing Digital Audio and Video in Today's Digital Environment".

4:2:2 Digital Video: Background and Implementation, 1989, SMPTE, White Plains, New York, U.S.A., pp. 77–82; K. P. Davies, "Some Concepts for the Digital Television Studio".

SMPTE Journal, vol. 102, No. 2, Feb. 1993, Scarsdale, New York, U.S.A., pp. 174–179; "Proposed SMPTE Standard 259M".

Signal Processing Image Communication, vol. 4, No. 2, May 1992, pp. 153–159; A. G MacInnis, "the MPG System Coding Specification".

Primary Examiner—Safet Metjahic

Attorney, Agent, or Firm—Limbach & Limbach

[57] **ABSTRACT**

A method and an apparatus capable of transmitting and receiving multiplexed signals as serial data in such a manner that, even in a state where a continuous signal such as an audio digital signal is not in synchronism with another signal such as a video digital signal, the continuous signal can be properly reproduced on a reception side. Address data based on a word clock of another digital signal is sampled on a transmission side in accordance with a sampling clock of the continuous signal, and the sampled address value is included in the multiplexed signals to be thereby transmitted together to the reception side. Then on the reception side, a word clock synchronously locked to the word clock of the transmission-side another digital signal is reproduced from the received serial data, and address data is generated on the basis of the reproduced word clock, so that the reception-side clock of the continuous signal is reproduced from the generated address data and the transmitted address value included in the multiplexed signals, whereby the continuous signal is reproduced in accordance with the clock thus reproduced.

11 Claims, 5 Drawing Sheets

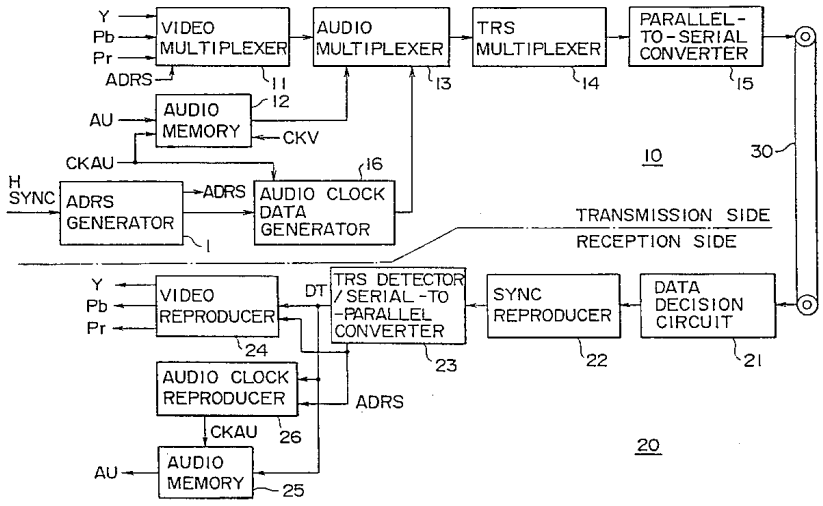
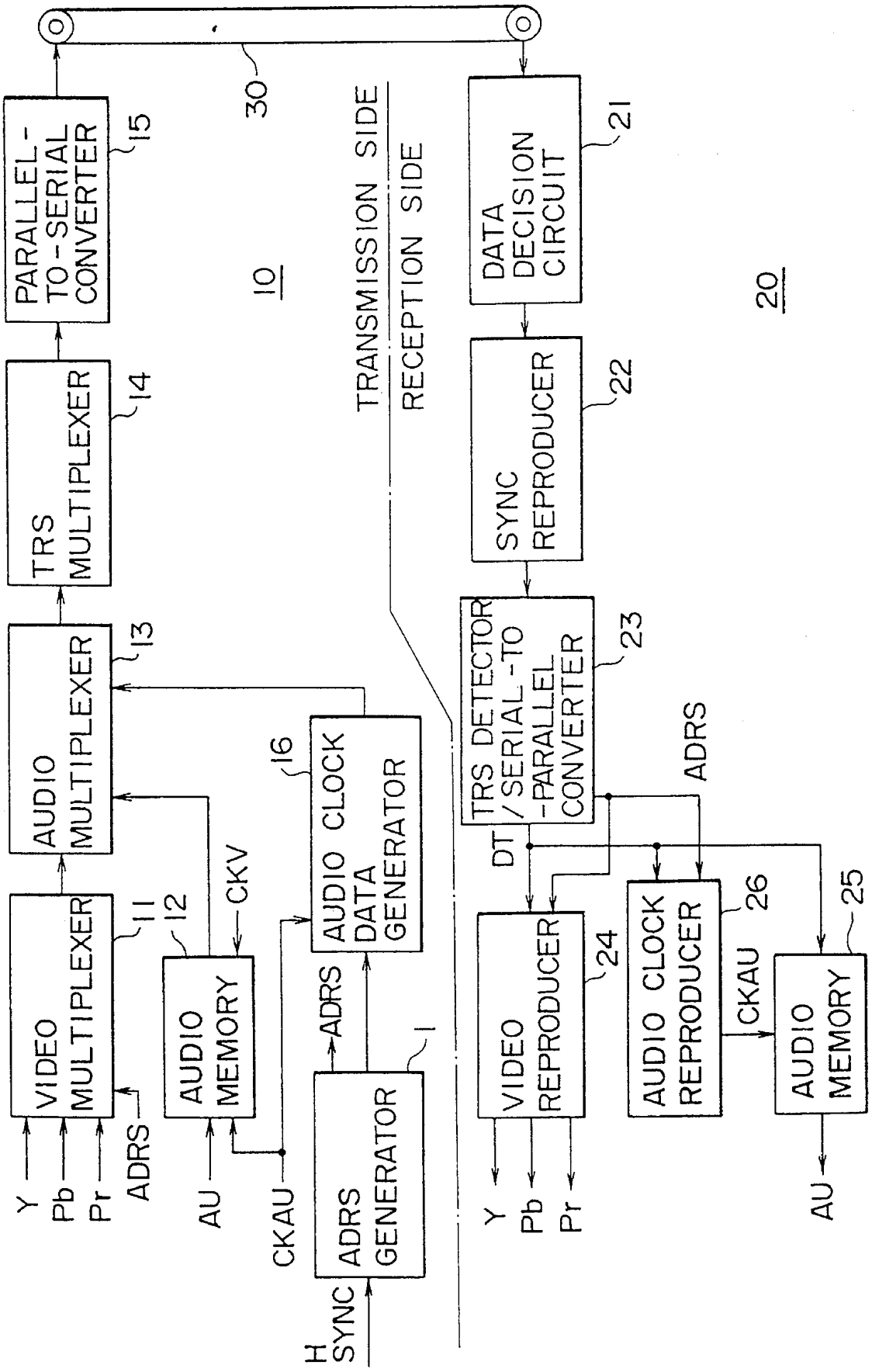


FIG. 1


30
TRANSMISSION SIDE
RECEPTION SIDE
10
20
PARALLEL-TO-SERIAL CONVERTER
15
TRS MULTIPLEXER
14
AUDIO MULTIPLEXER
13
VIDEO MULTIPLEXER
11
AUDIO MEMORY
12
CKV
AUDIO CLOCK DATA GENERATOR
16
ADRS GENERATOR
1
ADRS
Y
Pb
Pr
ADRS
AU
CKAU
H SYNC
DATA DECISION CIRCUIT
21
SYNC REPRODUCER
22
TRS DETECTOR / SERIAL-TO-PARALLEL CONVERTER
23
DT
ADRS
VIDEO REPRODUCER
24
AUDIO CLOCK REPRODUCER
26
AUDIO MEMORY
25
CKAU
Y
Pb
Pr
AU

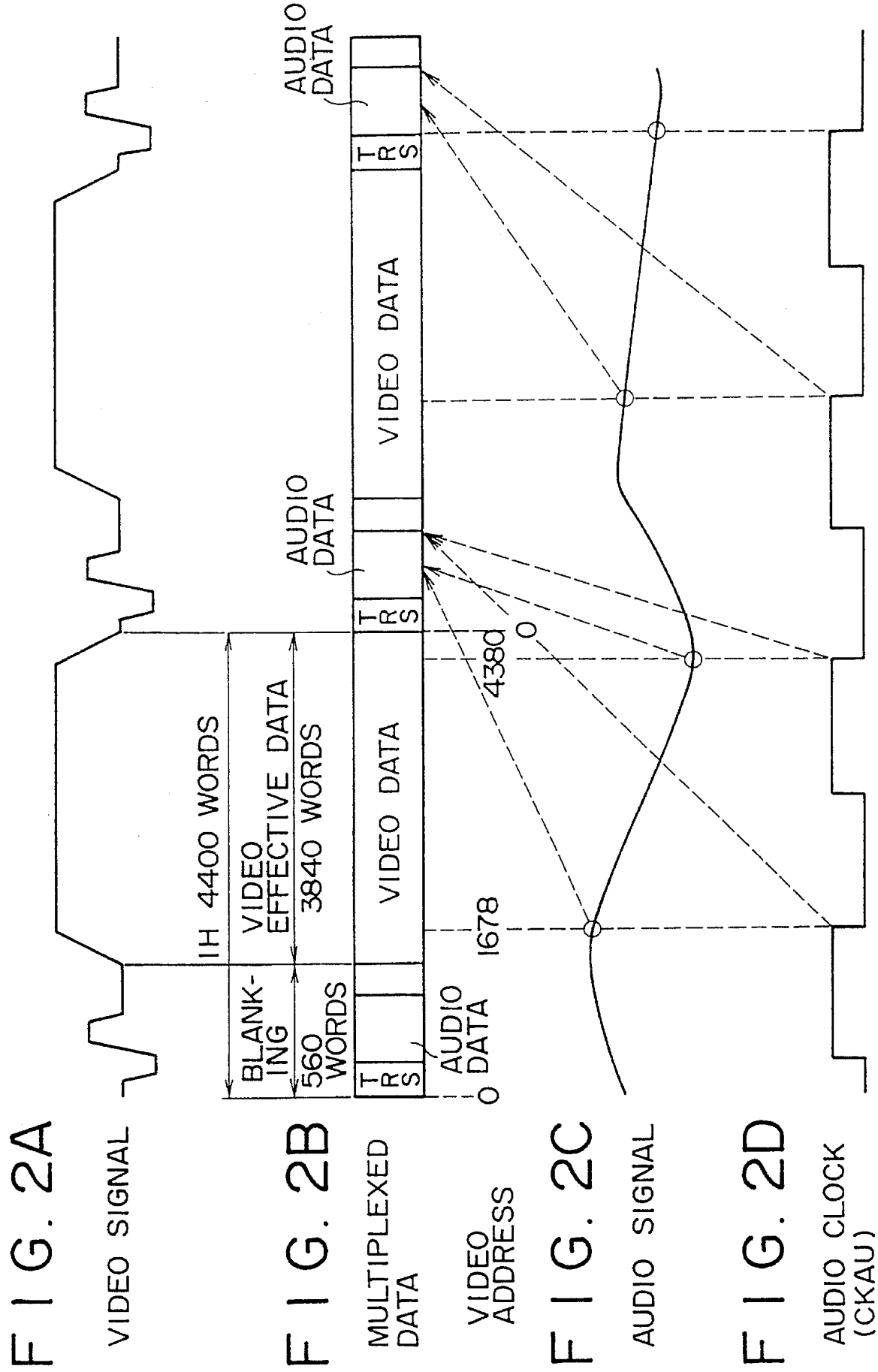


FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

FIG. 3

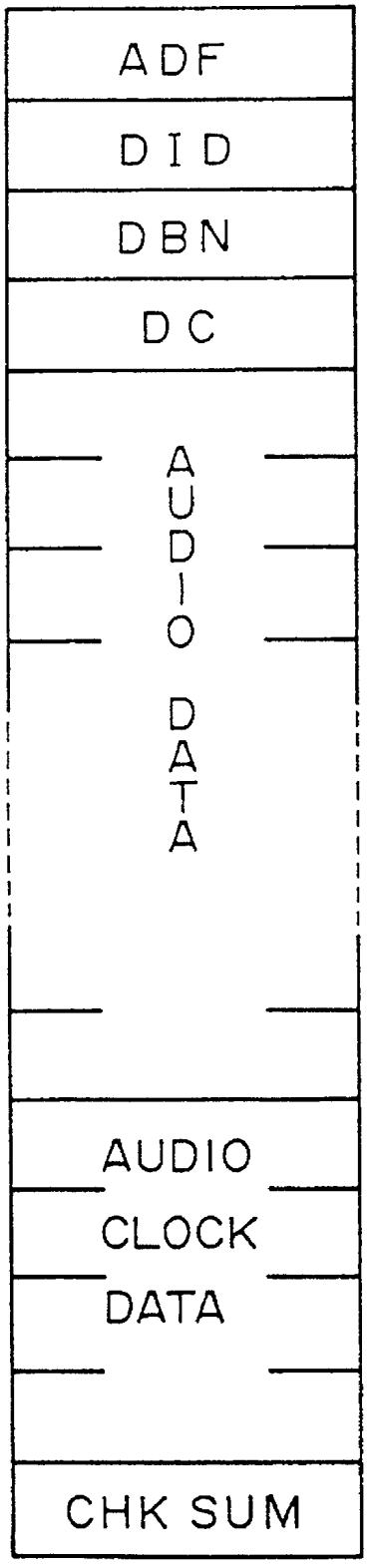


FIG. 4

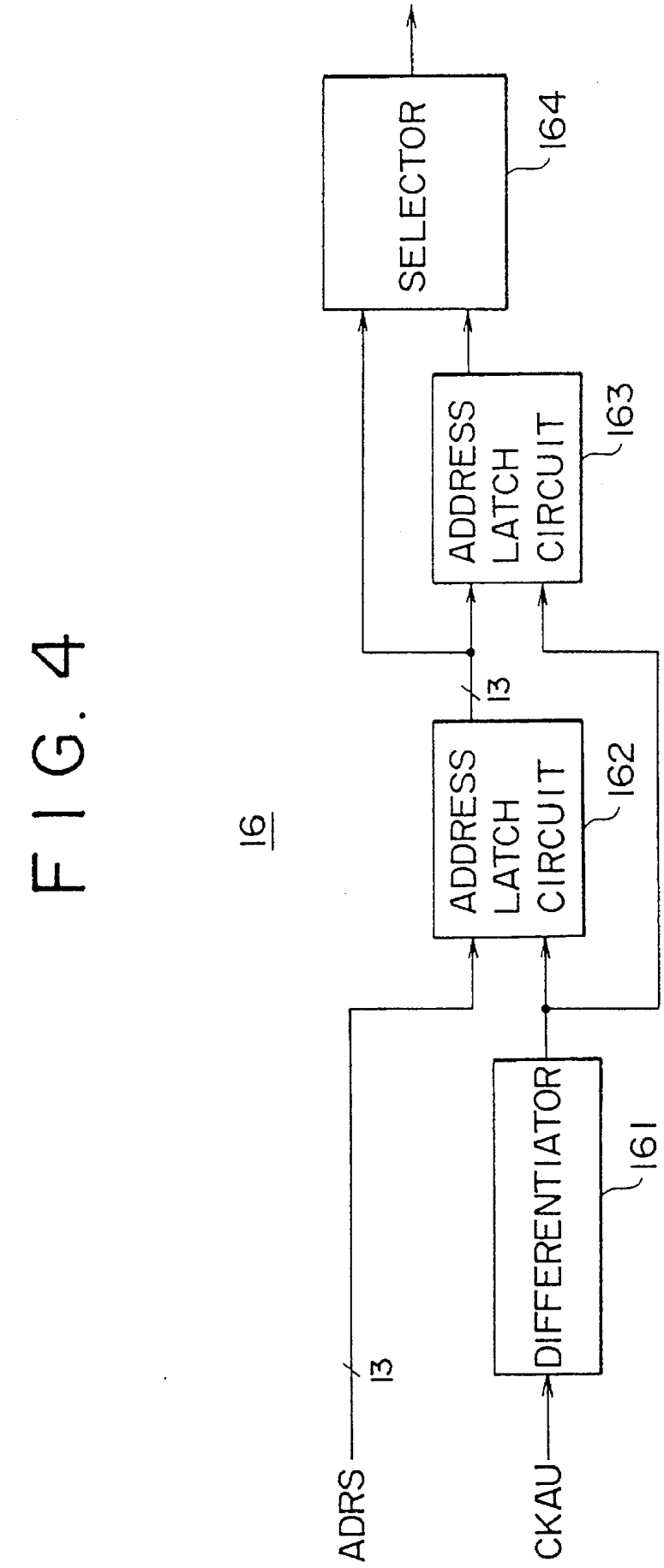
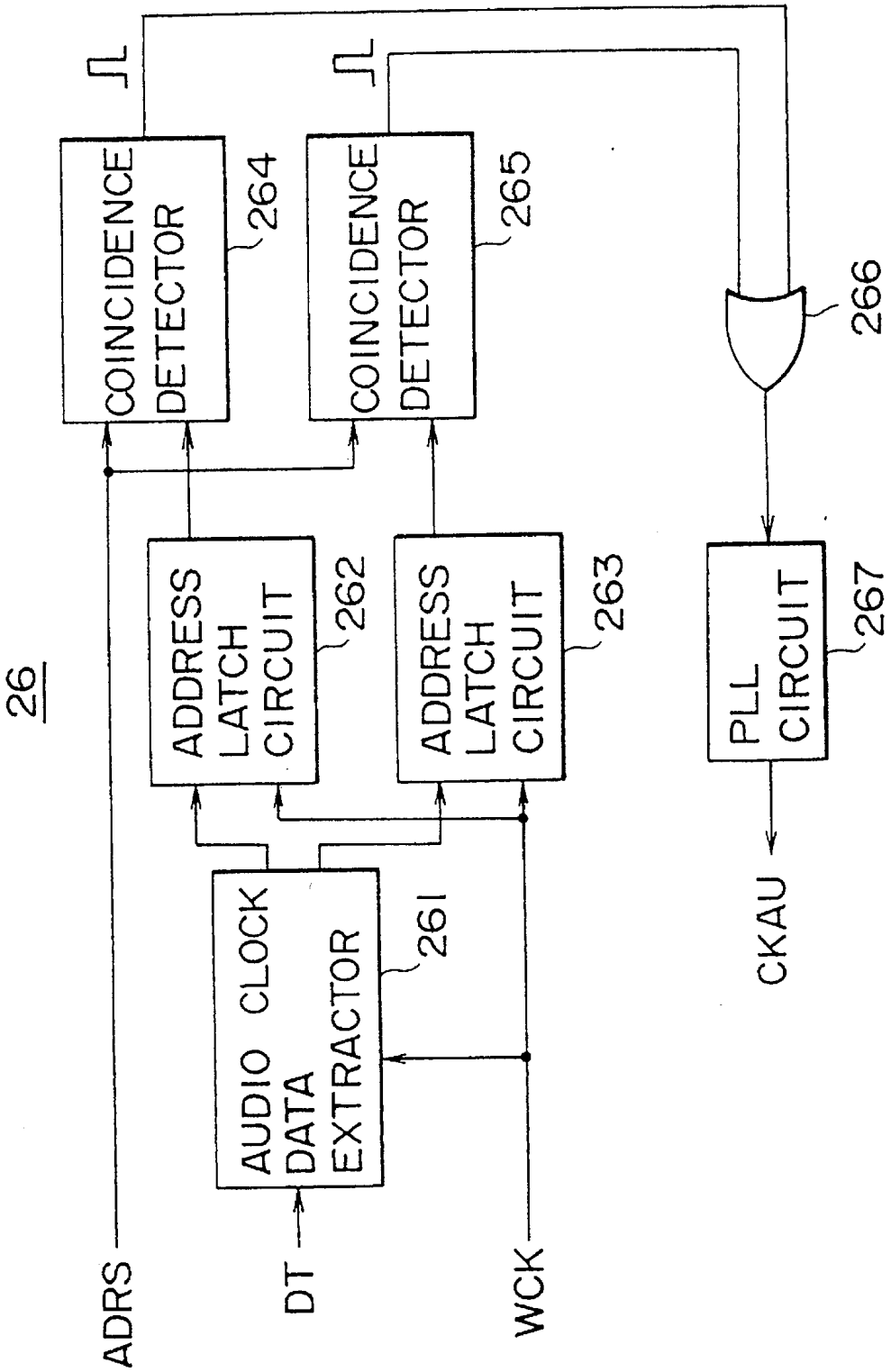

16
SELECTOR
164
ADDRESS LATCH CIRCUIT
163
ADDRESS LATCH CIRCUIT
162
DIFFERENTIATOR
161
13
13
ADRS
CKAU

FIG. 5


26
COINCIDENCE DETECTOR
264
COINCIDENCE DETECTOR
265
266
ADDRESS LATCH CIRCUIT
262
ADDRESS LATCH CIRCUIT
263
PLL CIRCUIT
267
AUDIO CLOCK DATA EXTRACTOR
261
CKAU
ADRS
DT
WCK

METHOD AND APPARATUS FOR SERIAL TRANSMISSION AND/OR RECEPTION OF NONSYNCHRONOUS, MULTIPLEXED SIGNALS

BACKGROUND OF THE INVENTION

The present invention relates to a method and an apparatus for multiplexing, for example, a digital audio signal with a digital video signal by time division and transmitting and/or receiving such multiplexed signals as serial data, and more particularly, to a method and an apparatus capable of transmitting and/or receiving multiplexed signals even in a state where an audio signal is not synchronized with a video signal.

For transmission of a digital video signal, there is known an exemplary system employing a serial digital interface. According to this interface, a digital video signal is transmitted as 1-bit serial data. More specifically, there is proposed in the serial digital interface a technique in which a blanking period of the video signal is rendered vacant due to non-transmission of horizontal and vertical sync signals, and a digital audio signal is transmitted during such blanking period through time-base compression and multiplexing.

In U.S. Pat. No. 5,199,030, there is disclosed a method of multiplexing and transmitting a digital video signal and a digital audio signal.

The serial digital interface mentioned above has the merit that both a digital video signal and a digital audio signal can be transmitted via a single coaxial cable without signal deterioration, whereby the signal connection between various digital video apparatus can be remarkably simplified.

Generally, the sampling clock frequencies for the digital video signal and the digital audio signal are different from each other. For example, the sampling rate in the case of NTSC video signal is 14.3 MHz, whereas the rate for the audio signal is 48 kHz. The transmission clock rate for the audio signal is generally set to be equal to that for the digital video signal. Assuming in the above example that each sample is composed of 10 bits, it follows that the transmission rate is 143 Mbps. The audio data is compressed in its time base and is multiplexed to form data of the above transmission rate.

In this case, for reproducing the digital audio data, it is generally necessary that the sampling clock on the transmission side and that on the reception side are coincident with each other. However, an occurrence of a frequency error is practically unavoidable even by the use of quartz oscillators. For attaining synchronism between the clocks on the transmission and reception sides, it is customary in the prior art to adopt means of synchronizing, on the transmission side, the sampling clock of the audio data with the video signal while using, on the reception side, the vertical sync signal included in the received video signal, and locking the clock frequency of the video signal to the reproduced sync signal in the same manner as on the transmission side, thereby achieving satisfactory reproduction of the audio data.

When a digital audio signal is transmitted via a serial interface while being multiplexed by time division with a digital video signal as described above, the following three requisite relations need to be ensured.

(1) The transmission audio clock is synchronized with the transmitted video signal.

(2) The transmission video signal and the received video signal are synchronized with each other.

(3) The reception audio clock is synchronized with the received video signal. Due to the above requirements, there exists the following implicit precondition.

(4) The transmission audio clock and the reception audio clock are synchronized with each other.

If the conditions (1) to (4) described above fail to be satisfied, there arises some excess or deficiency of the data on the reception side due to the frequency difference between the transmission audio clock and the reception audio clock, whereby the original digital audio signal is not reproduced properly.

Therefore, in the conventional transmission system employing such a digital interface, it is impossible to transmit an audio signal not synchronized with a video signal.

However, in a practical operation, it is not exactly ensured that a desired relationship of synchronism is maintained between the digital video signal and the digital audio signal. For example, though in any broadcasting station a video signal and an audio signal are locked to sync signals of that station, such sync signals of that station may not always be synchronized with the signals of the other station, so that the above problem is raised in using a television signal of the other station.

Although it is possible to attain synchronism with respect to the video signal in this case by locking the same to a sync signal, there still remains a problem that the clock for the audio signal may fail to follow up exactly.

Further in any program employing a VTR, there may be selected, depending on the content of a broadcast, a program play mode where the broadcast is so adjusted as to be completed within a changed time shorter or longer than a normal reproduction time. Supposing now that the time is shortened by 5 percent for example, the audio clock frequency is also shifted to be higher by 5 percent to consequently cause a non-locked state.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method and an apparatus capable of performing serial transmission of multiplexed signals in such a manner that, even in a state where a transmission audio clock is not synchronized with a transmitted video signal as mentioned, a digital audio signal can be properly reproduced without the necessity of any process of correction on the reception side.

According to a first aspect of the present invention, there is provided a method for transmission of multiplexed signals as serial data obtained by multiplexing a first digital sample signal of a continuous signal with a second digital sample signal. The method comprises the steps of: generating an address based on a clock of the second digital sample signal; sampling the generated address by the use of a sampling clock of the continuous signal; and transmitting the multiplexed signals inclusive of the sampled address value inserted therein.

According to a second aspect of the present invention, the above method further comprises the steps of: reproducing, from the received serial data on the reception side, a first clock synchronized with the transmission-side clock of the second digital sample signal; generating address data on the basis of the reproduced clock; generating a second clock for reproduction of the continuous signal from both the generated address data and the address value separated from the received serial data; and reproducing the continuous signal in accordance with the generated second clock. In the above, the word clock of the second digital sample signal is equal

to the word clock of the multiplexed signal. The continuous signal is an audio signal, and the second digital sample signal is a digital video signal, and the sample signal of the audio signal is multiplexed during the blanking period of the digital video signal.

According to a third aspect of the present invention, there is provided an apparatus for transmission of multiplexed signals as serial data obtained by multiplexing a first digital sample signal of a continuous signal with a second digital sample signal. The apparatus comprises: a circuit for generating an address based on a clock of the second digital sample signal; a circuit for sampling the generated address by the use of a sampling clock of the continuous signal; a circuit for inserting the sampled address value into the multiplexed signals; and a circuit for converting the multiplexed signals, where the address value is inserted, into serial data for transmitting the same.

According to a fourth aspect of the present invention, the above apparatus further comprises: a circuit for separating, on a reception side, the received serial data into the first digital sample signal of the continuous signal, the second digital sample signal and the address value; a circuit for reproducing a first clock synchronized with the clock of the second digital sample signal; a circuit for generating address data on the basis of the reproduced clock; a comparator circuit for comparing the generated address data with the address value of the received multiplexed signal; a circuit for generating a second clock for reproduction of the continuous signal on the basis of the output of the comparator circuit; and a circuit for reproducing the continuous signal in accordance with the generated second clock. In the above apparatus, the word clock of the second digital sample signal is equal to the word clock of the multiplexed signal. The continuous signal is an audio signal, and the second digital sample signal is a digital video signal, and the sample signal of the audio signal is multiplexed during the blanking period of the digital video signal.

According to a fifth aspect of the present invention, there is provided an apparatus for transmitting and receiving multiplexed signals as serial data obtained by multiplexing a first digital sample signal of a continuous signal with a second digital sample signal. The apparatus comprises: a circuit for generating a word address based on a word clock of the second digital sample signal; a circuit for sampling the generated word address in accordance with the sampling clock of the continuous signal; a circuit for inserting the sampled word address value into the multiplexed signals; a circuit for converting the multiplexed signals, where the word address value is inserted, into serial data for transmitting the same; a circuit for separating the received serial data into the first digital sample signal of the continuous signal, the second digital sample signal and the word address value; a circuit for reproducing the first word clock synchronized with the word clock of the second digital sample signal; a circuit for generating address data on the basis of the reproduced word clock; a comparator circuit for comparing the generated word address data with the word address value of the received multiplexed signal; a circuit for generating a second word clock for reproduction of the continuous signal on the basis of the output of the comparator circuit; and a circuit for reproducing the continuous signal in accordance with the generated second word clock. In this apparatus, the word clock of the second digital sample signal is equal to the word clock of the multiplexed signal. The continuous signal is an audio signal, and the second digital sample signal is a digital video signal, and the sample audio signal is multiplexed during the blanking period of the digital video signal.

In the present invention of the constitution mentioned above, the word clock for the second digital sample signal is reproduced in a synchronized state on the transmission and reception sides. And the address of the second digital sample signal is generated on the basis of such word clock.

The clock data relative to the multiplex continuous signal is transmitted in a state where the address value obtained by sampling the address of the second sample signal in accordance with the audio clock is included in the multiplexed signals. Consequently the audio clock, which represents the time point of sampling the address in accordance with the audio clock, is reproduced from both the address data reproduced on the reception side and the data of the transmitted address value. Therefore, even if the multiplex continuous signal is not in synchronism with the second sample signal, the clock for the continuous signal is properly reproducible on the reception side so that the continuous signal can be exactly reproduced.

The above and other features and advantages of the present invention will become apparent from the following description which will be given with reference to the illustrative accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a preferred embodiment representing an apparatus of the present invention for transmission and reception of multiplexed signals;

FIGS. **2**A to **2**D are timing charts of signals for explaining principal circuits in the present invention;

FIG. **3** illustrates an exemplary format of signals multiplexed in the present invention;

FIG. **4** is a block diagram of principal circuits on the transmission side of the embodiment shown in FIG. **1**; and

FIG. **5** is a block diagram of principal circuits on the reception side of the embodiment shown in FIG. **1**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter a preferred embodiment of the method and the apparatus of the present invention will be described with reference to an exemplary case of employing a serial digital interface which transmits serial data of a multiplexed signal obtained by multiplexing a digital audio signal with a digital high-definition video signal.

FIG. **1** is a block diagram showing exemplary constructions of transmission and reception sides in the embodiment. In this diagram, a high-definition video signal of 1125/60 system (1 field=60 Hz, 1125 lines per frame=2 fields) is composed of a luminance signal Y and color difference signals Pb, Pr each converted into a 10-bit digital video signal in accordance with sampling clock pulses of 74.25 MHz and 37.125 MHz respectively.

In this case, as shown also in FIG. **2**B, a word address ADRS of the digital video signal is generated in a word address generator **1** with reference to a horizontal sync signal of the high-definition video signal shown in FIG. **2**A. More specifically, in the word address ADRS of the digital video signal, one horizontal interval is determined as its repetition period and, as shown in FIG. **2**B for example, the top address of the horizontal sync signal is 0, and the last address of the effective video data is 4399.

The digital video signal composed of respective words of the luminance signal Y and the color difference signals Pb, Pr is supplied to a video multiplexer **11** and is multiplexed

in the order of Pb, Y, Pr, Y . . . during the period of the video effective data shown in FIG. **2B**, to be thereby formed into digital video data. Although not shown, the luminance signal and the color difference signals are distributed on the basis of the word address data ADRS.

As obvious from FIG. **2B**, the horizontal sync signal of the video signal is not included in the transmitted data, and the video signal is the data except for the blanking period. More specifically, the transmitted video data is the effective data of a total of 3840 words including the luminance signal Y of 1920 words (1 word=10 bits) per horizontal interval and the color difference signals Pr and Pb each of 960 words per horizontal interval. The blanking period corresponds to 560 words.

Meanwhile the audio signal is converted into a digital audio signal AU composed of 24-bit words in accordance with an audio clock CKAU of, e.g., 48 kHz. The digital audio signal AU is written in an audio memory **12** in accordance with the audio clock CKAU.

The audio data AU is read out from the audio memory **12** during the blanking period of the high-definition video signal in accordance with the word clock CKV of the video signal, and then the audio data is time-division multiplexed in an audio multiplexer **13** with the-video data obtained from the video multiplexer **11**. In this stage of the operation, the audio data is compressed by time division on the basis of the frequency difference between the write clock and the read clock.

This embodiment is equipped with an audio clock data generator **16**, to which the word address ADRS of the digital video data is inputted to be sampled in accordance with the audio clock CKAU.

In this case, approximately 1.5 words of the audio data are included in each horizontal interval since the sampling clock frequency of the audio signal is 48 kHz and one horizontal interval is approximately 30 μsec.

In the audio clock data generator **16**, the word address ADRS of the video data is latched in accordance with the sampling clock CKAU of the audio data AU. And the value of the word address ADRS of the video data at the sampling time point of the latched audio word is supplied to the audio multiplexer **13** and then is inserted as data in the blanking period of the multiplexed data shown in FIG. **2B**.

FIG. **3** shows a format of the data to be multiplexed by time division as ancillary data (auxiliary data) during the blanking period.

In FIG. **3**, the first word "ADF" denotes an ancillary data flag which is used for identifying the data inserted in the blanking period, thereby indicating a start of the ancillary data. A next word "DID" denotes identification data signifying the kind of the ancillary data to make a discrimination as to whether the relevant ancillary data is audio data or some other data. A subsequent word "DBN" denotes a data block number which is serial in a packet during succession of audio data. And a jump of the number indicates a joint of the audio signal.

The following "DC" (data count) denotes information signifying the number of words of the ancillary data inserted in one packet. And audio data is inserted posterior to the data DC. In this example, the audio data is followed by the aforementioned audio clock data, i.e., the address data of the video data at the time point of the sample word of each digital audio signal. The last "CHK SUM" denotes a check sum covering from the data DID to the audio clock data and is used for error detection.

Thus the audio signal is multiplexed with the video signal as described, and further the address data of the video word is multiplexed as the clock data for the audio data to form multiplexed data, which is then supplied from the audio multiplexer **13** to a TRS multiplexer **14**. In this multiplexer **14**, there is multiplexed a timing reference signal (TRS) indicative of synchronization timing or the like anterior to the ancillary data in the blanking period.

The output of the TRS multiplexer **14** is parallel data where each word is composed of 10 bits. The word clock for such parallel data is the one for high-definition video data.

This parallel data is supplied to a parallel-to-serial converter **15**, where the 10-bit parallel data of 148.5 MHz is converted into 1-bit serial data of 1.485 GHz. The data thus converted is outputted to a coaxial cable **30** and so forth, through which the multiplexed data is transmitted from the transmission side **10** to the reception side **20**.

On the reception side **20**, a sync reproducer **22** including a data decision circuit **21** and a PLL circuit reproduces the serial data of 1.485 GHz and the bit clock from the received signal. A TRS detector/serial-to-parallel converter **23** in the next stage detects the timing reference signal (TRS) to reproduce the word sync signal and then converts the 1-bit serial data of 1.485 GHz into parallel data DT of 148.5 MHz where each word is composed of 10 bits.

In the converter **23**, the word address ADRS of the video data is reproduced from the word sync clock obtained from the sync reproducer **22**. And the parallel data DT is supplied from the converter **23** to a video reproducer **24**, where the luminance signal Y and the color difference signals Pb, Pr are reproduced on the basis of the word address ADRS.

The parallel data DT is supplied also to an audio memory **25**, where the audio data in the blanking period is written and stored. Meanwhile the parallel data DT is further supplied to an audio clock reproducer **26**, which then reproduces the word address corresponding to the timing of the audio clock in the blanking period.

To the audio clock reproducer **26**, there is supplied the word address ADRS of the video data thus reproduced, so that the word address relative to the reproduced audio clock and the word address ADRS of the reproduced video data are compared with each other, and a clock pulse is obtained at the time of coincidence thereof. Then the clock pulse is supplied to, e.g., the PLL circuit to thereby reproduce the audio clock CKAU equal to the stable transmission-side clock. Subsequently the clock CKAU is supplied to the audio memory **25**, from which the audio data is read out. Thus, the audio data can be read out without any excess or deficiency on the reception side to be thereby reproduced properly.

FIG. **4** is a block diagram of the audio clock data generator **16** employed on the transmission side **10**.

As shown in this diagram, the audio clock CKAU from the transmission side is supplied to a differentiator **161**, where a differential pulse is obtained at the sampling time point corresponding to, e.g., the fall or trailing edge. The differential pulse thus obtained is then supplied to address latch circuits **162** and **163**.

Meanwhile the word address signal ADRS of the digital video data is supplied to the address latch circuit **162**. The address latch circuits **162** and **163** are in cascade connection to serve as a shift register where an address value is transferred to the latter-stage latch circuit in response to each clock pulse.

In the construction described above, the word address ADRS of the digital video data at the timing of the audio clock CKAU is sequentially latched by the address latch

circuits **162** and **163**, and then is supplied via a selector **164** to the audio multiplexer **13**, where the word address ADRS is inserted and multiplexed in the blanking period as mentioned.

FIG. **5** is a block diagram showing an exemplary construction of the audio clock data reproducer **26** employed on the reception side **20**.

The parallel data DT outputted from the converter **23** is supplied to an audio clock data extractor **261**, to which a word clock WCK is also supplied from the converter **23**. Consequently the word address data of the video data relative to the audio clock inserted in the blanking period is extracted and then is held by address latch circuits **262** and **263**.

The address value of the video signal at the time point of each audio clock held by the address latch circuits **262** and **263** is supplied to coincidence detectors **264** and **265**, which are also supplied with the word address signal ADRS of the reception-side digital video data. And upon coincidence between the word address data obtained from the latch circuits **262**, **263** and the input word address data ADRS, coincidence detection pulses are generated from the coincidence detectors **263** and **265**. Such pulses are supplied via an OR gate **266** to a PLL circuit **267** so that the audio clock CKAU is reproduced.

The provision of such a PLL circuit **267** is based on the following reason. Since the audio clock data is equal to the data obtained by sampling the original transmission-side audio clock CKAU in accordance with the video clock, the audio clock data includes some jitters of the video clock period (6.734 nsec). Consequently the clock pulse obtained via the OR gate **266** includes such a jitter component. Therefore the PLL circuit **267** is employed to acquire a jitterless clock CKAU.

In this embodiment, as described above, a jitterless audio clock is generated through the PLL circuit **267** on the reception side so as to eliminate the jitter component caused by sampling the audio clock in accordance with the video clock. However, the jitter is permissible to some extent depending on the purpose of use. In such a case, therefore, the output of the OR gate **266** may be used directly as the audio clock.

Thus, in this embodiment where the reception-side audio clock is generated by utilizing the address data of the video data relative to the audio clock multiplexed with the transmission data, there occurs neither excess nor deficiency of the data in the reception-side audio memory even if the audio clock on the transmission side is not in synchronism with the video signal, so that the audio signal can be reproduced properly without any disadvantage.

It is to be noted in the above embodiment that the audio signal is not limited to one channel alone, and signals of two or more channels may be transmitted within a range of the blanking period during which multiplexing is performed.

Also in the above embodiment where the audio clock frequency is set to 48 kHz as an example, it is a matter of course that any other adequate frequency is applicable as well. Meanwhile the video signal described as an example is the one based on a 1125/60 high-definition television system. However, it is obvious that the present invention is further applicable to a component video signal of a 525/60 or 625/50 system, or to a video signal of any other television system such as NTSC or PAL.

Although the description has been given with regard to an exemplary case of multiplexing a video signal and an audio signal, the present invention is applicable to any multiplexed signals composed of a continuous signal and another signal.

The embodiment mentioned above represents an example where the continuous signal is an audio signal while the other sample signal is a digital video signal, and the audio signal is multiplexed by utilizing the blanking period of the video signal. Therefore the word clock used for such multiplexing is equal to the word clock of the video data. However, in case the other sample signal is a continuous signal, its time base is compressed and a vacant period is prepared for multiplexing the continuous signal.

In this case, the word clock of the other sample signal and the word clock used for multiplexing are different in frequency from each other. But if the word clock of the other sample signal is synchronously locked on both the transmission side and the reception side, the reception-side clock of the continuous signal can be reproduced in the same manner as mentioned by inclusively transmitting, together with the multiplexed signals, the address value obtained by sampling the address data, which is based on the word clock of the other sample signal, in accordance with the clock of the continuous signal. It is a matter of course that, in this case also, the address value obtained by sampling the address data, which is based on the word clock for multiplexing, in accordance with the clock of the continuous signal, may be included in the multiplexed signals so as to be transmitted therewith.

As described hereinabove, in the present invention for transmission of multiplexed data formed by time-division multiplexing a continuous signal with another signal, the word address data of signal reproducible on the reception side is sampled in accordance with the clock signal of the multiplex continuous signal, and the address data thus sampled is inserted into the multiplexed signals to be thereby transmitted together. Consequently, even if the continuous signal is not in synchronism with another signal on the transmission side, the clock of the continuous signal is accurately reproducible from the transmitted address data, whereby the continuous signal can be properly reproduced on the reception side.

What is claimed is:

1. A method for transmission of multiplexed signals as serial data obtained by multiplexing a first digital sample signal of a continuous signal with a second digital sample signal, said method comprising the steps of:

generating an address based on a clock signal of said second digital sample signal;

sampling the generated address by the use of a sampling clock signal of said continuous signal to produce a sampled address value; and

transmitting the multiplexed signals inclusive of the sampled address value inserted therein.

2. The method according to claim **1**, further comprising the steps of:

receiving serial data on a reception side and reproducing, from the received serial data, a first clock signal synchronized with a transmission-side clock signal of said second digital sample signal;

generating address data on the basis of the reproduced first clock signal;

generating a second clock signal for reproduction of said continuous signal from both the generated address data and an address value separated from the received serial data; and

reproducing said continuous signal in accordance with the generated second clock signal.

3. The method according to claim **1**, wherein a word clock signal of said second digital sample signal is equal to a word clock signal of the multiplexed signals.

4. The method according to claim 1, wherein said continuous signal is an audio signal, and said second digital sample signal is a digital video signal, and the sample signal of said audio signal is multiplexed during a blanking period of said digital video signal.

5. An apparatus for transmission of multiplexed signals as serial data obtained by multiplexing a first digital sample signal of a continuous signal with a second digital sample signal, said apparatus comprising:

a circuit for generating an address based on a clock signal of said second digital sample signal;

a circuit for sampling the generated address by the use of a sampling clock signal of said continuous signal to produce a sampled address value;

a circuit for inserting the sampled address value into said multiplexed signals; and

a circuit for converting said multiplexed signals, where the address value is inserted, into serial data for transmitting the same.

6. The apparatus according to claim 5, further comprising:

a circuit for receiving serial data and separating, on a reception side, the received serial data into said first digital sample signal of the continuous signal, said second digital sample signal and said address value;

a circuit for reproducing a first clock signal synchronized with the clock signal of said second digital sample signal;

a circuit for generating address data on the basis of the reproduced first clock signal;

a comparator circuit for comparing the generated address data with the address value of the received received serial data;

a circuit for generating a second clock signal for reproduction of said continuous signal on the basis of an output of said comparator circuit; and

a circuit for reproducing said continuous signal in accordance with the generated second clock signal.

7. The apparatus according to claim 5, wherein a word clock signal of said second digital sample signal is equal to a word clock signal of said multiplexed signal.

8. The apparatus according to claim 5, wherein said continuous signal is an audio signal, and said second digital sample signal is a digital video signal, and the sample signal of said audio signal is multiplexed during the blanking period of said digital video signal.

9. An apparatus for transmitting and receiving multiplexed signals as serial data obtained by multiplexing a first digital sample signal of a continuous signal with a second digital sample signal, said apparatus comprising:

a circuit for generating a word address based on a word clock signal of said second digital sample signal;

a circuit for sampling the generated word address in accordance with the sampling clock signal of said continuous signal to produce a word address value;

a circuit for inserting the word address value into said multiplexed signals;

a circuit for converting said multiplexed signals, where the word address value is inserted, into serial data for transmitting the same;

a circuit for receiving the serial data and separating the received serial data into said first digital sample signal of the continuous signal, said second digital sample signal and said word address value;

a circuit for reproducing a first word clock signal synchronized with a word clock signal of said second digital sample signal;

a circuit for generating word address data on the basis of the reproduced first word clock signal;

a comparator circuit for comparing the generated word address data with the word address value of the received serial data;

a circuit for generating a second word clock signal for reproduction of said continuous signal on the basis of the output of said comparator circuit; and

a circuit for reproducing said continuous signal in accordance with the generated second word clock signal.

10. The apparatus according to claim 9, wherein the word clock signal of said second digital sample signal is equal to the word clock signal of the multiplexed signal.

11. The apparatus according to claim 9, wherein said continuous signal is an audio signal, and said second digital sample signal is a digital video signal, and the sample signal of said audio signal is multiplexed during the blanking period of said digital video signal.

* * * * *

EXHIBIT C

US005999213A

United States Patent [19]

Tsushima et al.

[11] **Patent Number: 5,999,213**

[45] **Date of Patent: Dec. 7, 1999**

[54] **METHOD OF AND APPARATUS FOR SETTING UP ELECTRONIC DEVICE**

[75] Inventors: **Katsuhiko Tsushima**; **Kazuyoshi Miyamoto**; **Taku Kihara**; **Yoshio Chiba**, all of Kanagawa, Japan

[73] Assignee: **Sony Corporation**, Tokyo, Japan

[21] Appl. No.: **08/659,686**

[22] Filed: **Jun. 6, 1996**

[30] **Foreign Application Priority Data**

Jun. 8, 1995 [JP] Japan 7-142222

[51] **Int. Cl.**[6] **H04N 17/00**; H04N 17/02

[52] **U.S. Cl.** **348/180**; 348/181; 348/211; 348/212

[58] **Field of Search** 348/180, 181, 348/187, 223, 254, 722, 723, 211, 212, 213, 214; H04N 17/00, 17/02

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,949,286	8/1990	Ohba	348/580
5,036,251	7/1991	Lee	348/180
5,051,827	9/1991	Fairhurst	358/141
5,227,881	7/1993	Wess et al.	348/734
5,291,276	3/1994	Matsumoto et al.	348/180
5,298,993	3/1994	Edgar et al.	348/10
5,335,013	8/1994	Faber	348/254
5,384,768	1/1995	Fujii	370/14
5,483,259	1/1996	Sachs	348/189
5,647,019	7/1997	Iino et al.	348/442
5,675,358	10/1997	Bullock et al.	348/211
5,745,161	4/1998	Ito	346/211

FOREIGN PATENT DOCUMENTS

0 656 731 6/1995 European Pat. Off. .

OTHER PUBLICATIONS

Patent Abstracts of Japan vol. 017, No. 581 (P–1631), Oct. 21, 1993 of JP 05 165943 A (Fuji Xerox Co Ltd), Jul. 2, 1993.

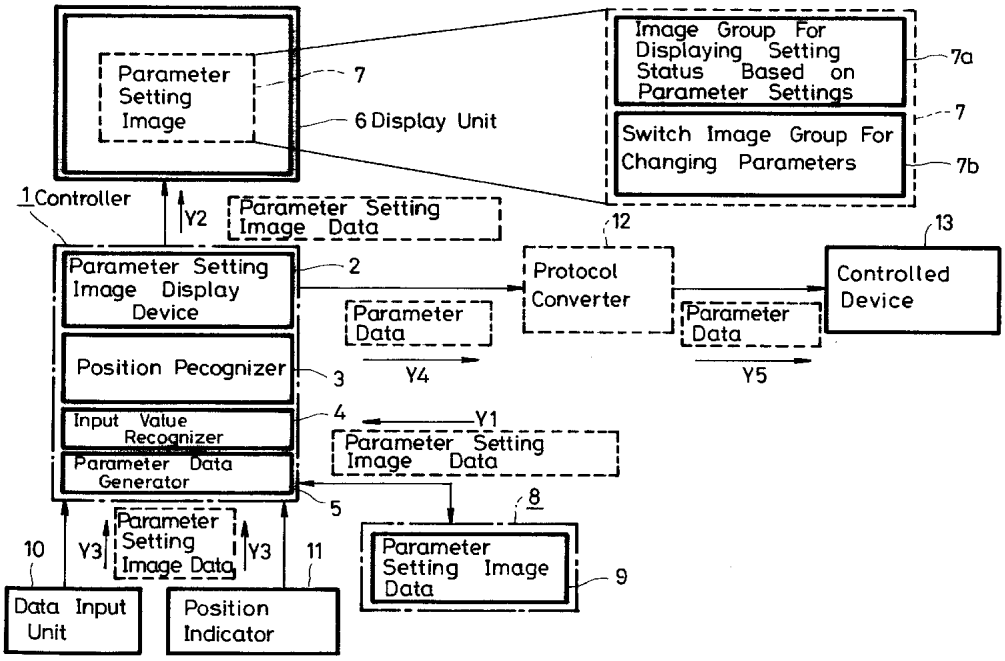
Patent Abstracts of Japan vol. 018, No. 029 (E–1492), Jan. 17, 1994 of JP 05 260405 A (Sony Corp), Oct. 8, 1993.

Primary Examiner—Nathan Flynn
Assistant Examiner—Vivek Srivastava
Attorney, Agent, or Firm—Frommer Lawrence & Haug, LLP.; William S. Frommer

[57] **ABSTRACT**

An apparatus for setting up an electronic device has a memory for storing parameter setting image data for establishing one or more parameters with respect to a controlled device, the parameter setting image including parameter changing switch image data and setting state display image data, a display unit for displaying a parameter setting image based on the parameter setting image data read from the memory, an input unit for entering input information indicating changes in display states of a parameter changing switch image data and a setting state display image which are displayed by the display unit and a parameter to be established, and a controller for changing the display states of the parameter changing switch image data an the setting state display image which are displayed by the display unit and the parameter to be established, based on the input information entered by the input unit, and transmitting changed parameter data or a change in the parameter to the controlled device.

27 Claims, 84 Drawing Sheets



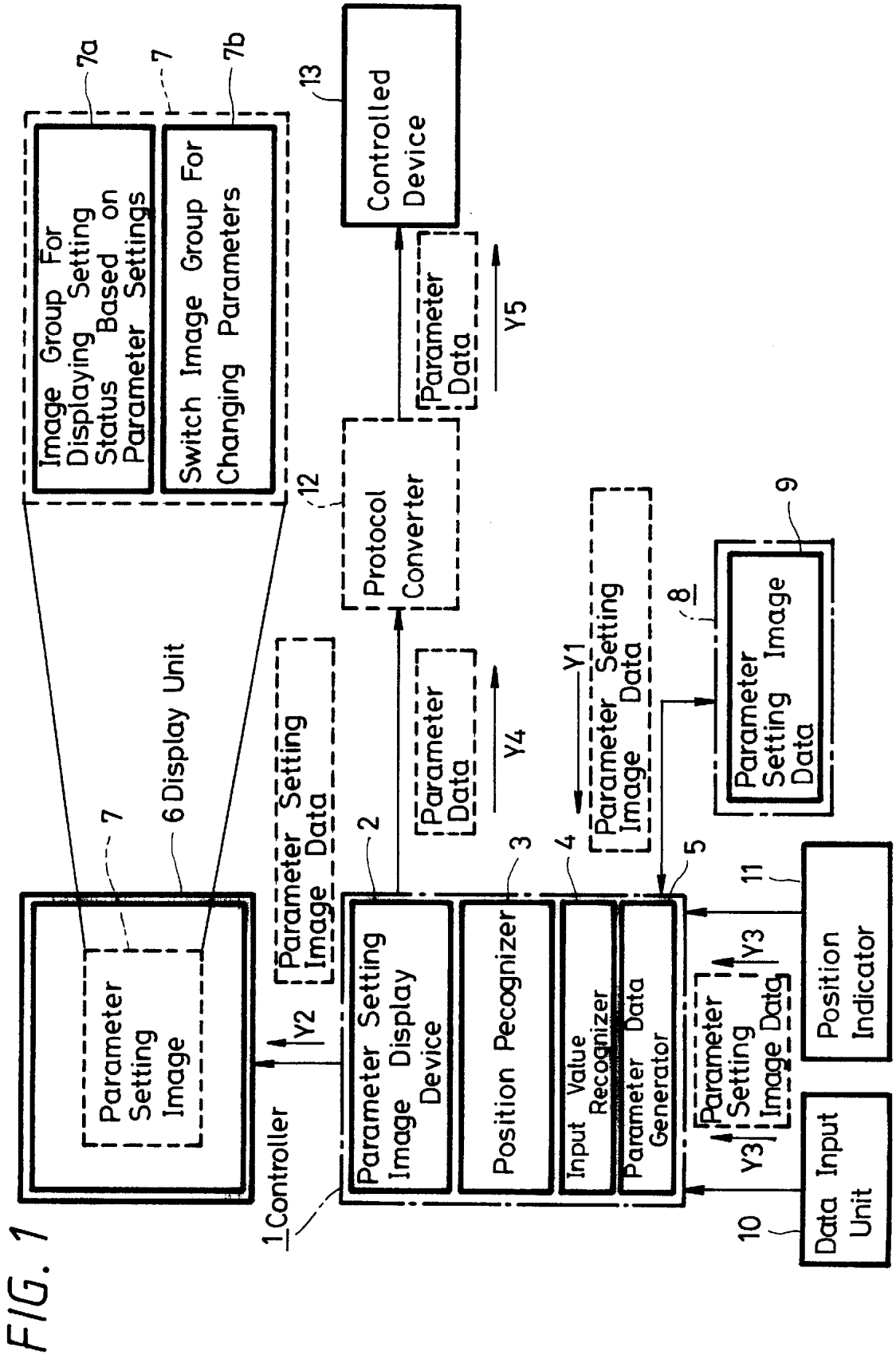

1 Controller
2
3
4
5
6 Display Unit
7
7a
7b
8
9
10
11
12
13
Parameter Setting Image
Parameter Setting Image Data
Parameter Setting Image Display Device
Position Recognizer
Input Value Recognizer
Parameter Data Generator
Parameter Setting Image Data
Parameter Data
Protocol Converter
Controlled Device
Image Group For Displaying Setting Status Based on Parameter Settings
Switch Image Group For Changing Parameters
Parameter Setting Image Data
Parameter Data
Parameter Setting Image Data
Position Indicator
Data Input Unit
Y1
Y2
Y3
Y4
Y5

FIG. 1

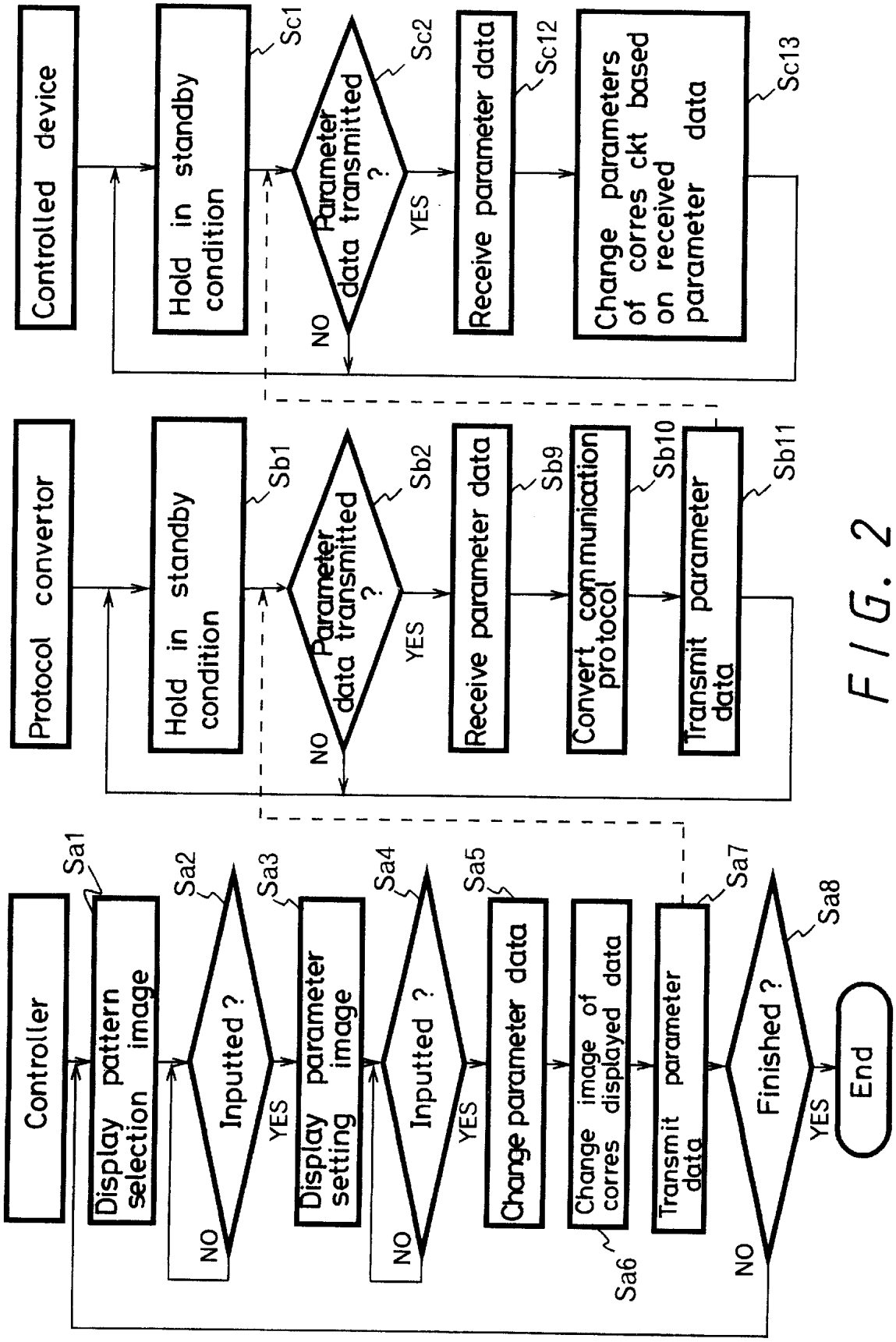

Controlled device
Hold in standby condition
Sc1
Parameter data transmitted ?
Sc2
NO
YES
Receive parameter data
Sc12
Change parameters of corres ckt based on received parameter data
Sc13
Protocol convertor
Hold in standby condition
Sb1
Parameter data transmitted ?
Sb2
NO
YES
Receive parameter data
Sb9
Convert communication protocol
Sb10
Transmit parameter data
Sb11
Controller
Display pattern selection image
Sa1
Inputted ?
Sa2
NO
YES
Display parameter setting image
Sa3
Inputted ?
Sa4
NO
YES
Change parameter data
Sa5
Change image of corres displayed data
Sa6
Transmit parameter data
Sa7
Finished ?
Sa8
NO
YES
End

FIG. 2

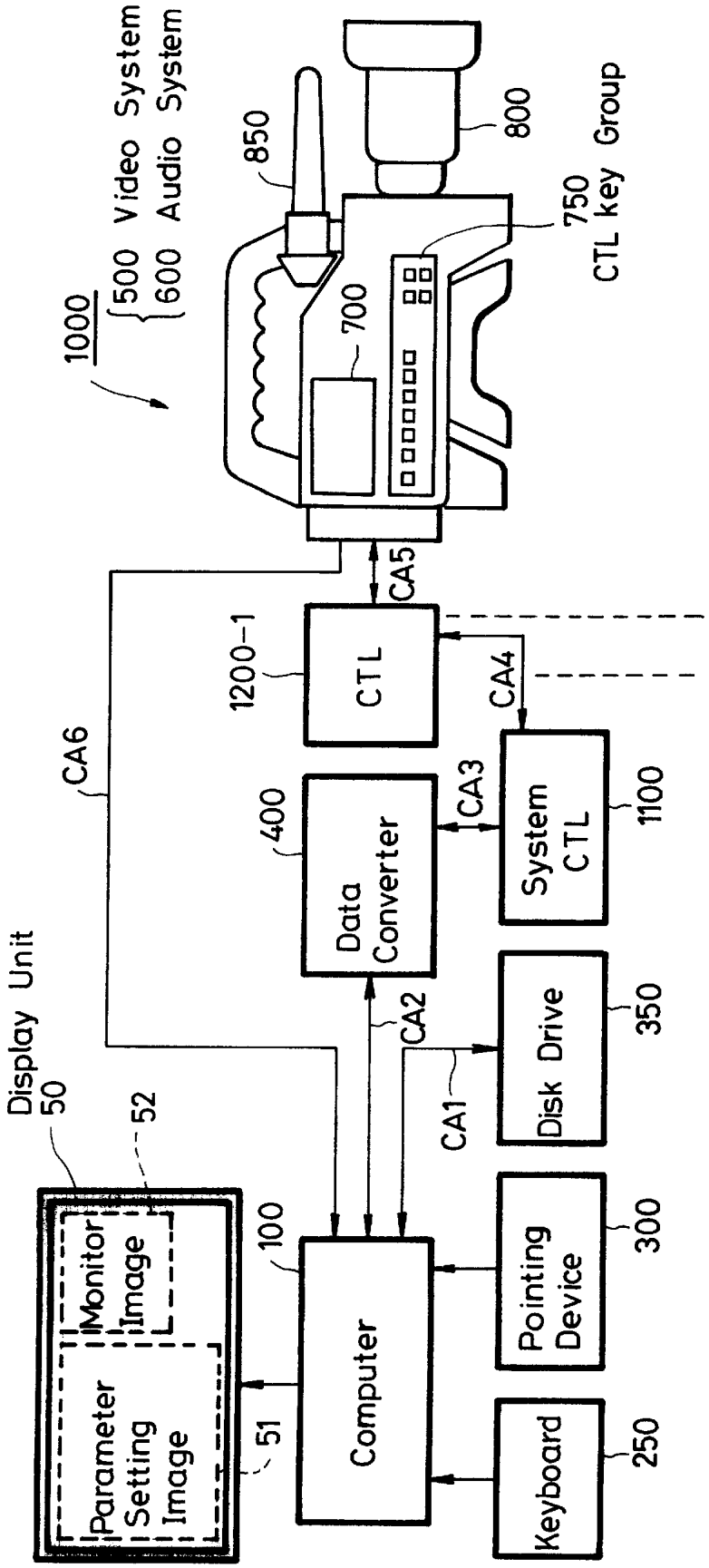

1000
500 Video System
600 Audio System
850
800
750
CTL key Group
700
CA5
1200-1
CTL
CA4
CA6
400
Data Converter
CA3
System CTL
1100
CA2
CA1
Disk Drive
350
Display Unit
50
52
Monitor Image
Parameter Setting Image
100
Computer
51
Pointing Device
300
Keyboard
250

FIG. 3

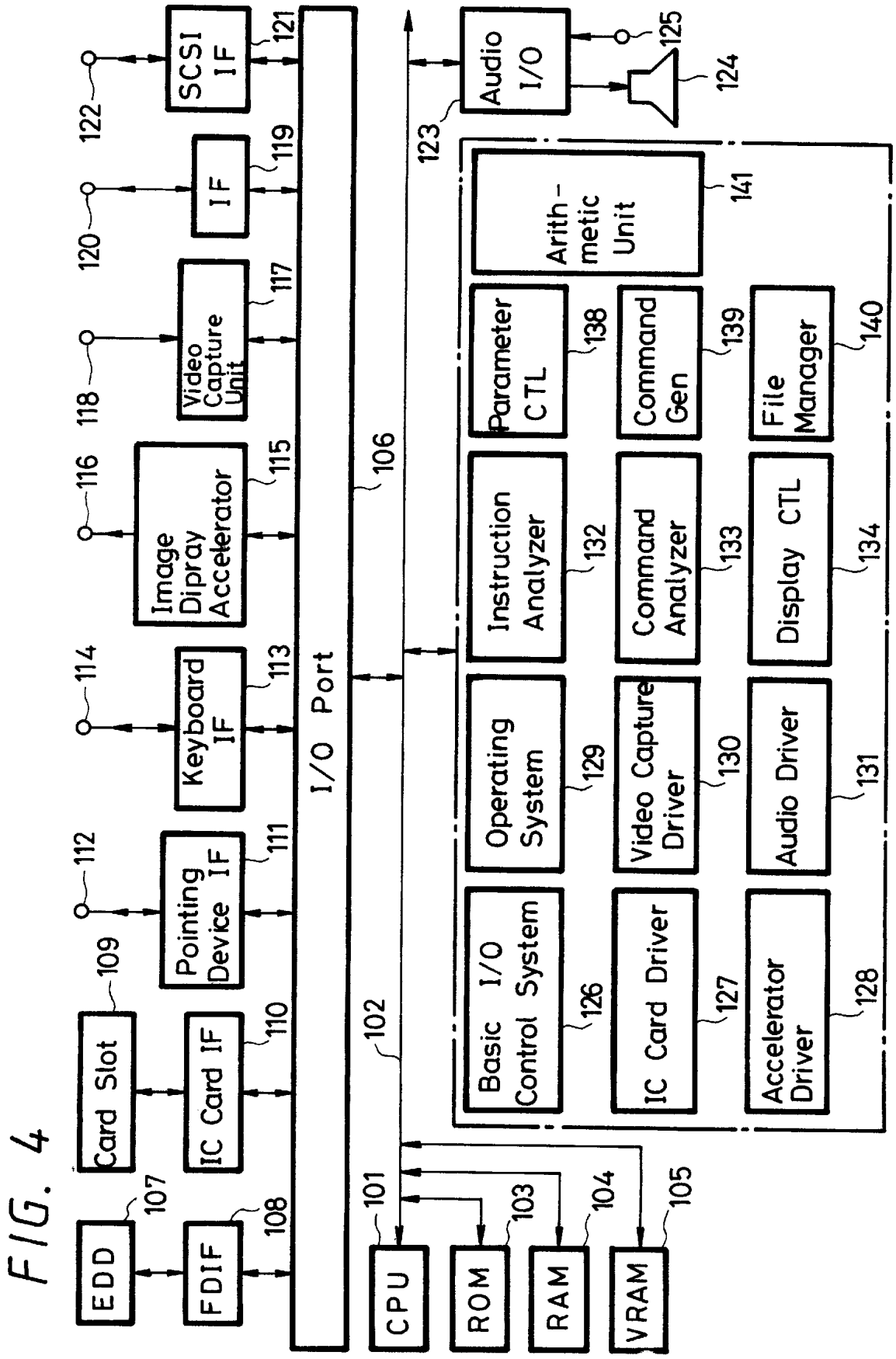

EDD
FDIF
Card Slot
IC Card IF
Pointing Device IF
Keyboard IF
Image Dipray Accelerator
Video Capture Unit
IF
SCSI IF
Audio I/O
I/O Port
CPU
ROM
RAM
VRAM
Basic I/O Control System
IC Card Driver
Accelerator Driver
Operating System
Video Capture Driver
Audio Driver
Instruction Analyzer
Command Analyzer
Display CTL
Parameter CTL
Command Gen
File Manager
Arith-metic Unit
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
138
139
140
141

FIG. 4

FIG. 5

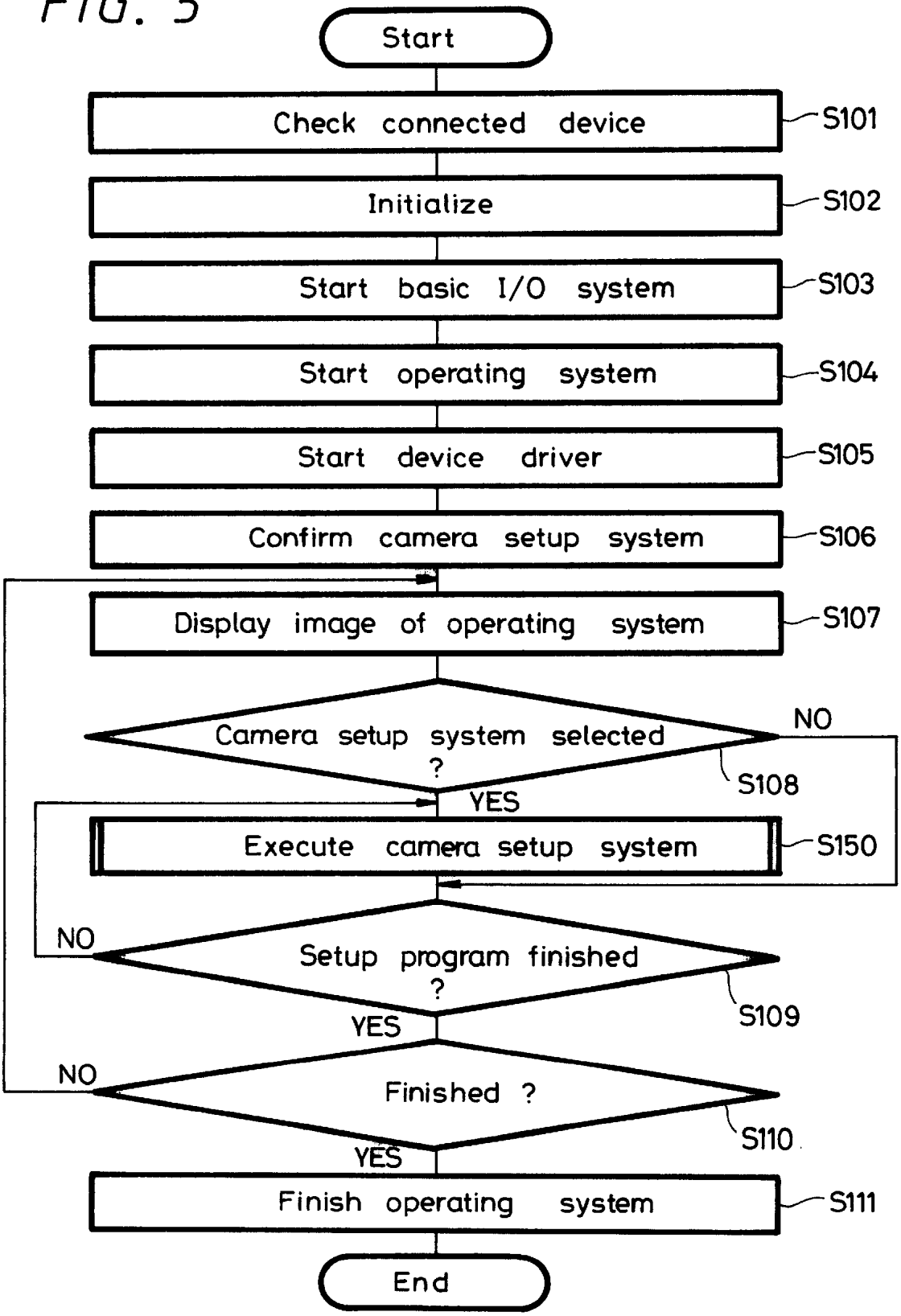

Start
Check connected device
S101
Initialize
S102
Start basic I/O system
S103
Start operating system
S104
Start device driver
S105
Confirm camera setup system
S106
Display image of operating system
S107
Camera setup system selected ?
NO
S108
YES
Execute camera setup system
S150
NO
Setup program finished ?
S109
YES
NO
Finished ?
S110
YES
Finish operating system
S111
End

FIG. 6A

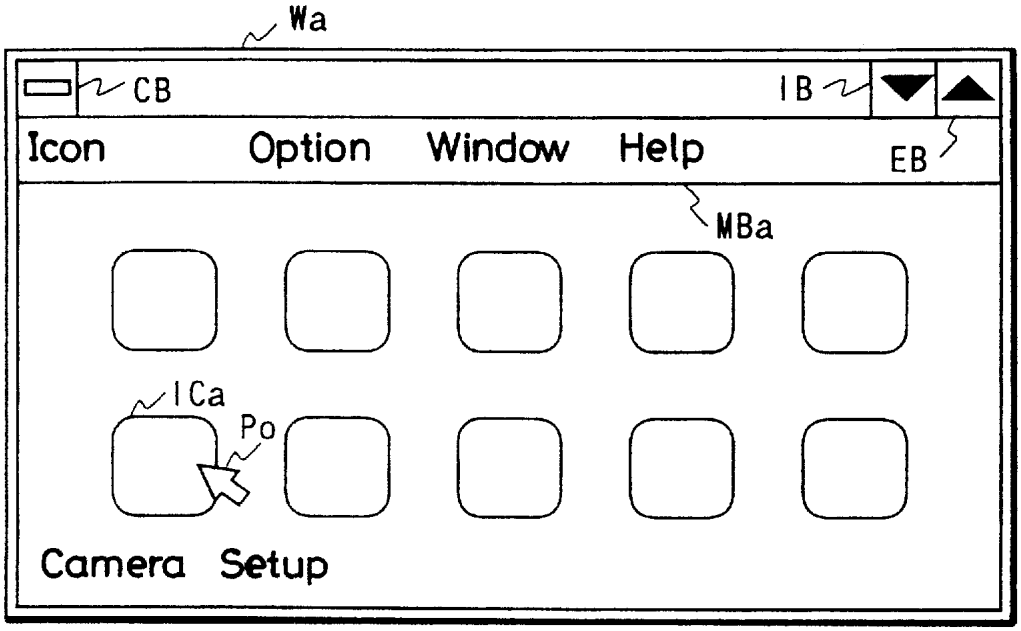

Wa
CB
IB
Icon
Option
Window
Help
EB
MBa
ICa
Po
Camera Setup

FIG. 6B

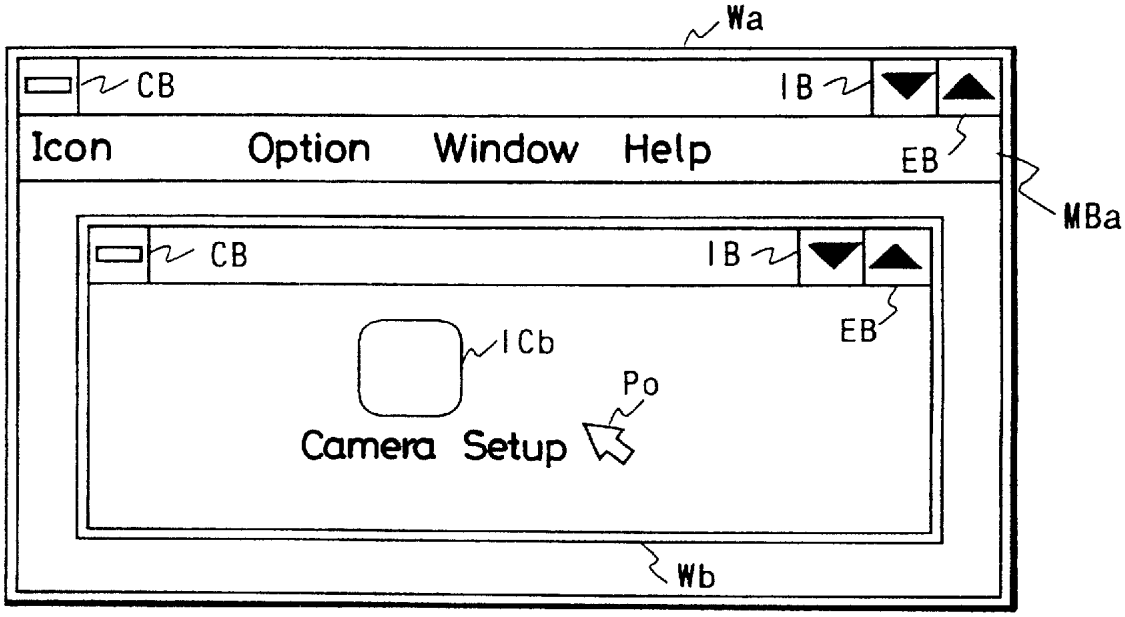

Wa
CB
IB
Icon
Option
Window
Help
EB
MBa
CB
IB
EB
ICb
Po
Camera Setup
Wb

FIG. 7

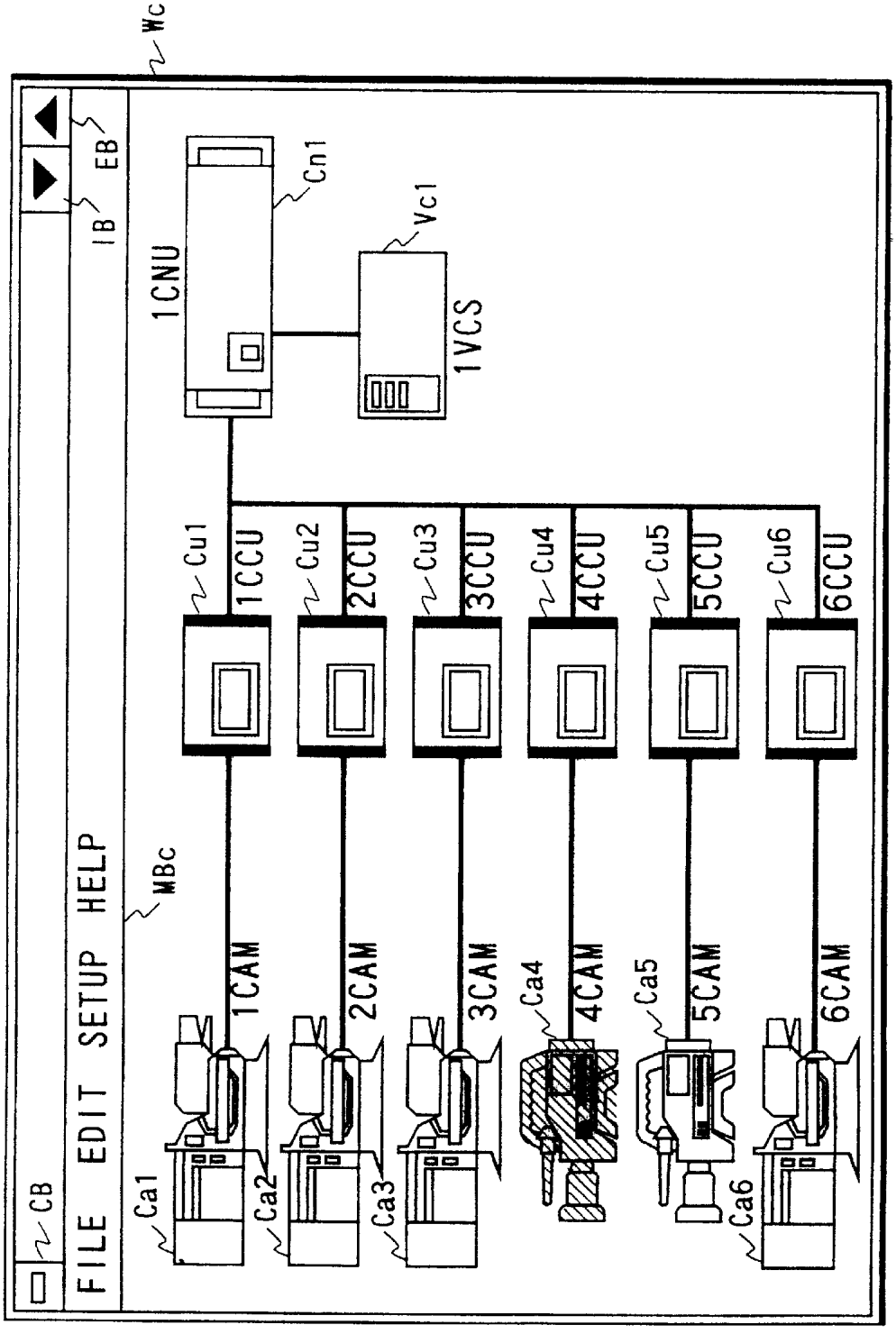
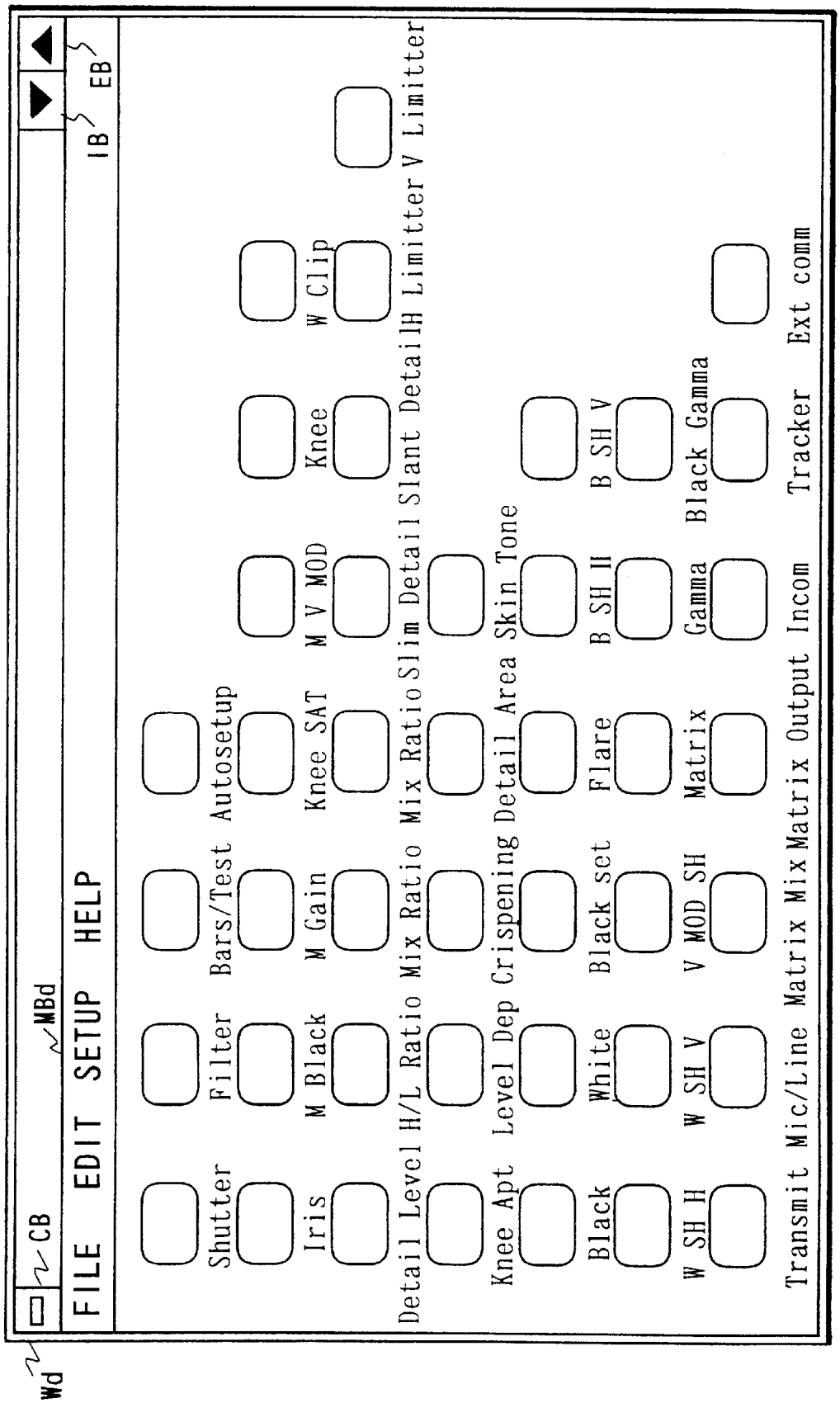

Wc
CB
FILE EDIT SETUP HELP
IB
EB
MBc
1CNU
Cn1
Vc1
1VCS
Cu1
1CCU
Cu2
2CCU
Cu3
3CCU
Cu4
4CCU
Cu5
5CCU
Cu6
6CCU
1CAM
2CAM
3CAM
4CAM
5CAM
6CAM
Ca1
Ca2
Ca3
Ca4
Ca5
Ca6

FIG. 8


Wd
CB
MBd
IB
EB
FILE EDIT SETUP HELP
Shutter
Filter
Bars/Test
Autosetup
Iris
M Black
M Gain
Knee SAT
M V MOD
Knee
W Clip
Detail Level H/L Ratio Mix Ratio Mix Ratio Slim Detail Slant Detail H Limitter V Limitter
Knee Apt
Level Dep
Crispening
Detail Area
Skin Tone
Black
White
Black set
Flare
B SH H
B SH V
W SH H
W SH V
V MOD SH
Matrix
Gamma
Black Gamma
Transmit Mic/Line Matrix Mix Matrix Output Incom
Tracker
Ext comm

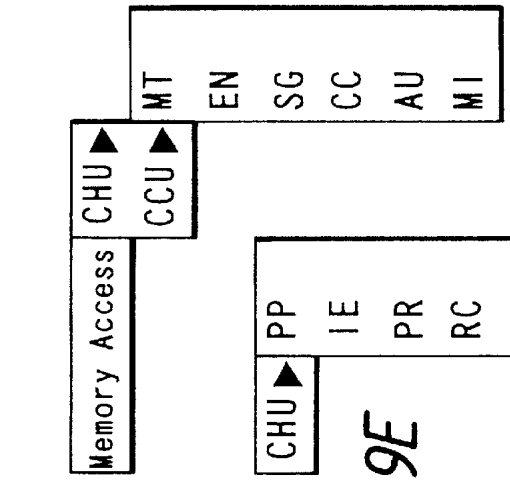


FIG. 9D

FIG. 9E

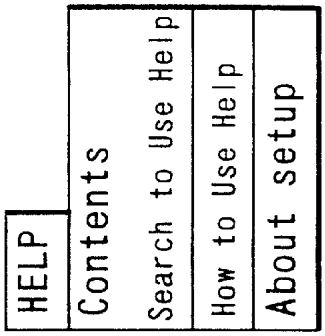


FIG. 9F

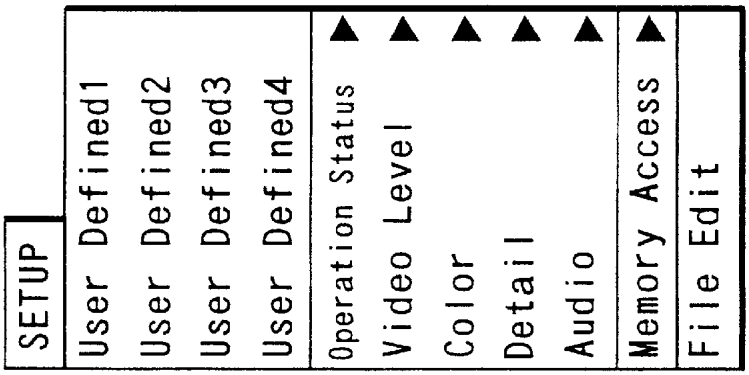


FIG. 9C

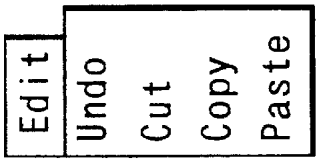


FIG. 9B

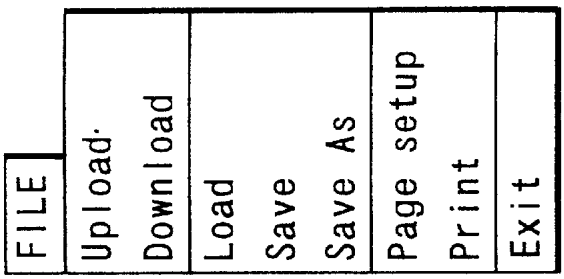


FIG. 9A

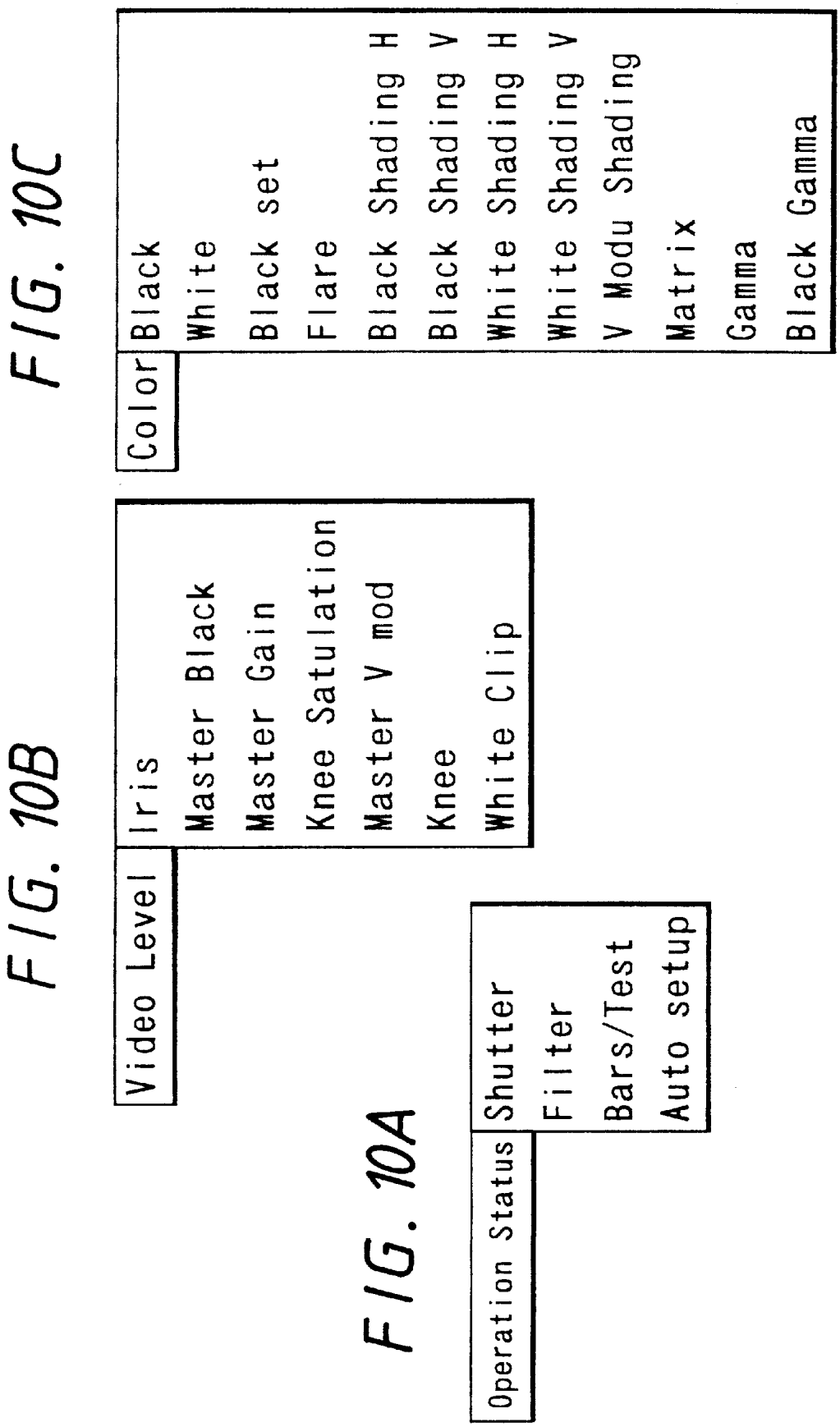


FIG. 10C

FIG. 10B

FIG. 10A

FIG. 11A

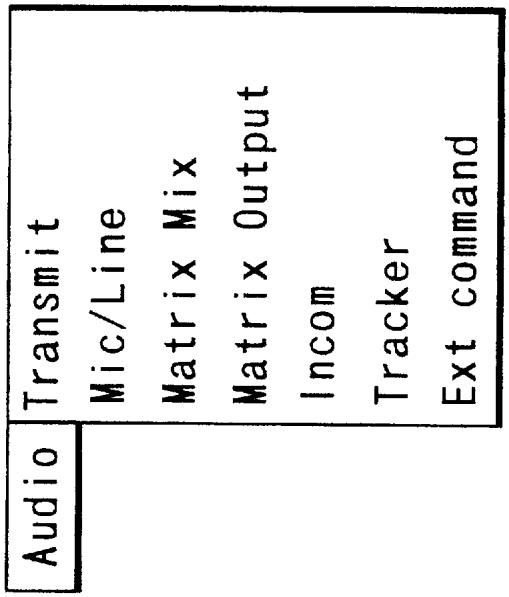
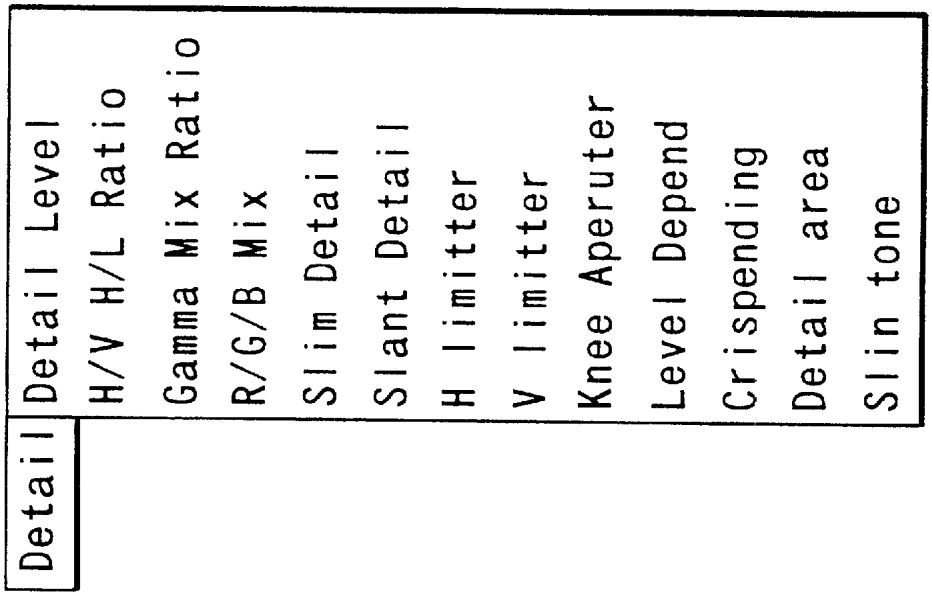


FIG. 11B



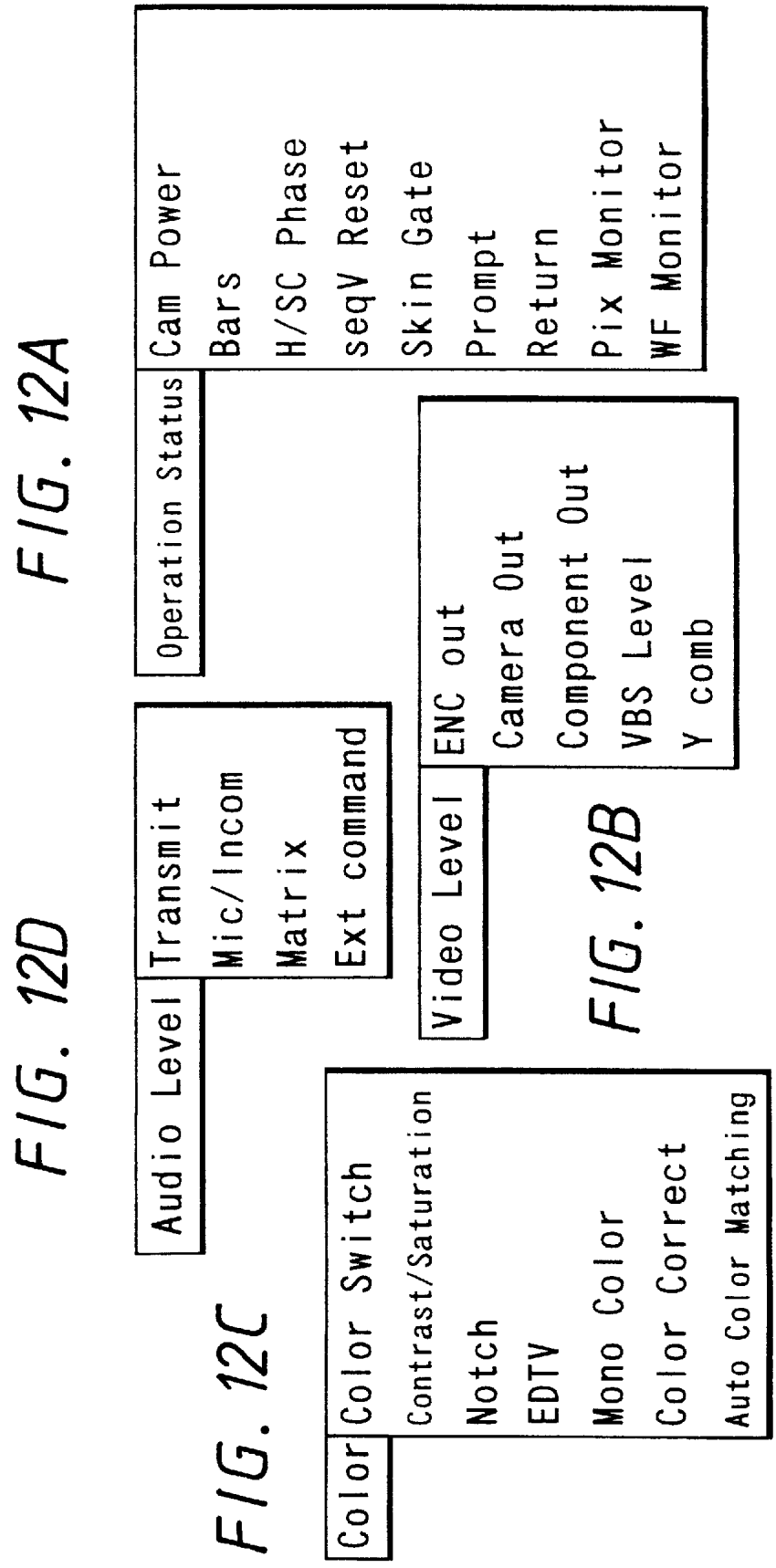


FIG. 12A

FIG. 12B

FIG. 12C

FIG. 12D

FIG. 13

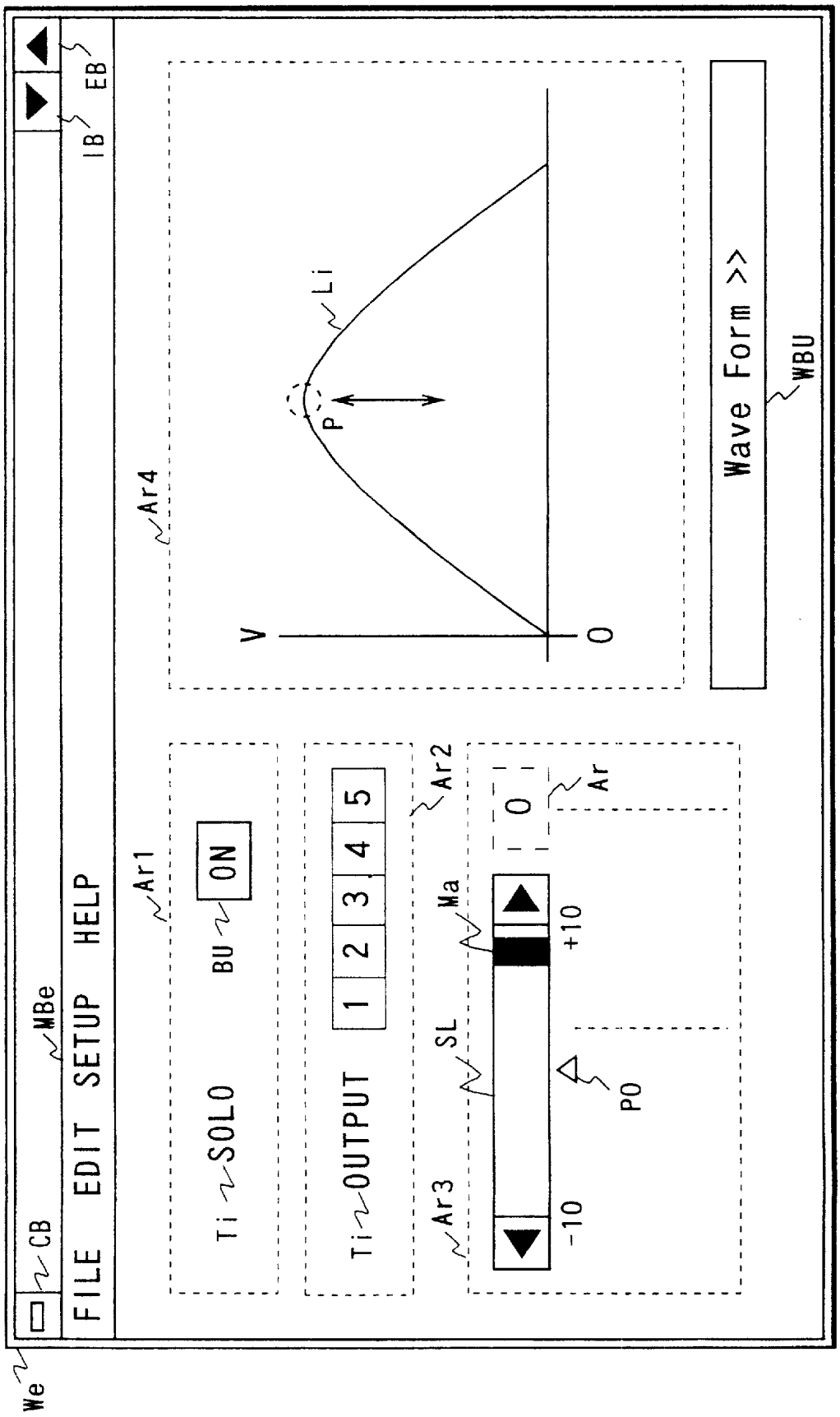

We
CB
MBe
FILE EDIT SETUP HELP
IB
EB
Ar1
Ti SOLO
BU
ON
Ti OUTPUT
1 2 3 4 5
Ar2
Ar3
SL
Ma
+10
-10
0
Ar
PO
Ar4
V
0
Li
P
Wave Form >>
WBU

FIG. 14

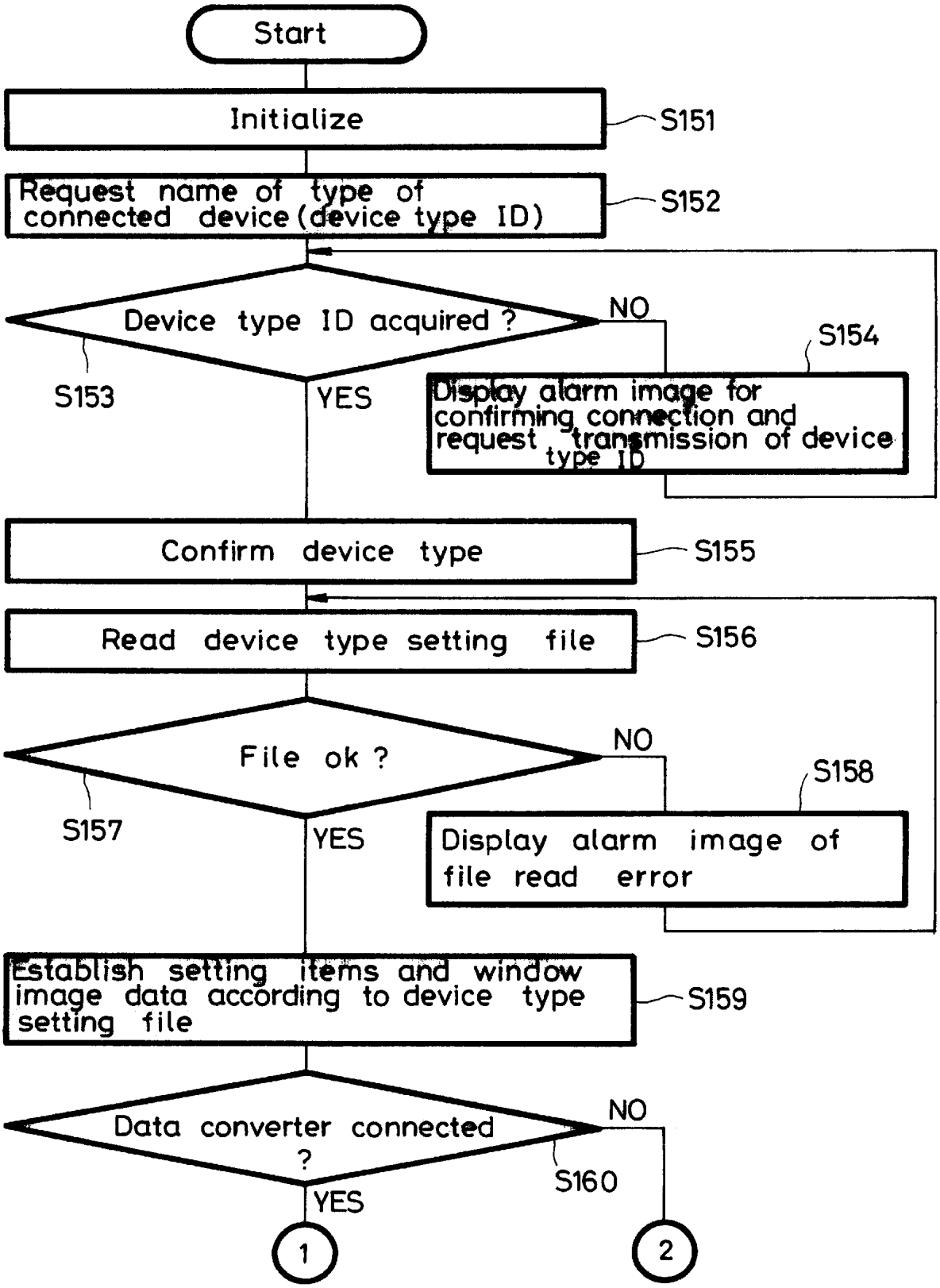

Start
Initialize
S151
Request name of type of connected device (device type ID)
S152
Device type ID acquired ?
NO
S154
S153
YES
Display alarm image for confirming connection and request transmission of device type ID
Confirm device type
S155
Read device type setting file
S156
File ok ?
NO
S158
S157
YES
Display alarm image of file read error
Establish setting items and window image data according to device type setting file
S159
Data converter connected ?
NO
S160
YES
1
2

FIG. 15

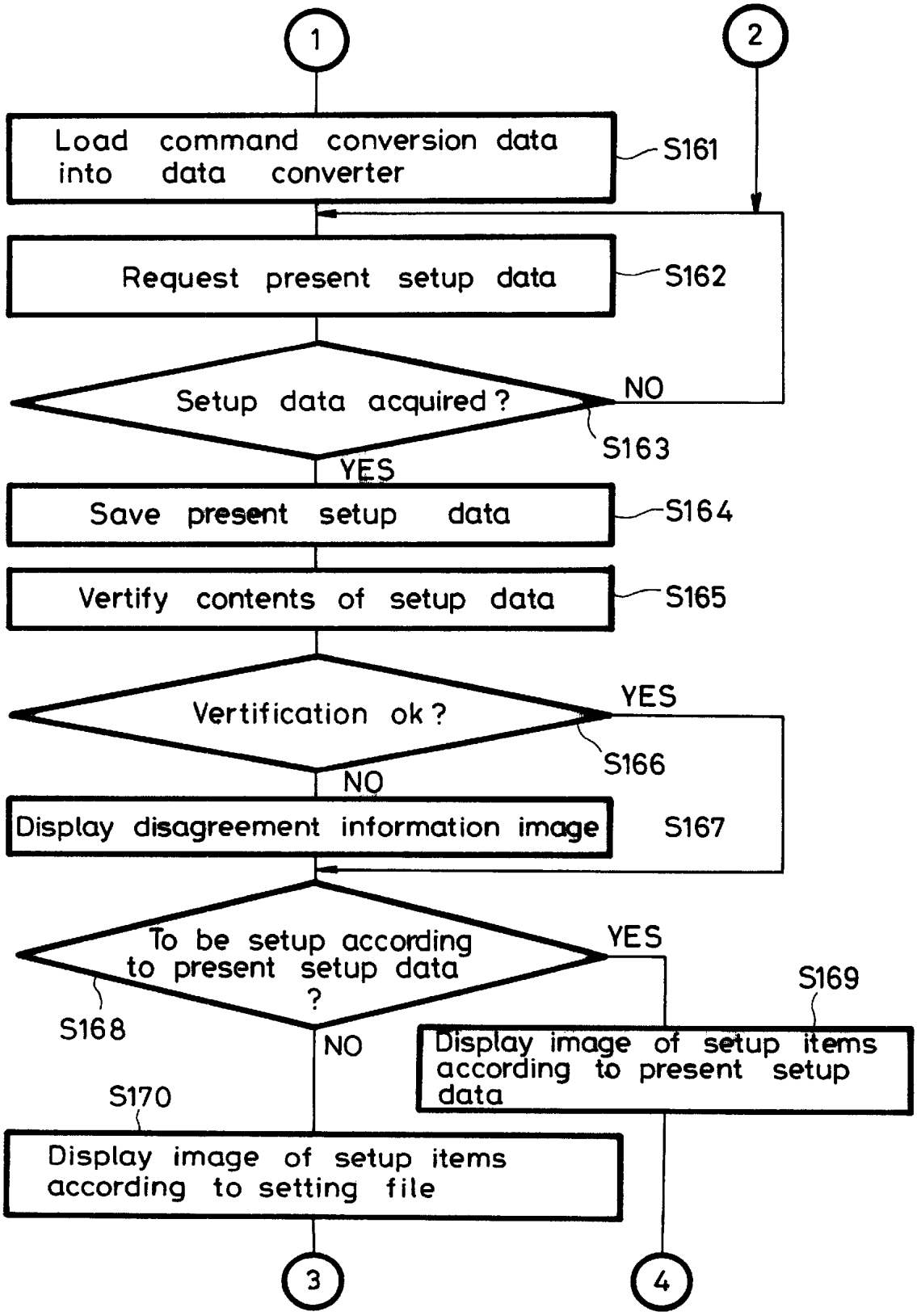

1
2
Load command conversion data into data converter
S161
Request present setup data
S162
Setup data acquired ?
NO
S163
YES
Save present setup data
S164
Vertify contents of setup data
S165
Vertification ok ?
YES
S166
NO
Display disagreement information image
S167
To be setup according to present setup data ?
YES
S168
S169
NO
Display image of setup items according to present setup data
S170
Display image of setup items according to setting file
3
4

FIG. 16

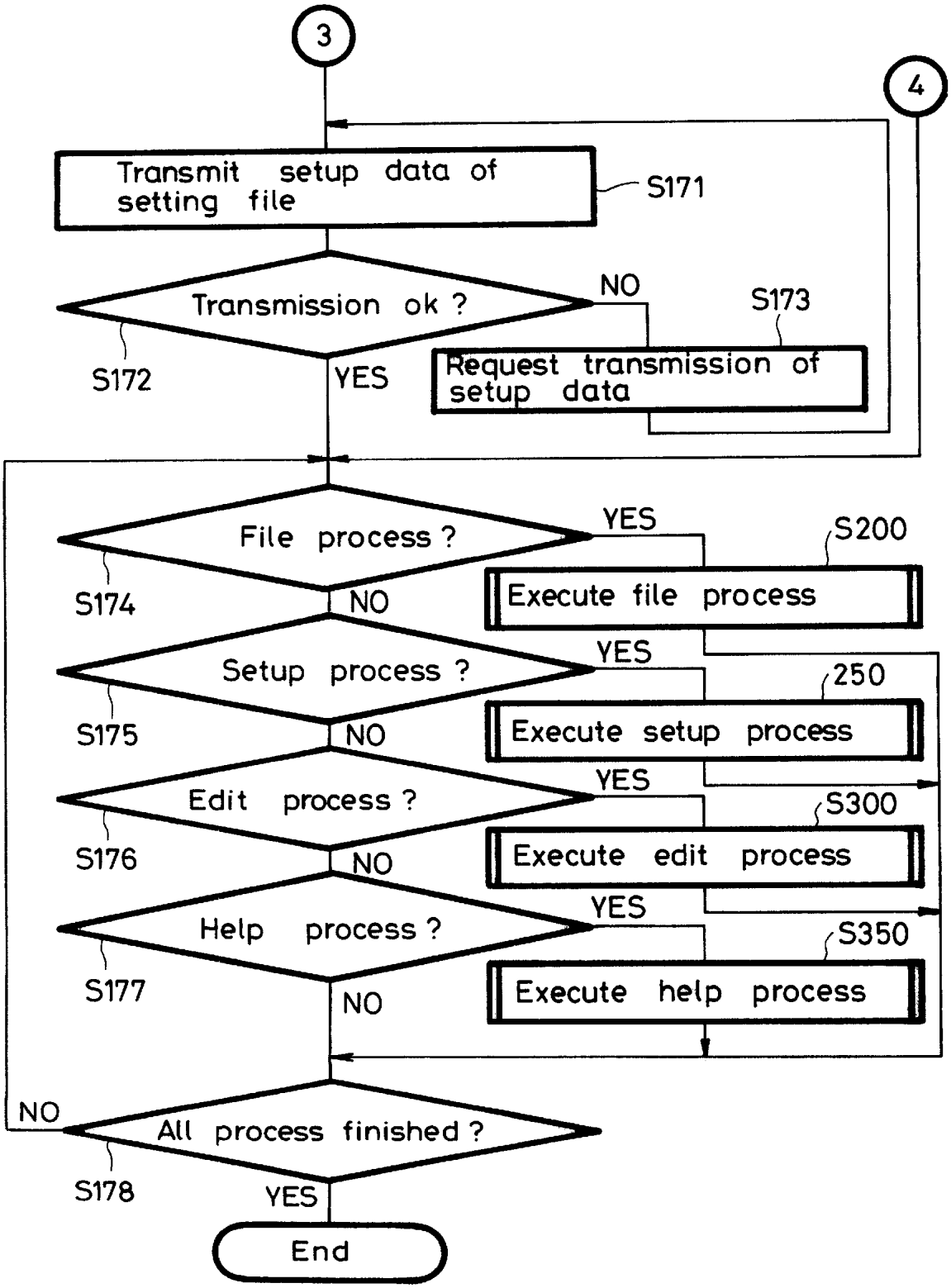

3
4
Transmit setup data of setting file
S171
Transmission ok ?
NO
S173
S172
YES
Request transmission of setup data
File process ?
YES
S200
S174
NO
Execute file process
Setup process ?
YES
250
S175
NO
Execute setup process
Edit process ?
YES
S300
S176
NO
Execute edit process
Help process ?
YES
S350
S177
NO
Execute help process
NO
All process finished ?
S178
YES
End

FIG. 17

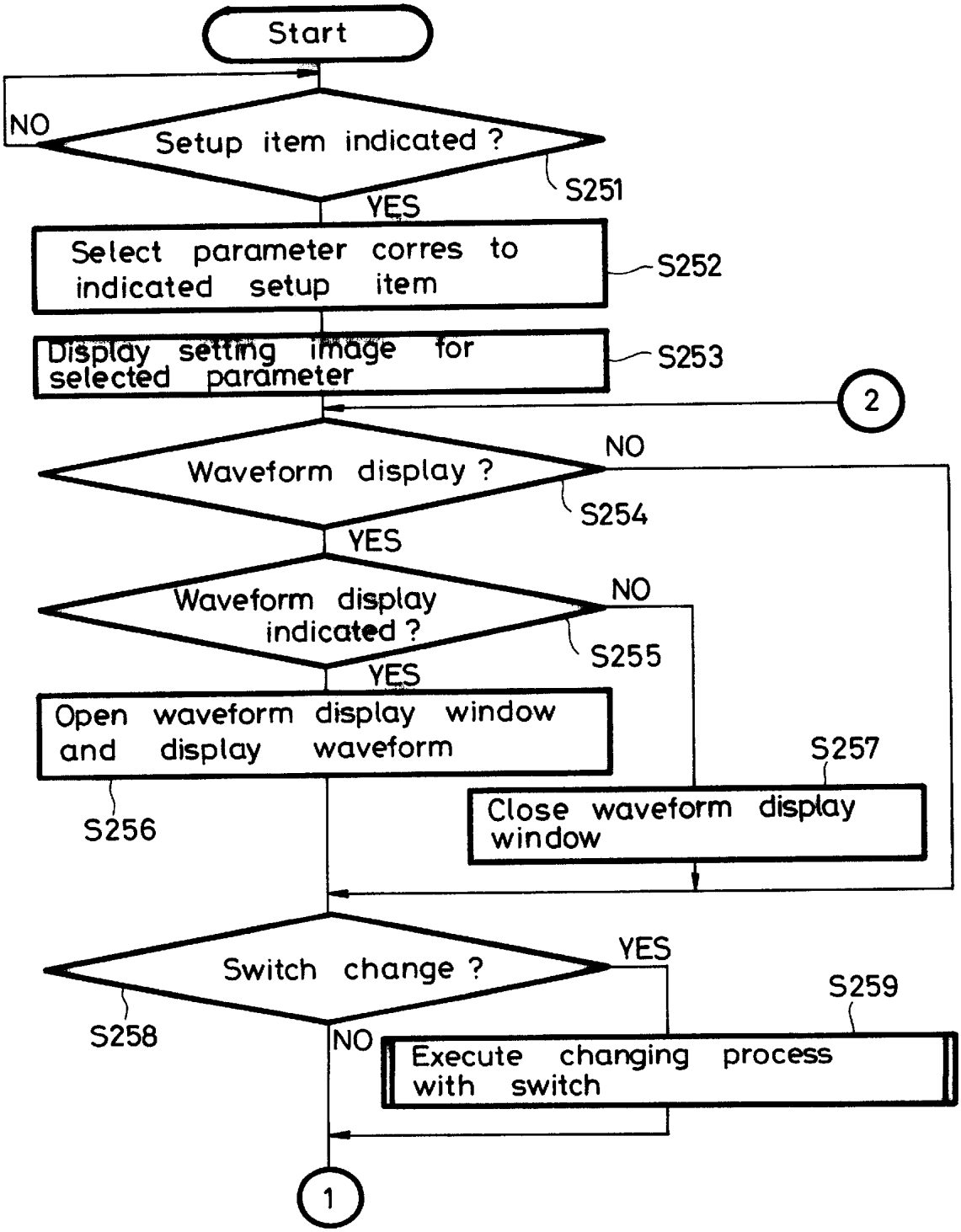

Start
NO
Setup item indicated ?
S251
YES
Select parameter corres to indicated setup item
S252
Display setting image for selected parameter
S253
2
Waveform display ?
NO
S254
YES
Waveform display indicated ?
NO
S255
YES
Open waveform display window and display waveform
S256
S257
Close waveform display window
Switch change ?
YES
S258
S259
NO
Execute changing process with switch
1

FIG. 18

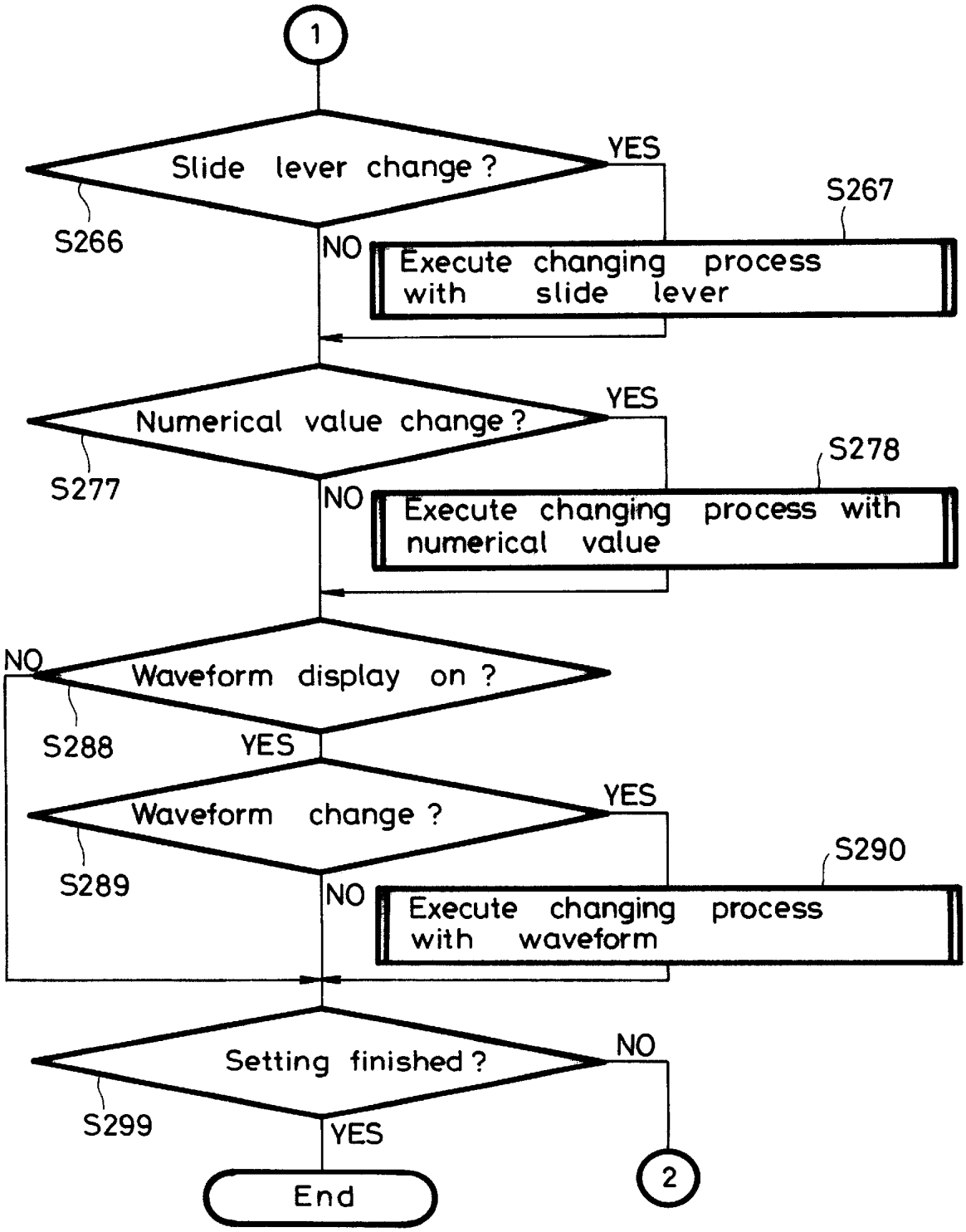

1
Slide lever change ?
YES
S266
S267
NO
Execute changing process with slide lever
Numerical value change ?
YES
S277
S278
NO
Execute changing process with numerical value
NO
Waveform display on ?
S288
YES
Waveform change ?
YES
S289
S290
NO
Execute changing process with waveform
Setting finished ?
NO
S299
YES
End
2

FIG. 19

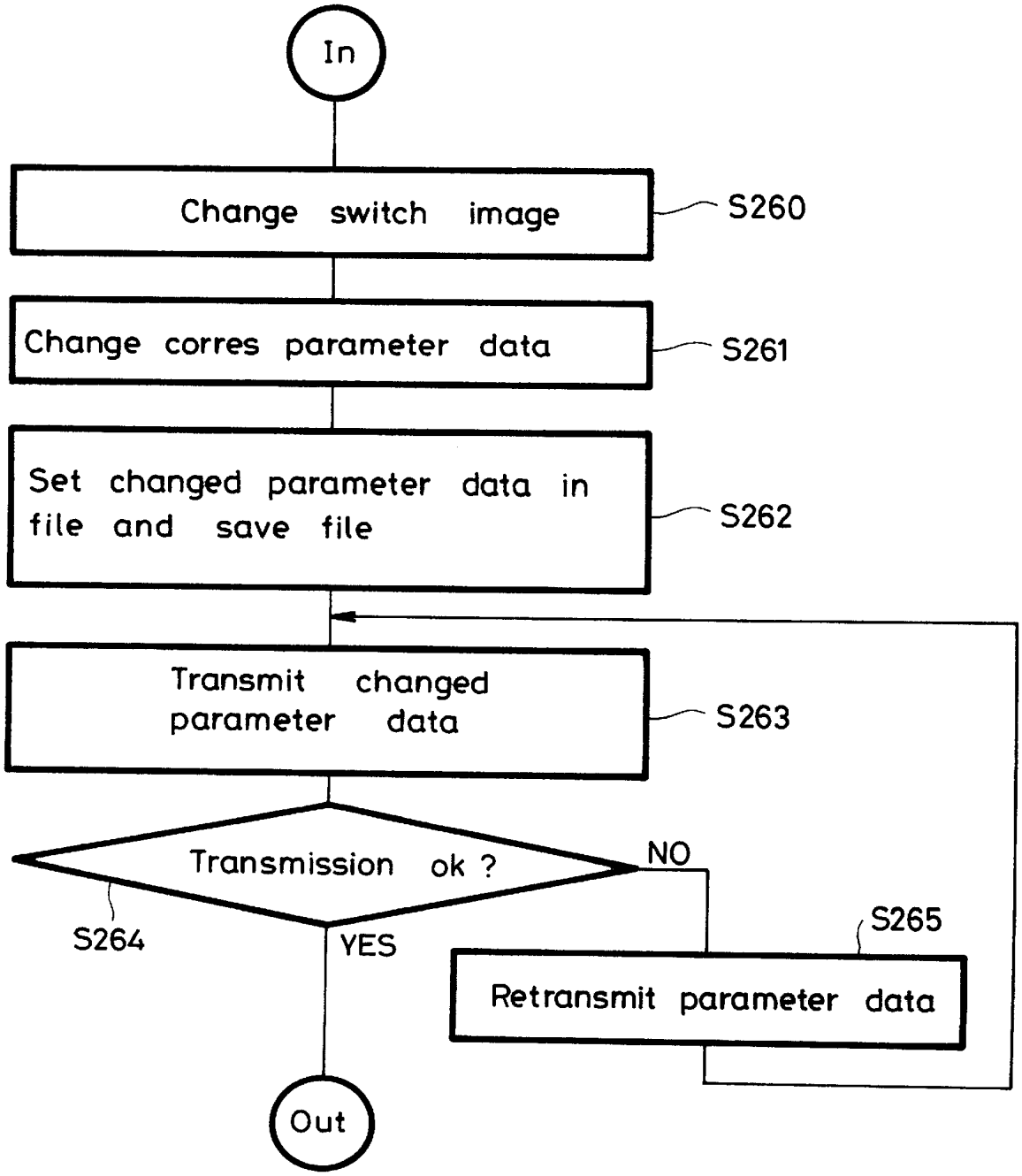

In
Change switch image
S260
Change corres parameter data
S261
Set changed parameter data in file and save file
S262
Transmit changed parameter data
S263
Transmission ok ?
NO
S264
YES
S265
Retransmit parameter data
Out

FIG. 20

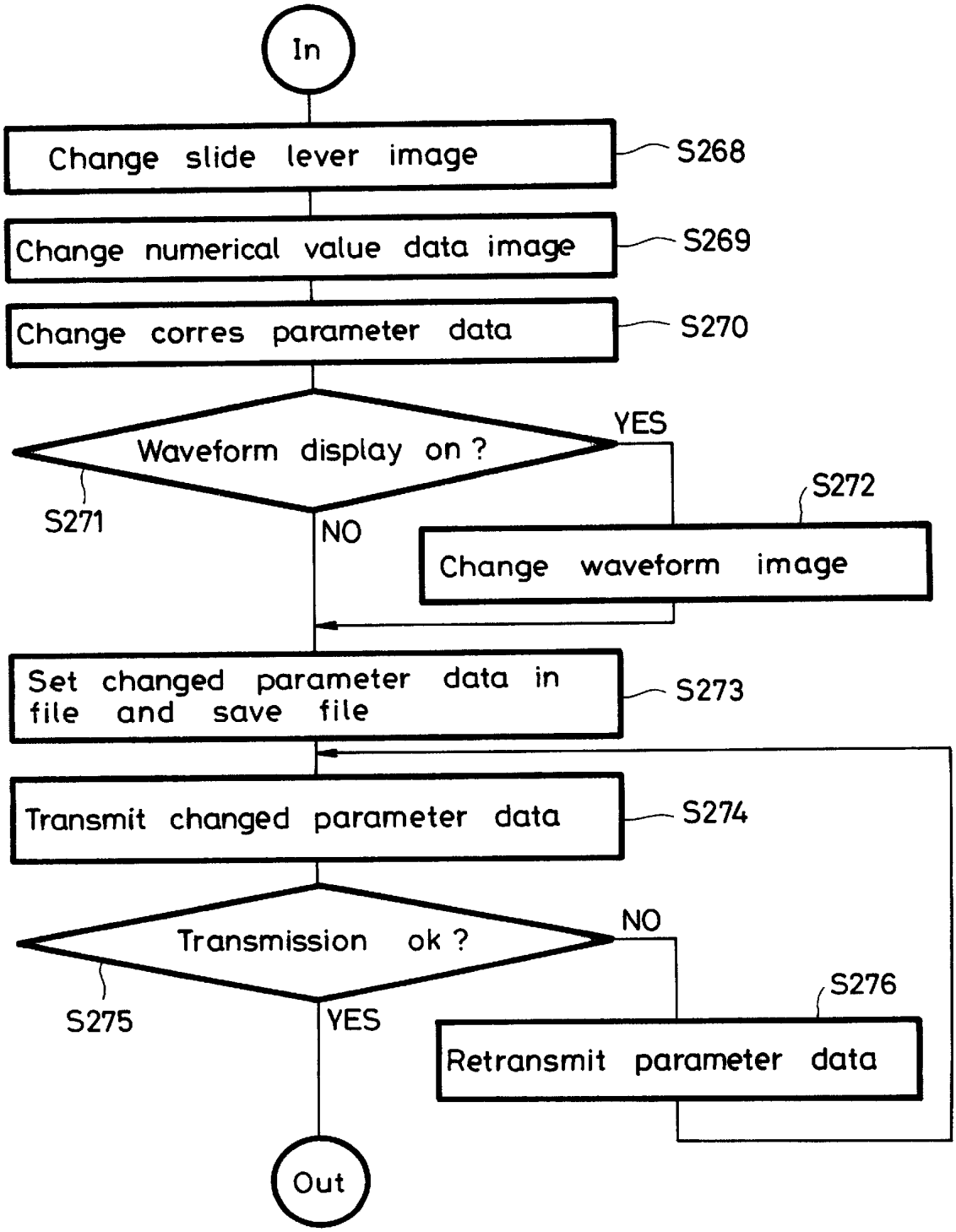

In
Change slide lever image
S268
Change numerical value data image
S269
Change corres parameter data
S270
Waveform display on ?
YES
S271
NO
S272
Change waveform image
Set changed parameter data in file and save file
S273
Transmit changed parameter data
S274
Transmission ok ?
NO
S275
YES
S276
Retransmit parameter data
Out

FIG. 21

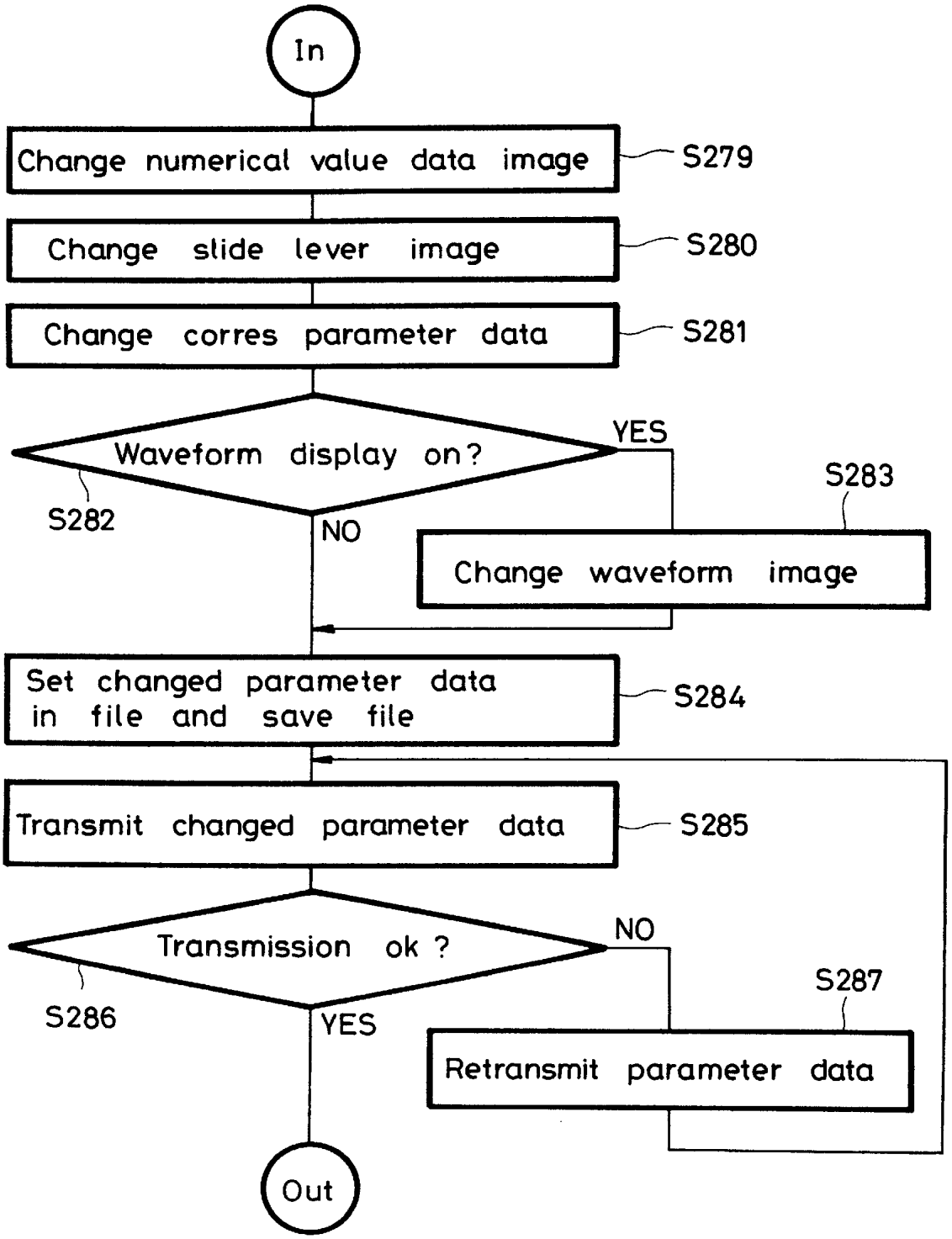
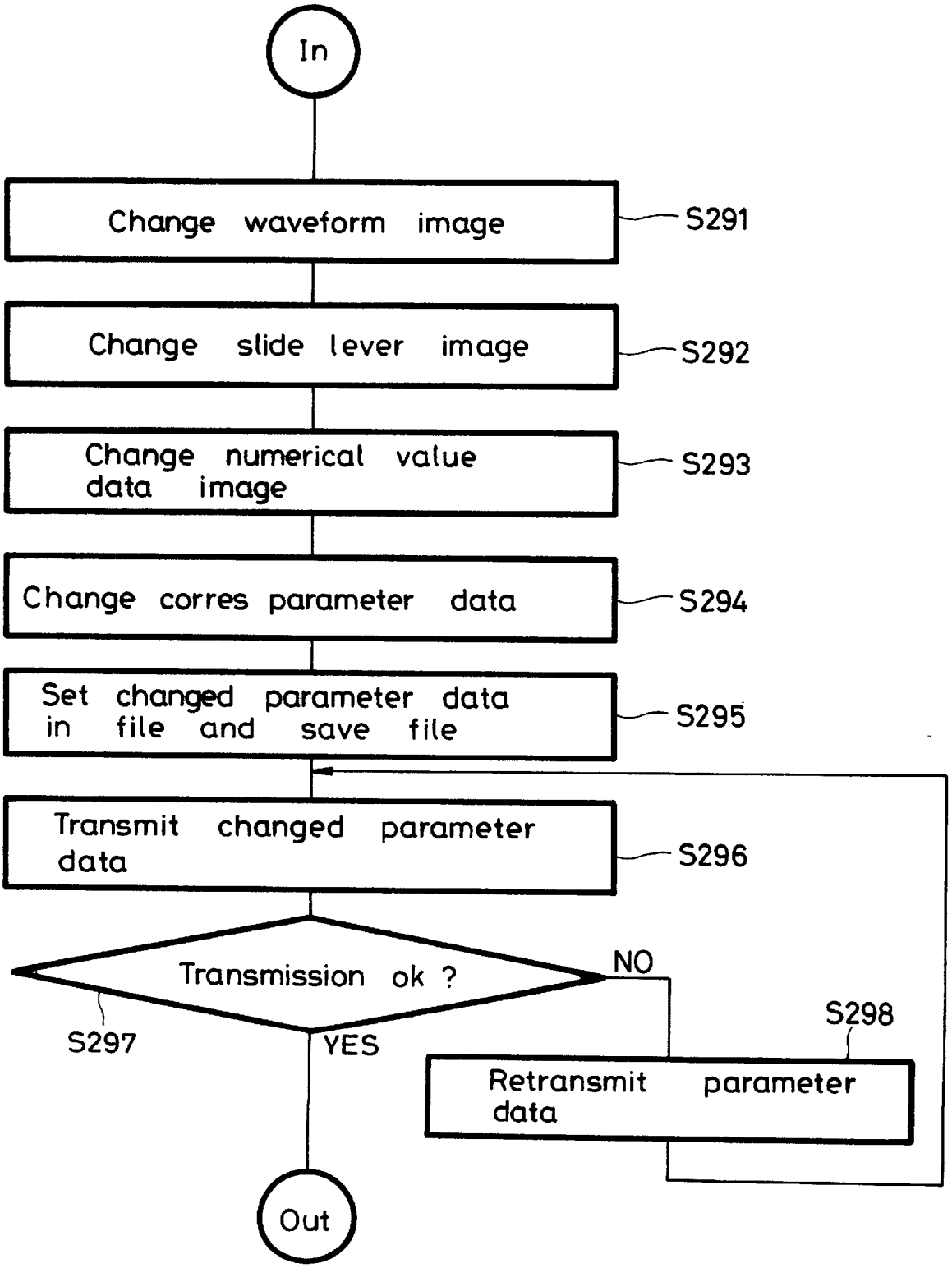

In
Change numerical value data image
S279
Change slide lever image
S280
Change corres parameter data
S281
Waveform display on?
YES
S282
NO
S283
Change waveform image
Set changed parameter data in file and save file
S284
Transmit changed parameter data
S285
Transmission ok ?
NO
S286
YES
S287
Retransmit parameter data
Out

FIG. 22


In
Change waveform image
S291
Change slide lever image
S292
Change numerical value data image
S293
Change corres parameter data
S294
Set changed parameter data in file and save file
S295
Transmit changed parameter data
S296
Transmission ok ?
NO
S297
YES
S298
Retransmit parameter data
Out

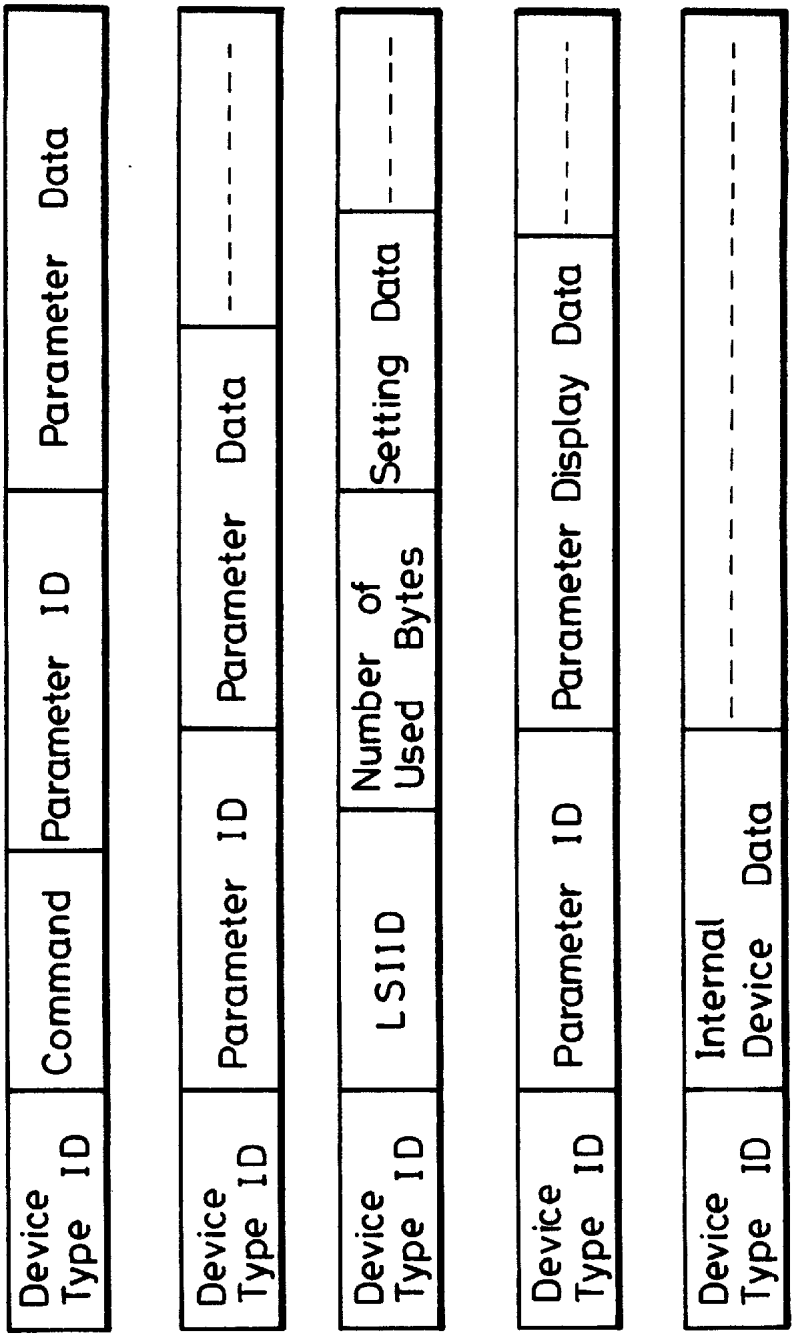


FIG. 23A

FIG. 23B

FIG. 23C

FIG. 23D

FIG. 23E

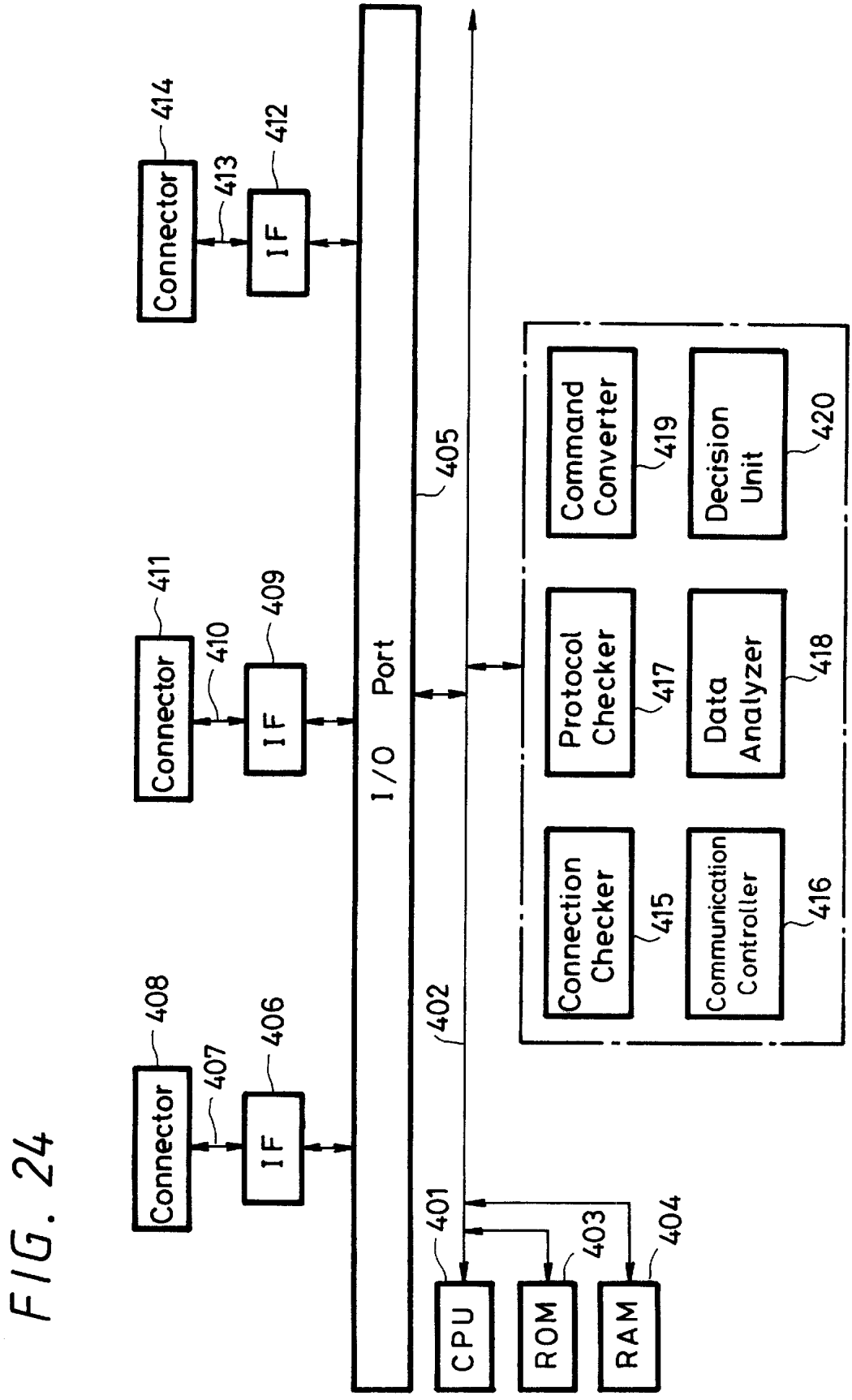

Connector
414
413
IF
412
Connector
411
410
IF
409
Connector
408
407
IF
406
I/O Port
405
402
Command Converter
419
Decision Unit
420
Protocol Checker
417
Data Analyzer
418
Connection Checker
415
Communication Controller
416
CPU
401
ROM
403
RAM
404

FIG. 24

FIG. 25

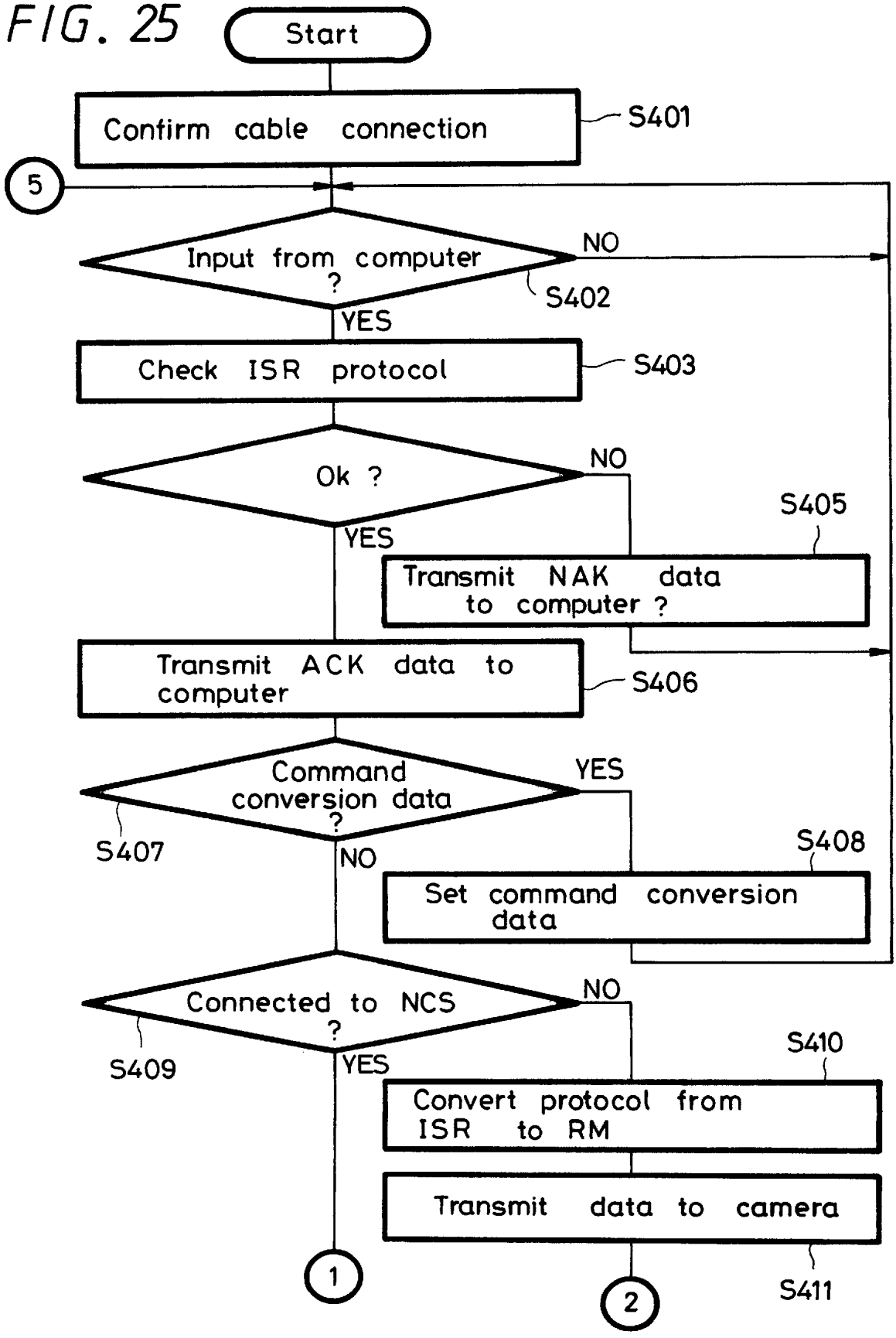

Start
Confirm cable connection
S401
5
Input from computer ?
NO
S402
YES
Check ISR protocol
S403
Ok ?
NO
S405
YES
Transmit NAK data to computer ?
Transmit ACK data to computer
S406
Command conversion data ?
YES
S407
NO
S408
Set command conversion data
Connected to NCS ?
NO
S409
YES
S410
Convert protocol from ISR to RM
Transmit data to camera
S411
1
2

FIG. 26

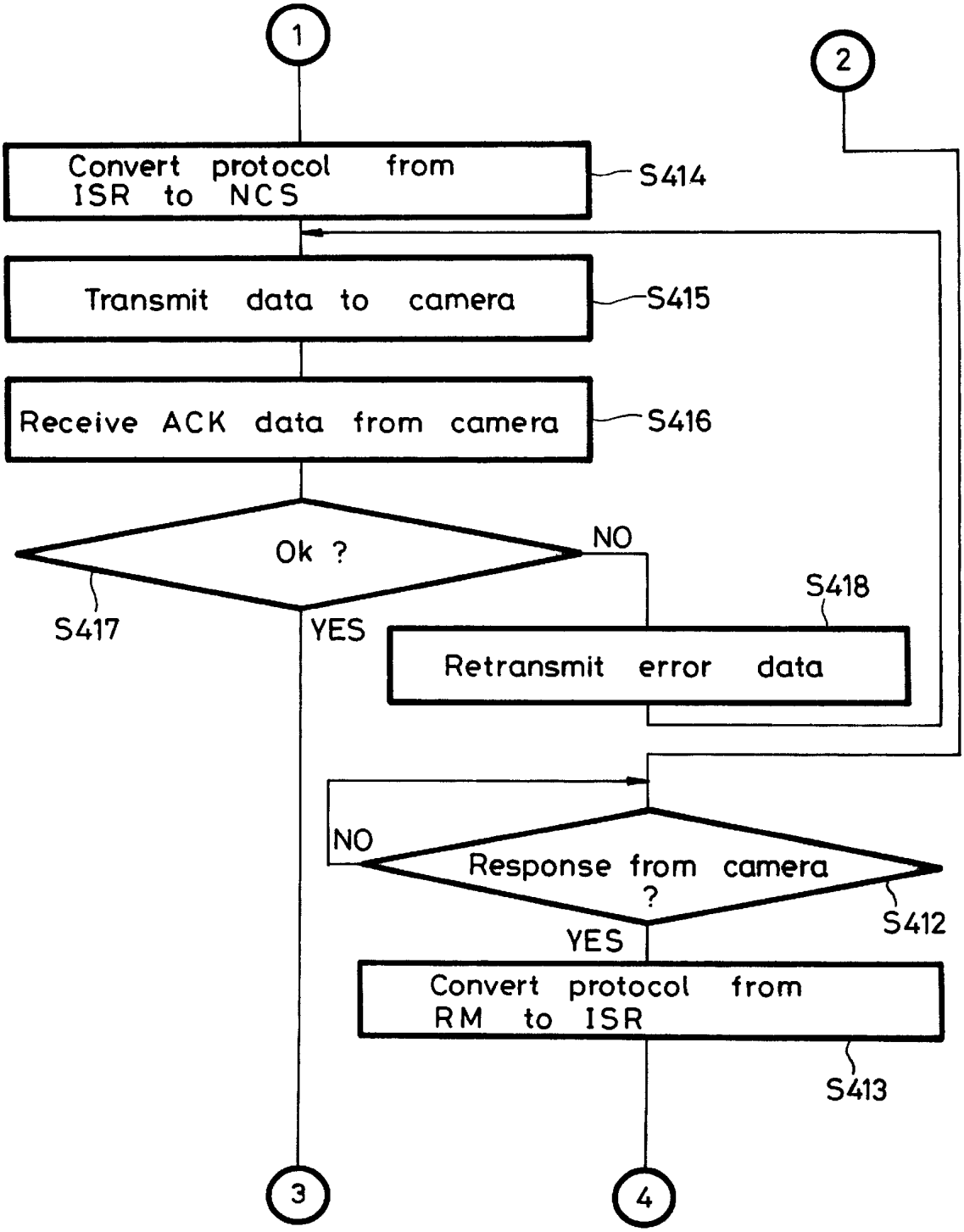
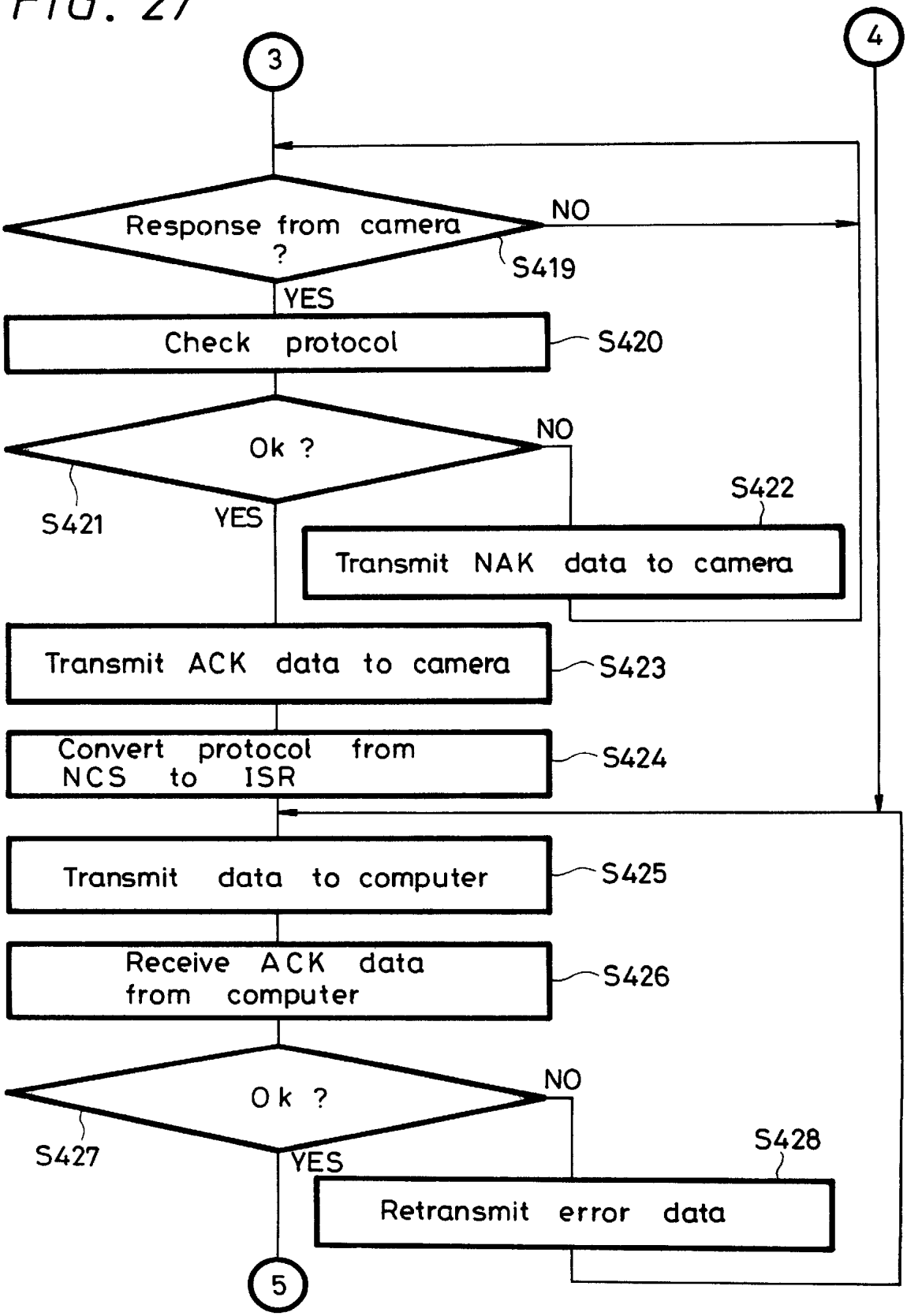

1
2
Convert protocol from ISR to NCS
S414
Transmit data to camera
S415
Receive ACK data from camera
S416
Ok ?
NO
S417
YES
S418
Retransmit error data
NO
Response from camera ?
S412
YES
Convert protocol from RM to ISR
S413
3
4

FIG. 27


3
4
Response from camera ?
NO
S419
YES
Check protocol
S420
Ok ?
NO
S421
YES
S422
Transmit NAK data to camera
Transmit ACK data to camera
S423
Convert protocol from NCS to ISR
S424
Transmit data to computer
S425
Receive ACK data from computer
S426
Ok ?
NO
S427
YES
S428
Retransmit error data
5

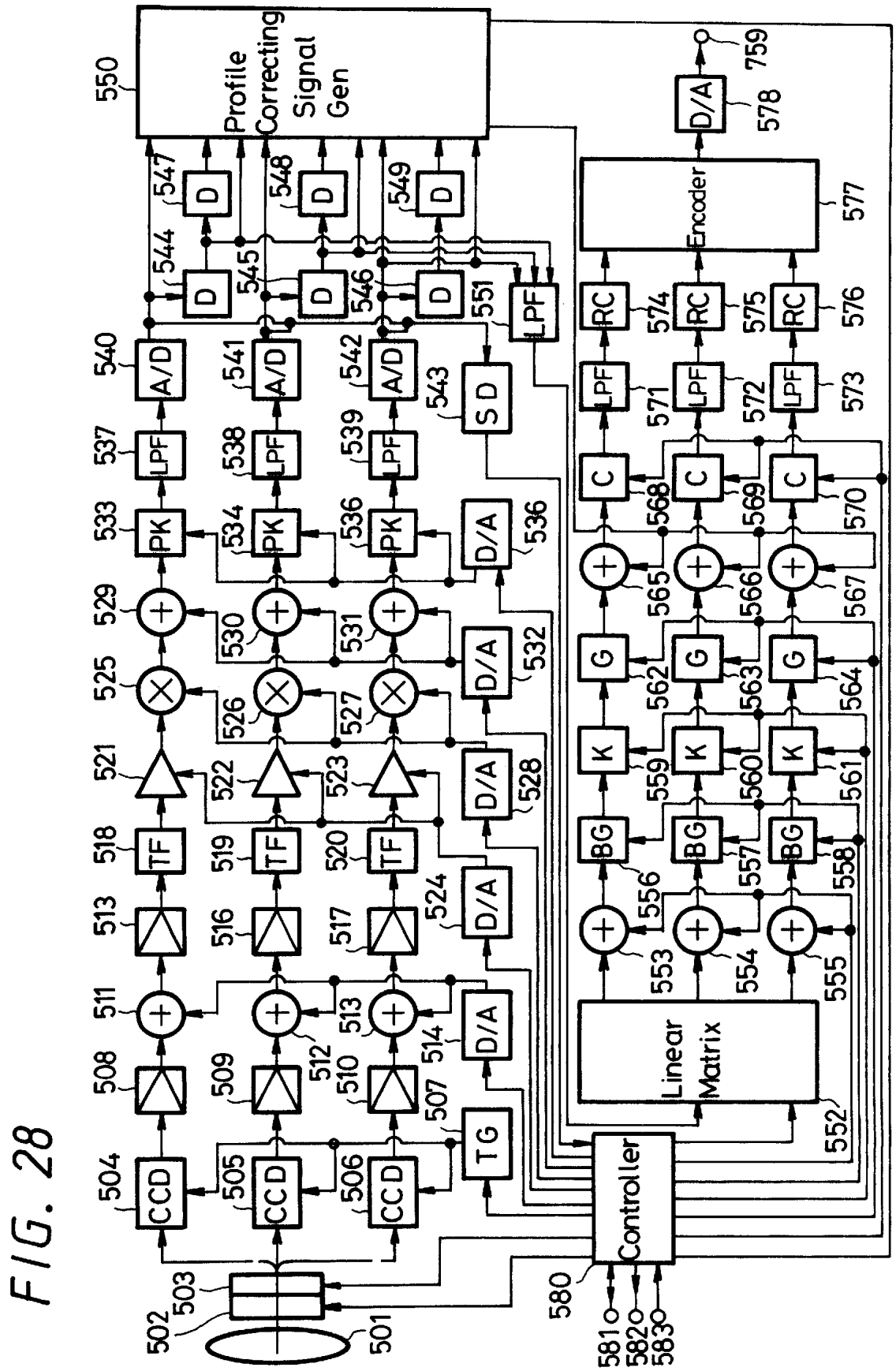

Profile Correcting Signal Gen
Encoder
Linear Matrix
Controller
CCD
A/D
LPF
PK
TF
TG
SD
D
D/A
RC
C
G
K
BG
LPF

FIG. 28

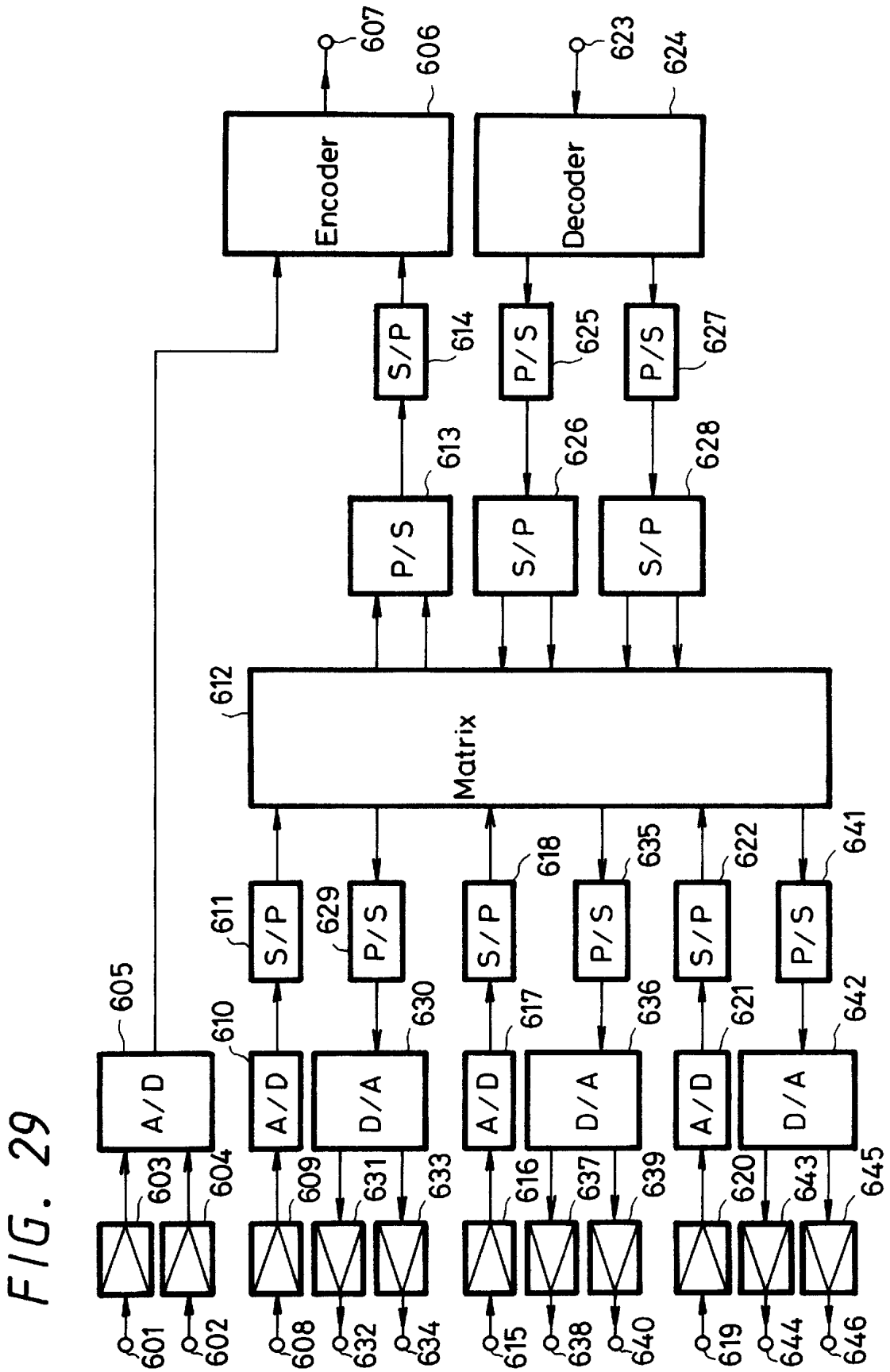

Encoder
Decoder
Matrix
A/D
D/A
S/P
P/S
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646

FIG. 29

FIG. 30A

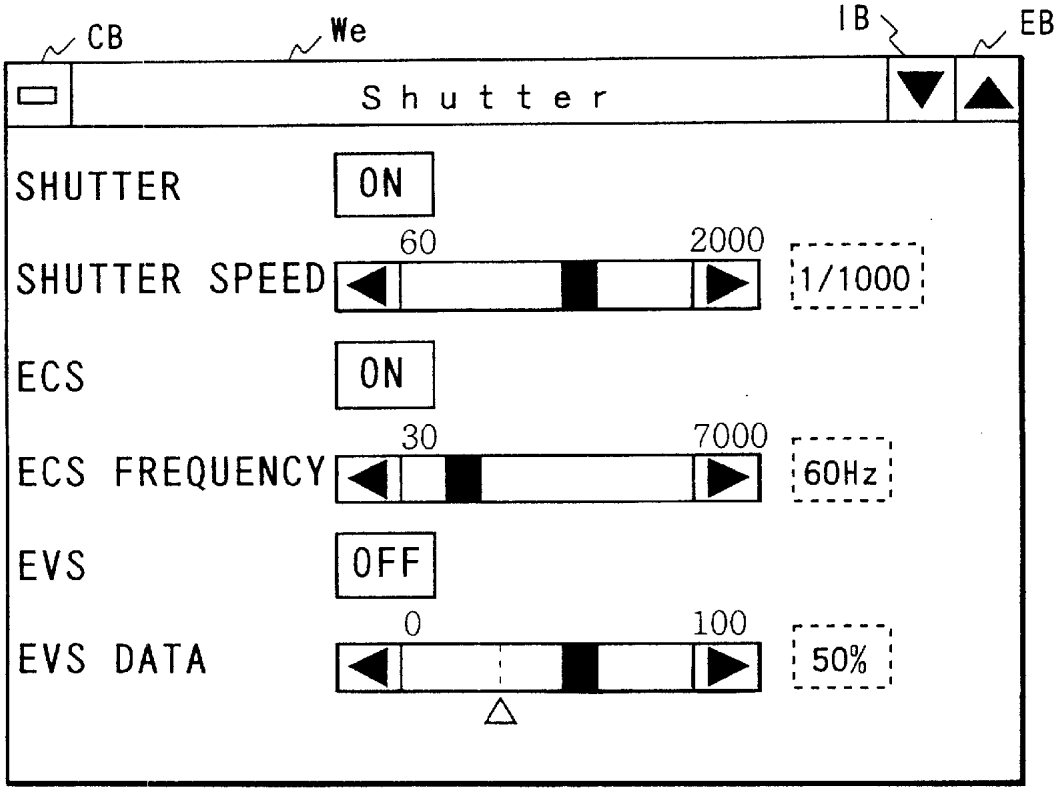


FIG. 30B

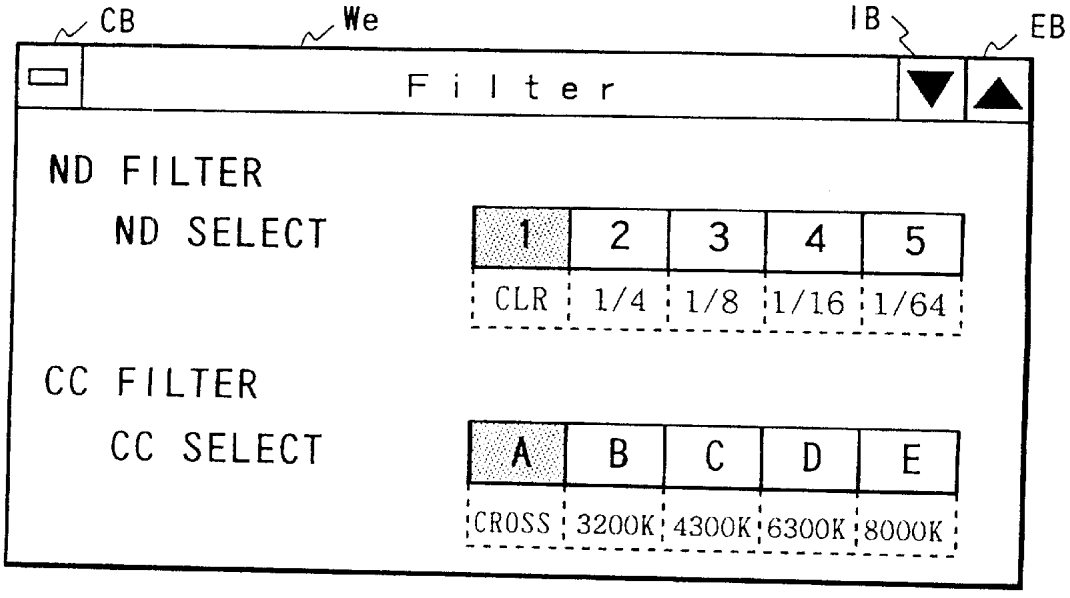


FIG. 31A

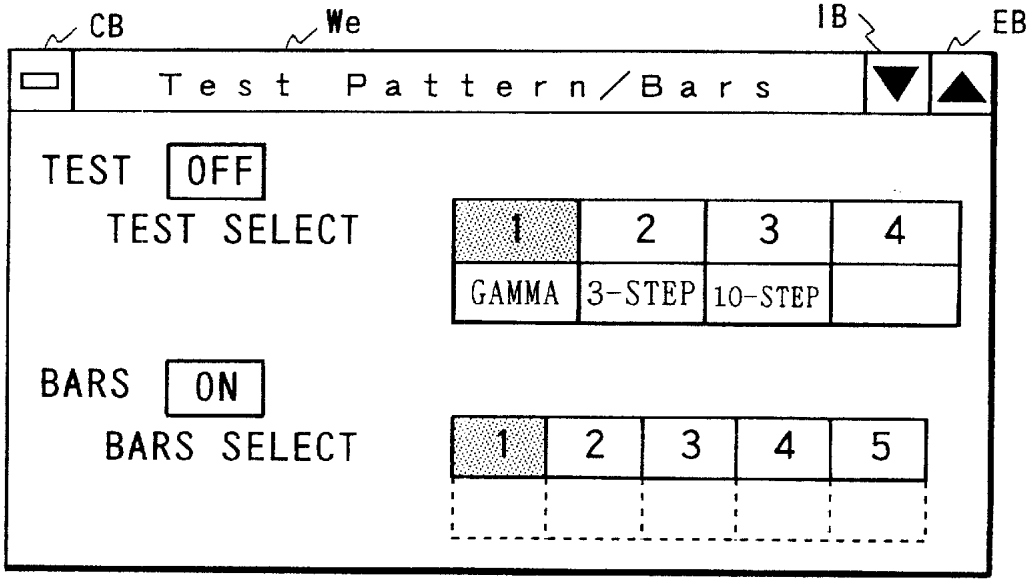


FIG. 31B

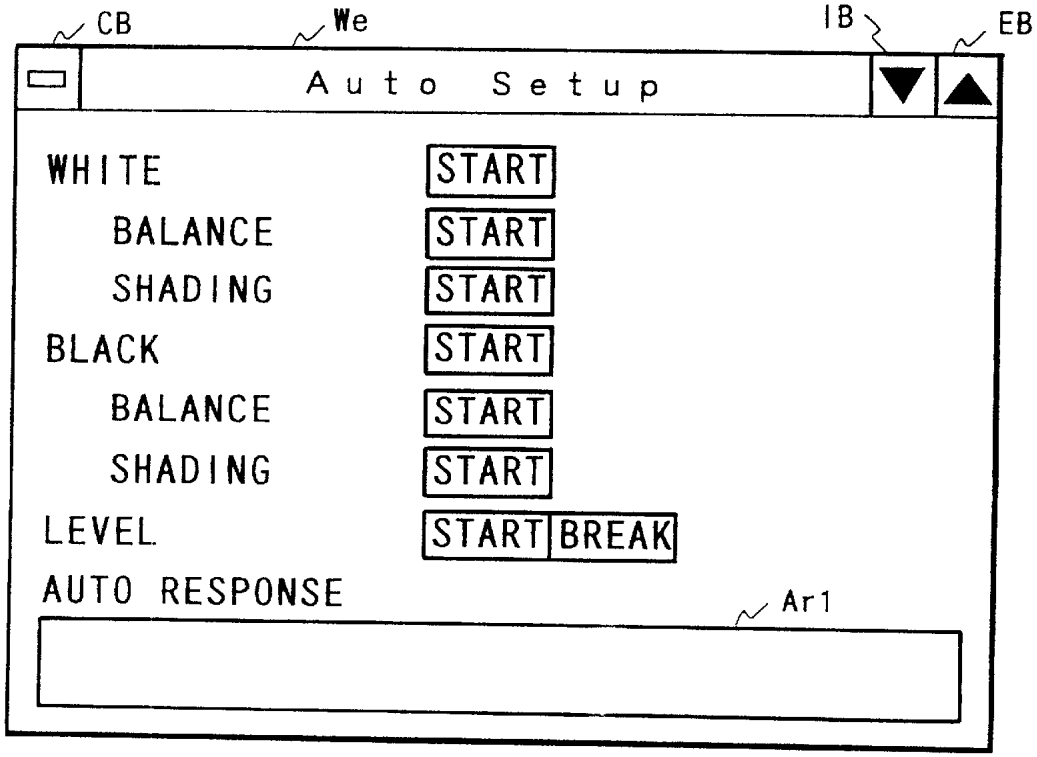


FIG. 32A

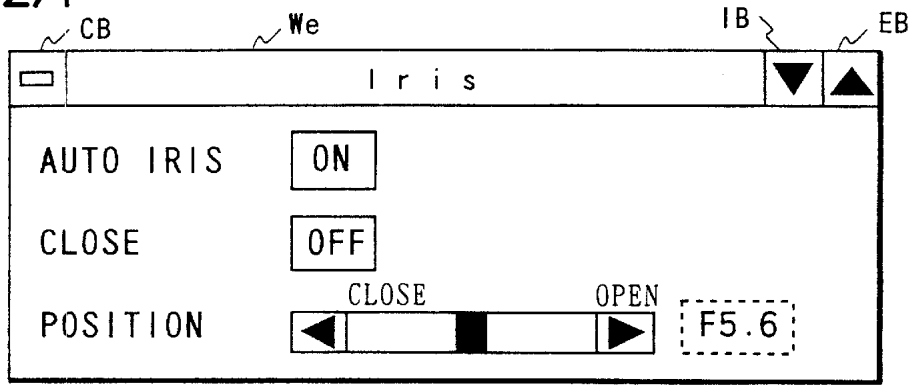


FIG. 32B

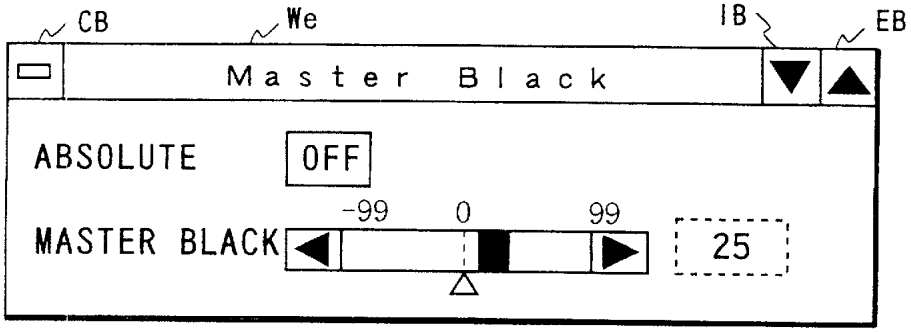


FIG. 32C

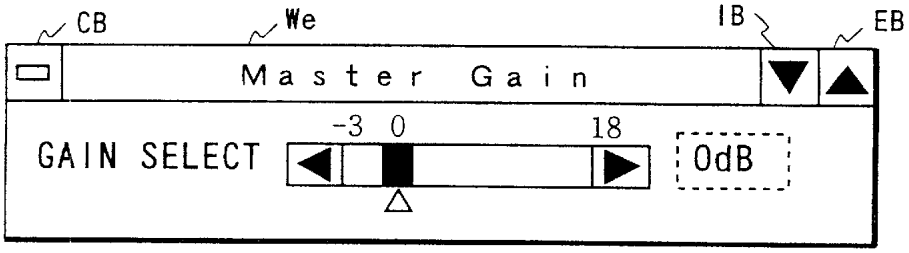


FIG. 33

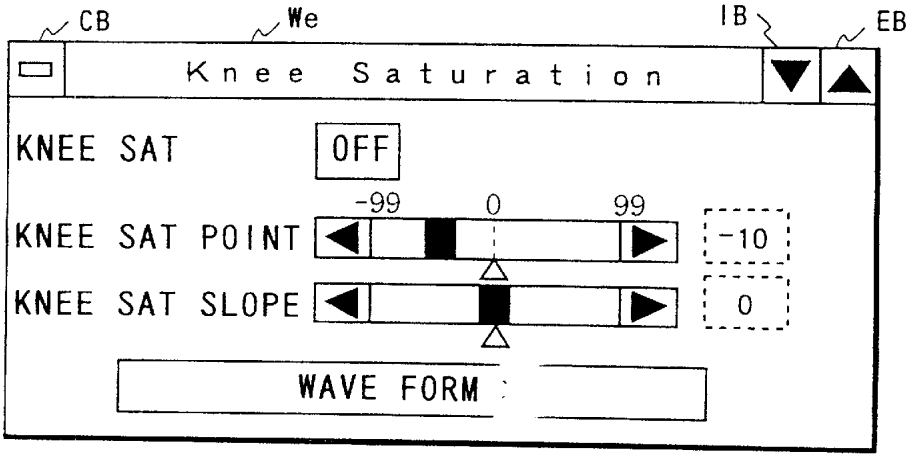


FIG. 34

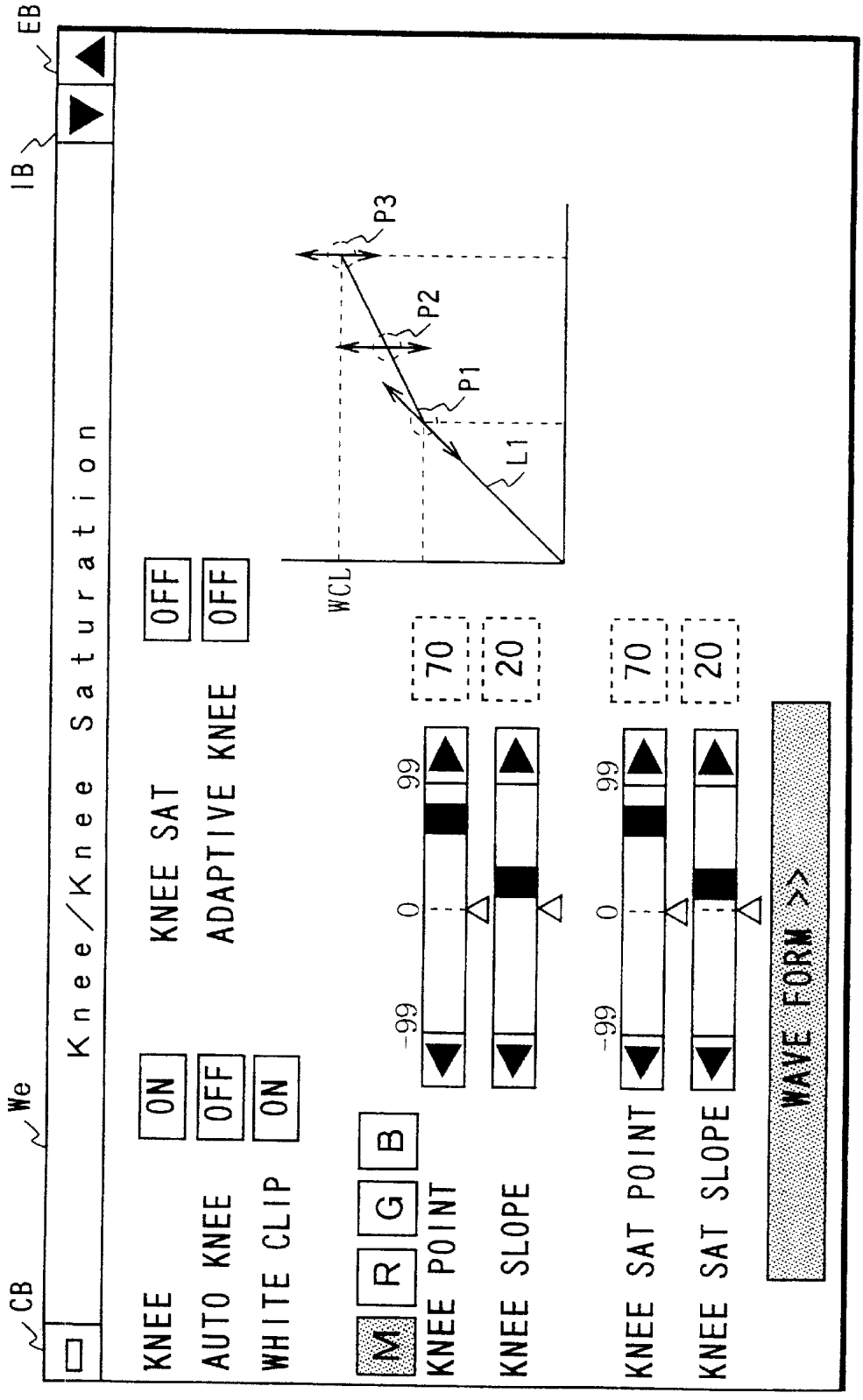

EB
IB
We
CB
Knee/Knee Saturation
KNEE
ON
AUTO KNEE
OFF
WHITE CLIP
ON
KNEE SAT
OFF
ADAPTIVE KNEE
OFF
M
R
G
B
KNEE POINT
KNEE SLOPE
99
0
-99
70
20
P3
P2
P1
L1
WCL
KNEE SAT POINT
KNEE SAT SLOPE
WAVE FORM >>

FIG. 35

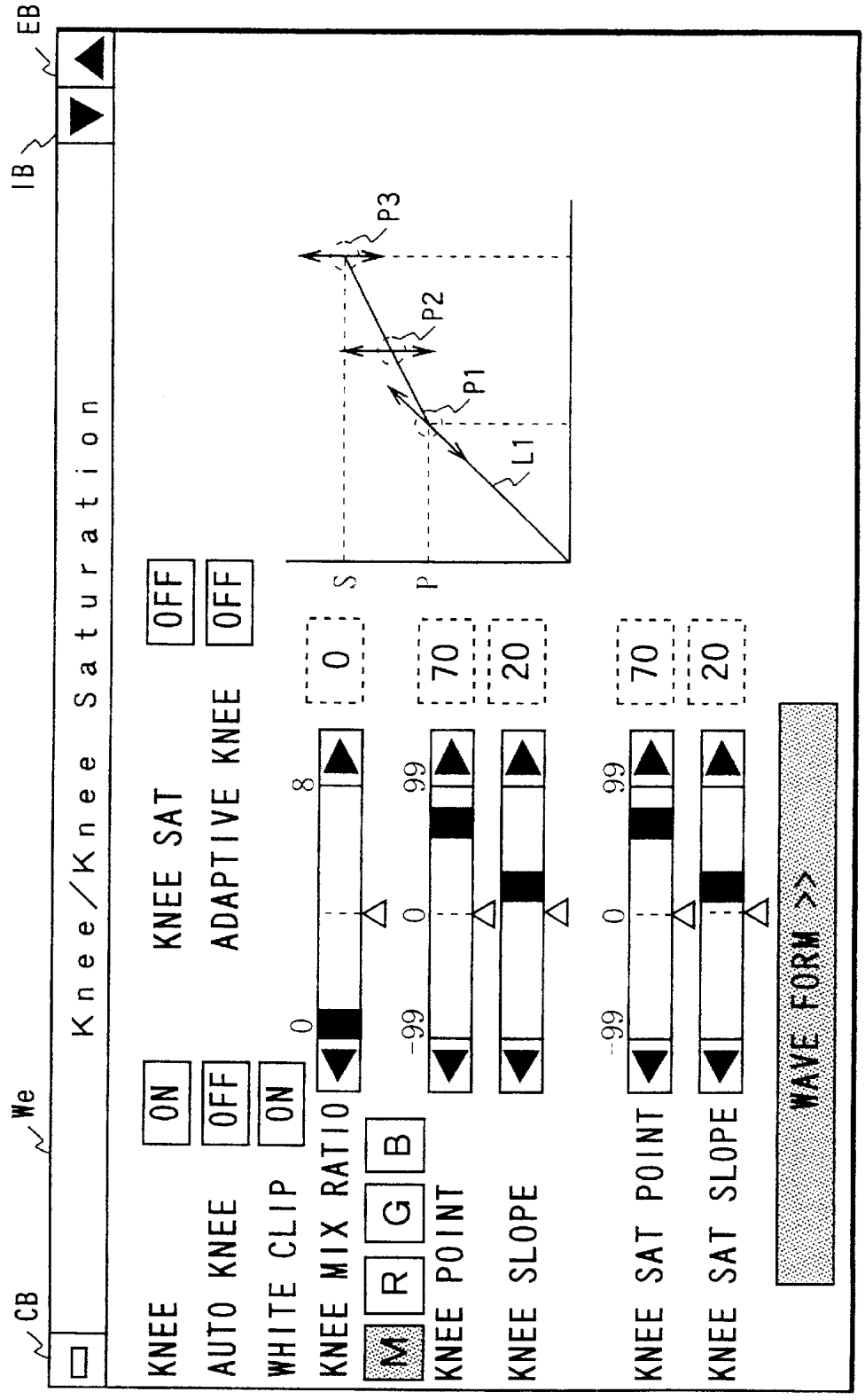

CB
We
IB
EB
Knee/Knee Saturation
KNEE
AUTO KNEE
WHITE CLIP
KNEE MIX RATIO
M
R
G
B
KNEE POINT
KNEE SLOPE
KNEE SAT POINT
KNEE SAT SLOPE
ON
OFF
ON
KNEE SAT
ADAPTIVE KNEE
OFF
OFF
0
8
0
99
0
-99
70
20
99
0
-99
70
20
P3
P2
P1
L1
S
P
WAVE FORM >>

FIG. 36A

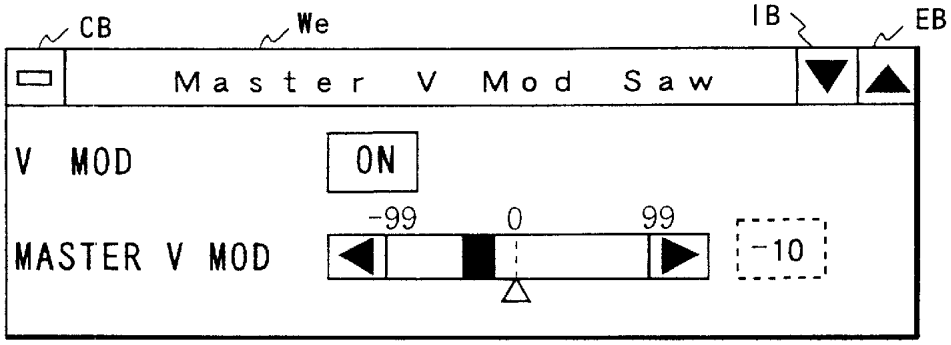


FIG. 36B

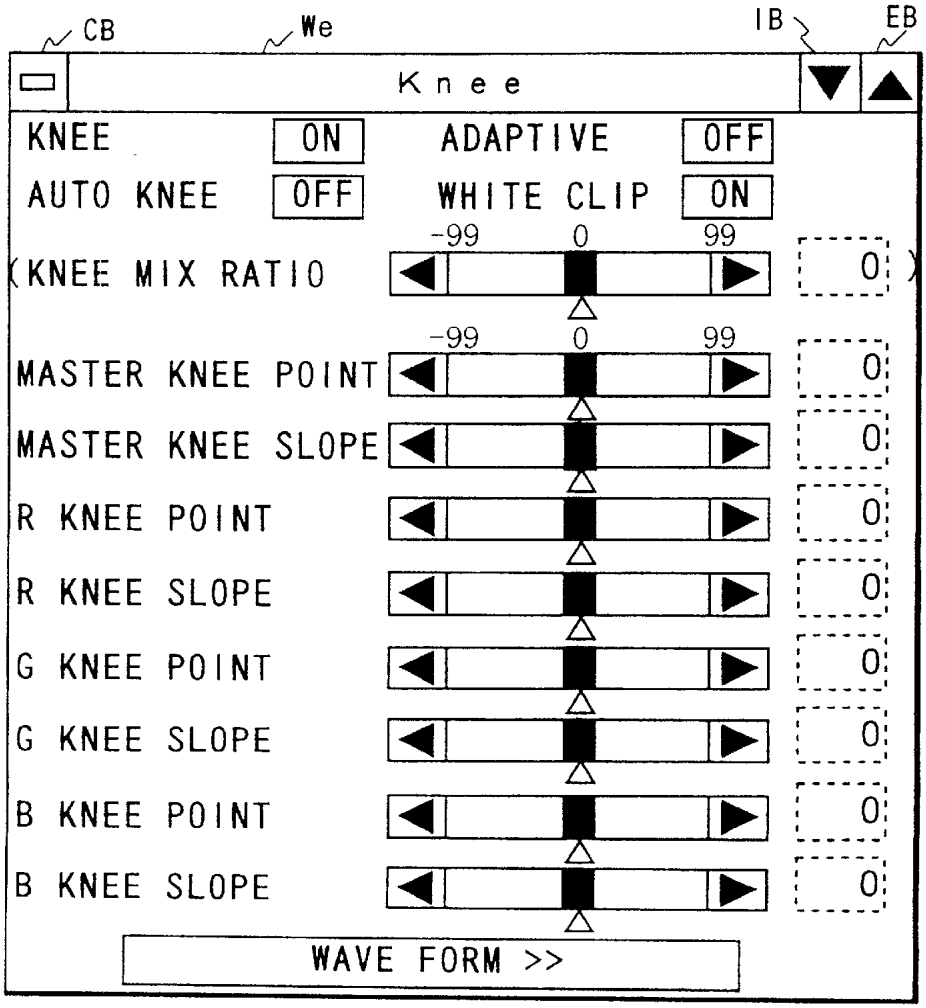


FIG. 37A

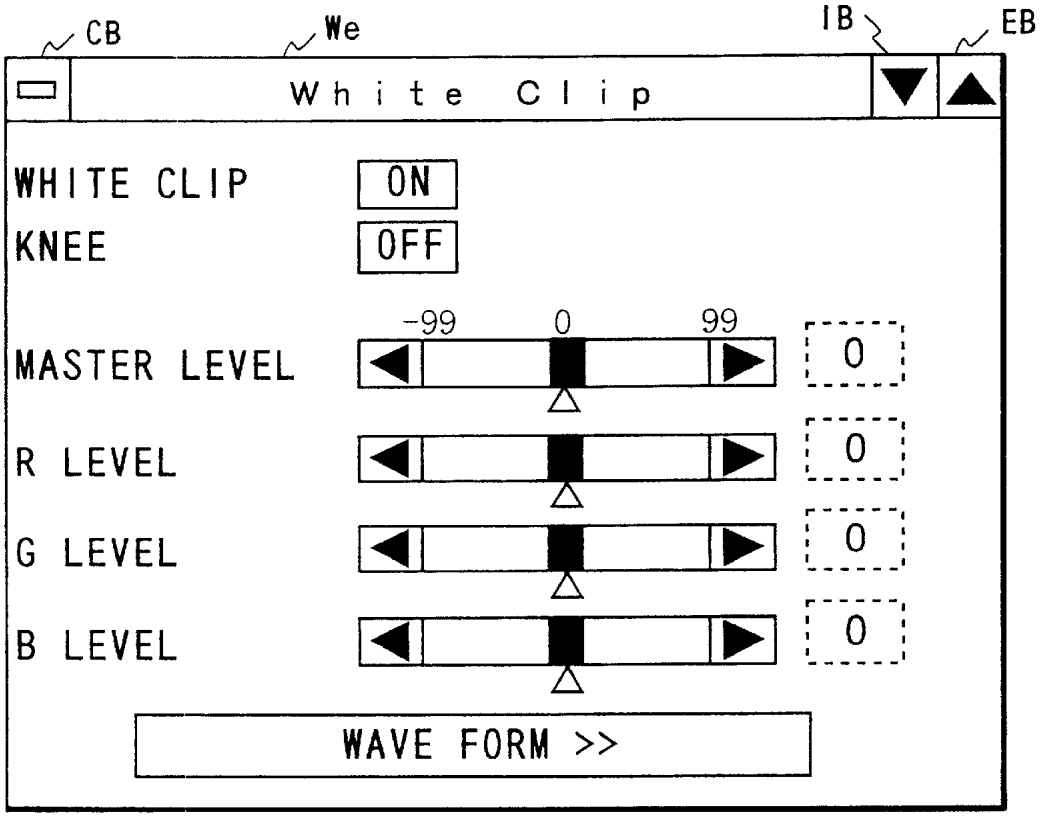


FIG. 37B

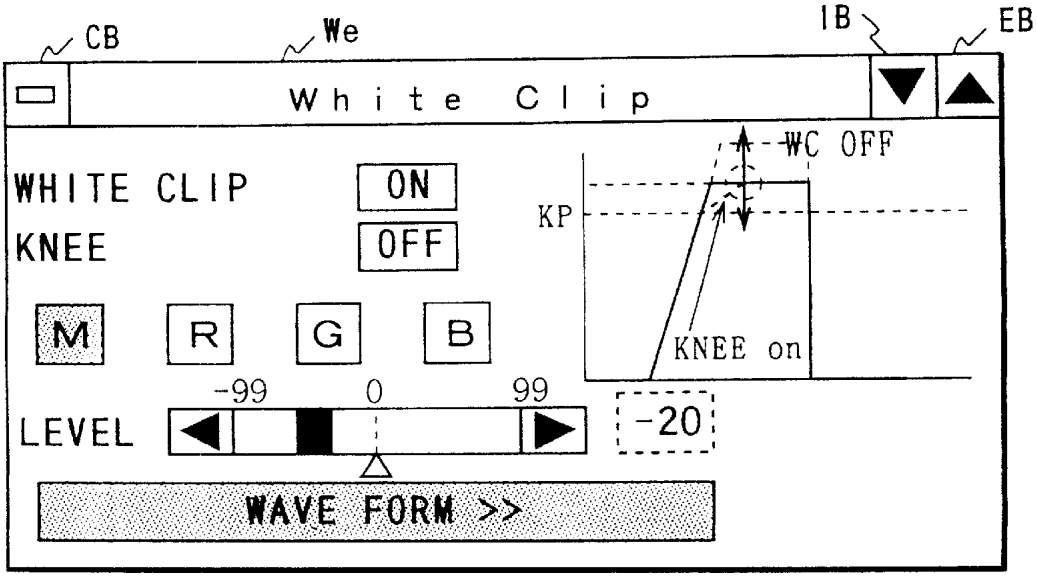


FIG. 38A

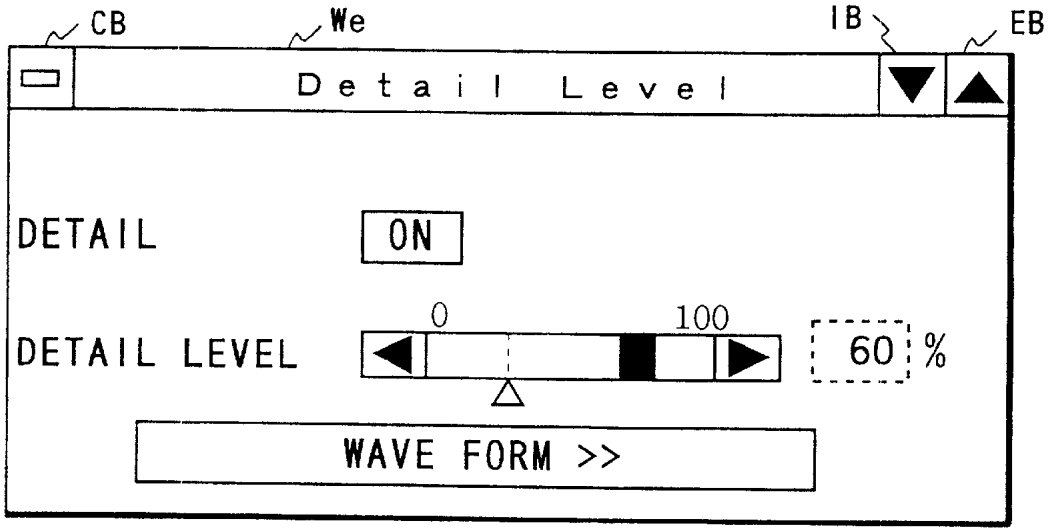


FIG. 38B

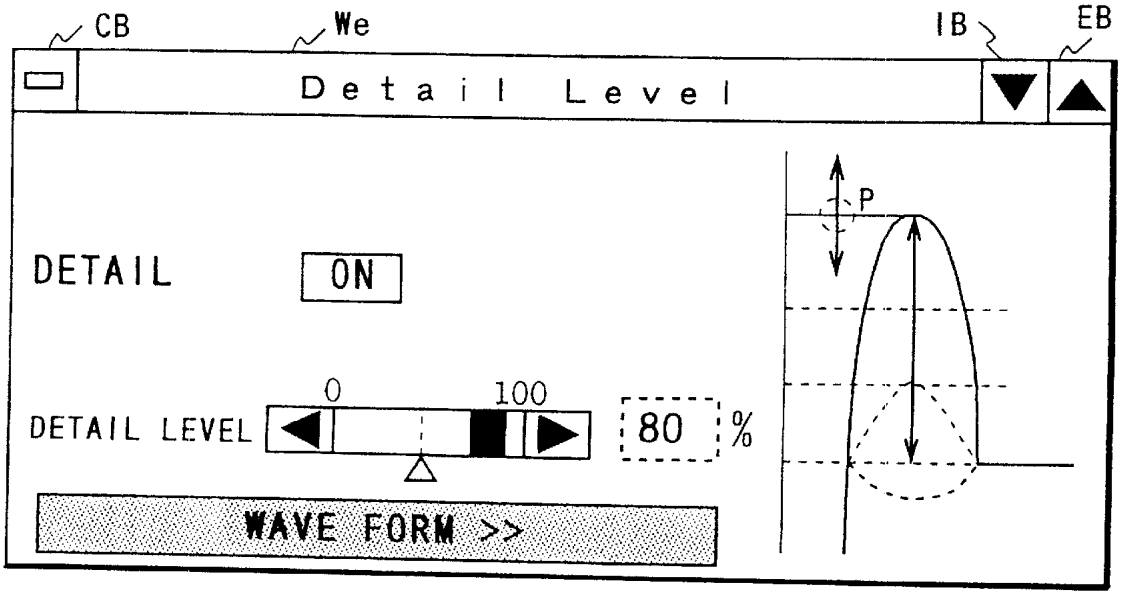


FIG. 39A

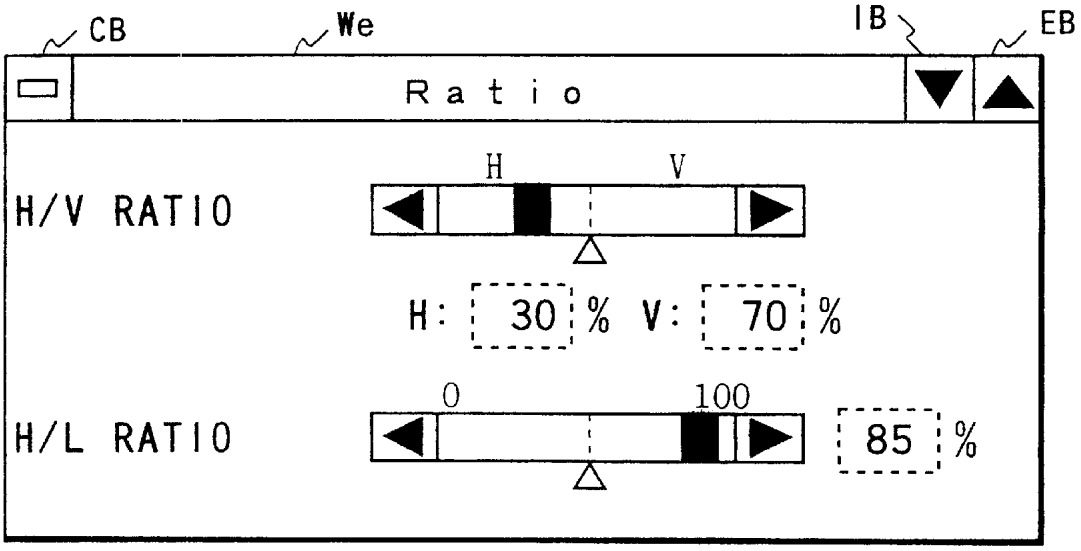


FIG. 39B

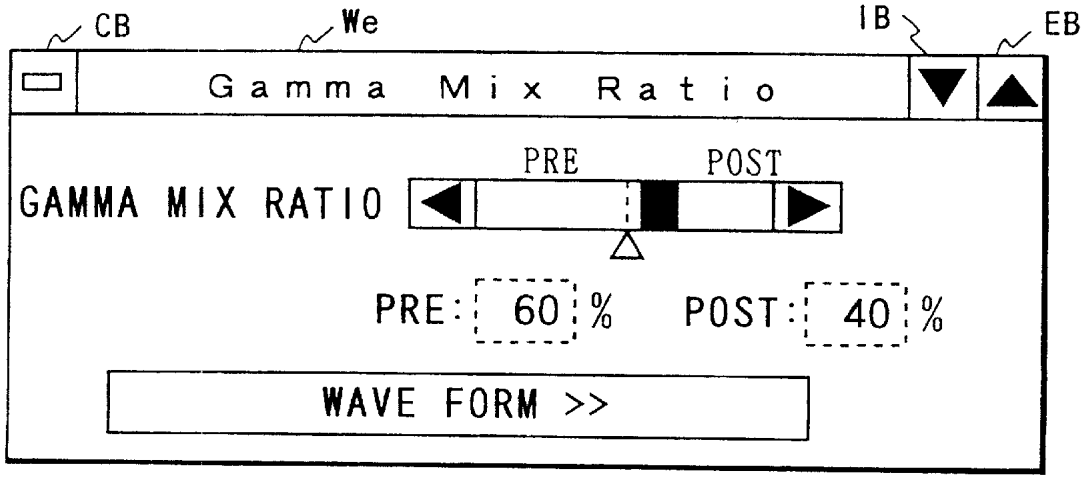


FIG. 40

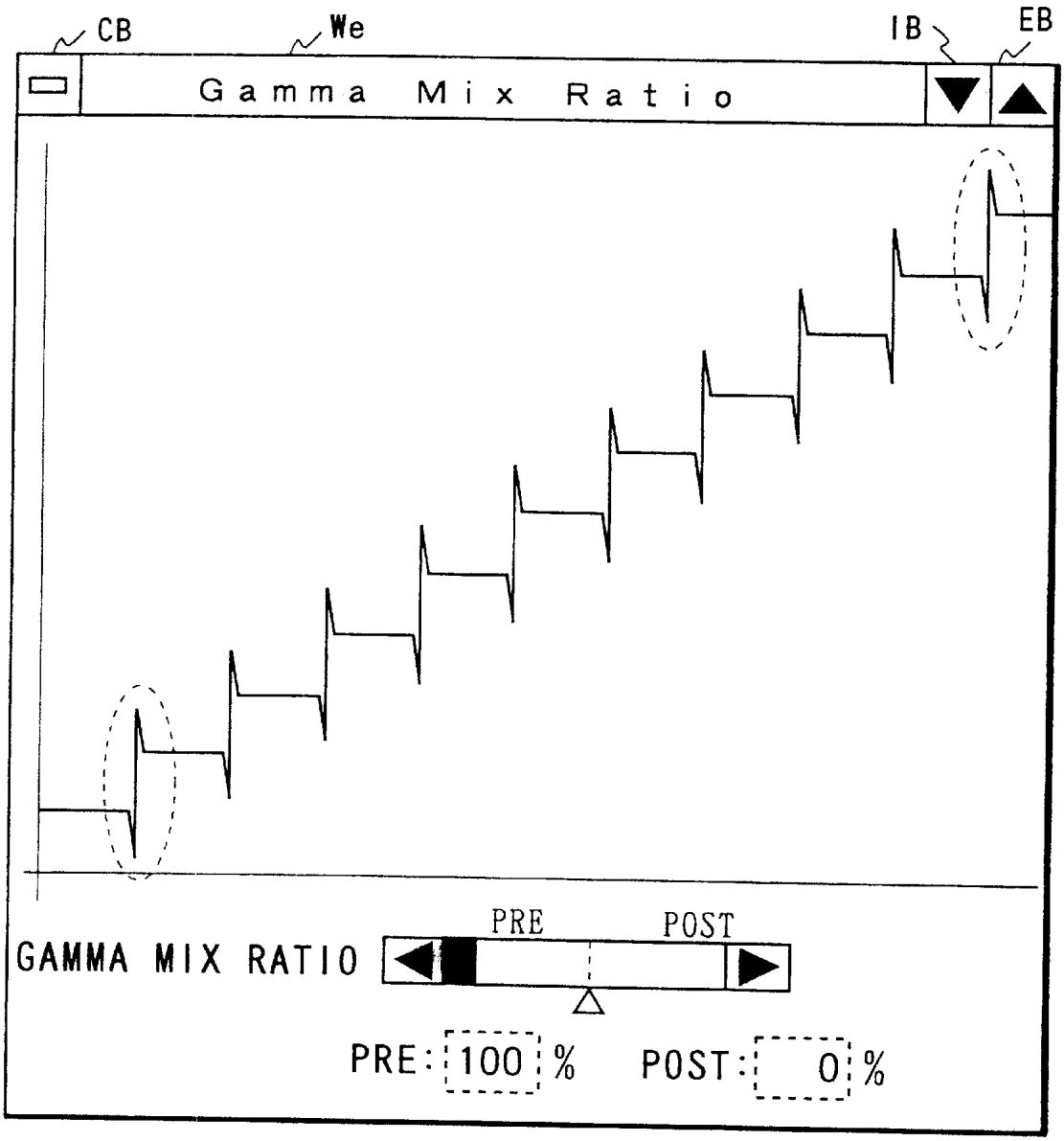

CB
We
IB
EB
Gamma Mix Ratio
PRE
POST
GAMMA MIX RATIO
PRE: 100 %
POST: 0 %

FIG. 41

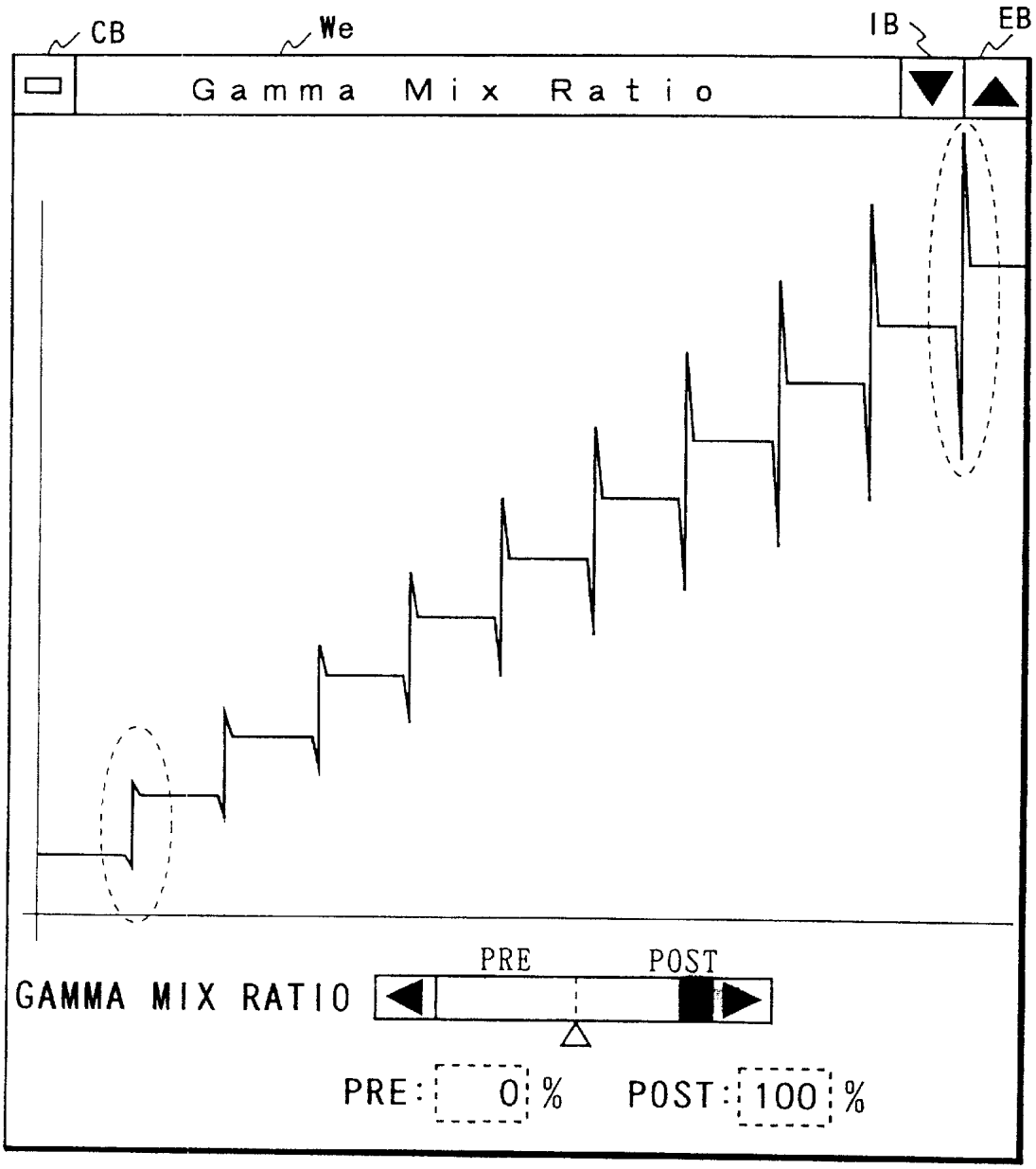

CB
We
IB
EB
Gamma Mix Ratio
PRE
POST
GAMMA MIX RATIO
PRE: 0 %
POST: 100 %

FIG. 42

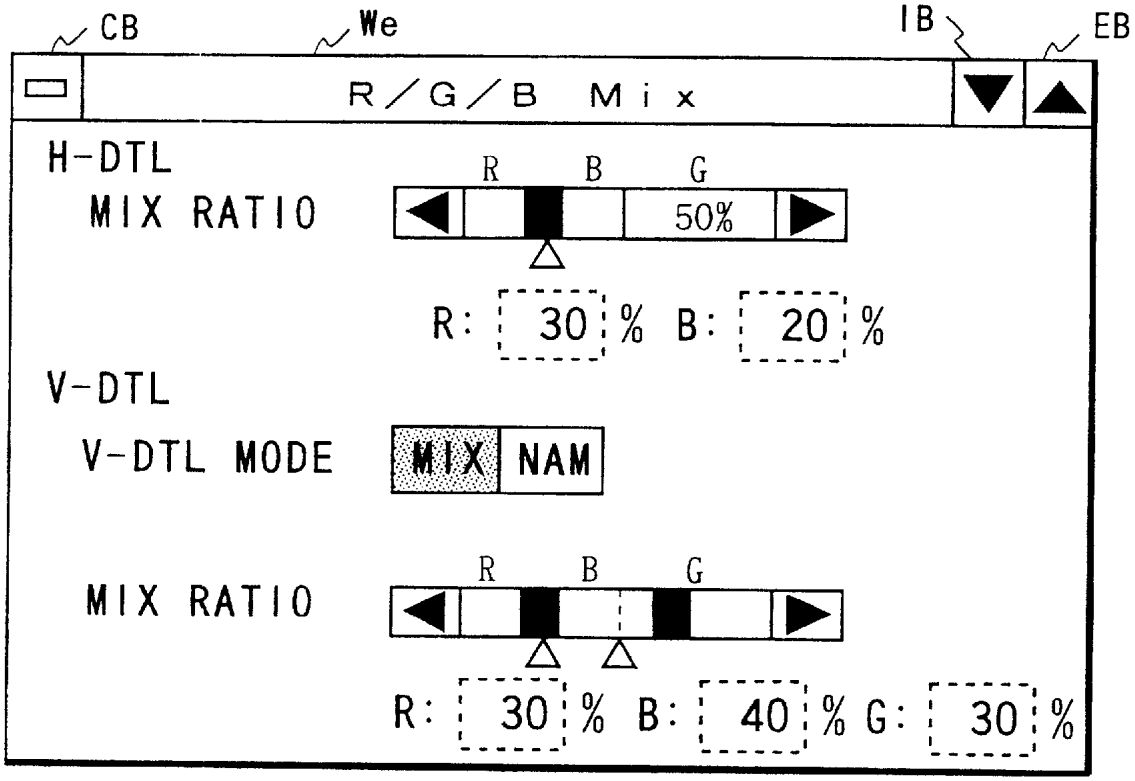

CB
We
IB
EB
R/G/B Mix
H-DTL
MIX RATIO
R
B
G
50%
R: 30 % B: 20 %
V-DTL
V-DTL MODE
MIX
NAM
MIX RATIO
R
B
G
R: 30 % B: 40 % G: 30 %

FIG. 43A

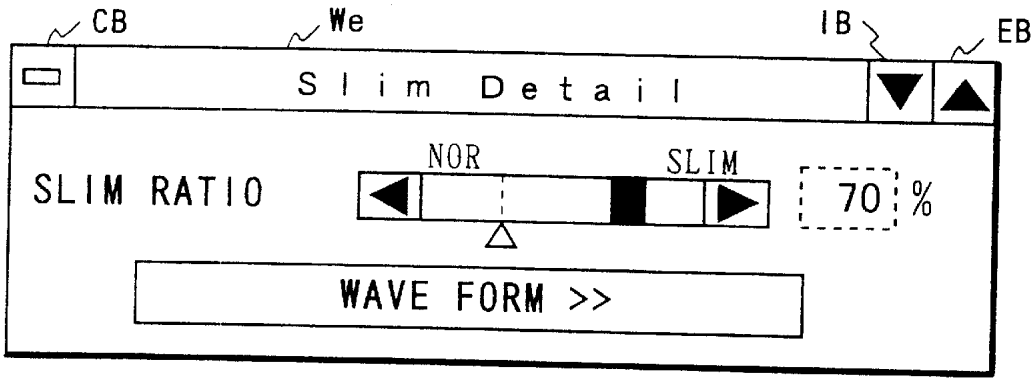


FIG. 43B

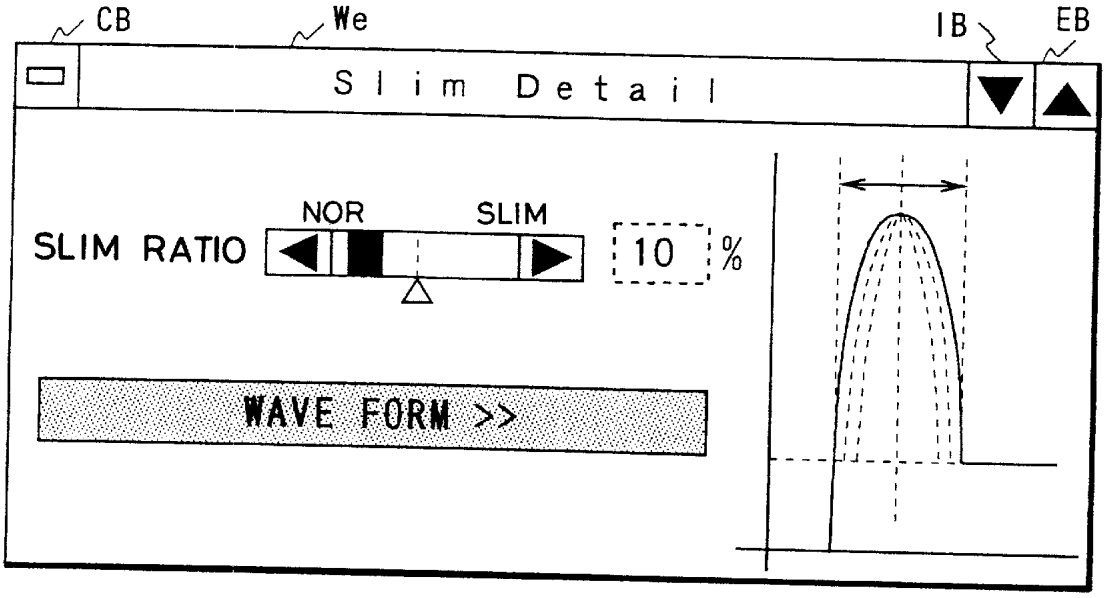


FIG. 43C

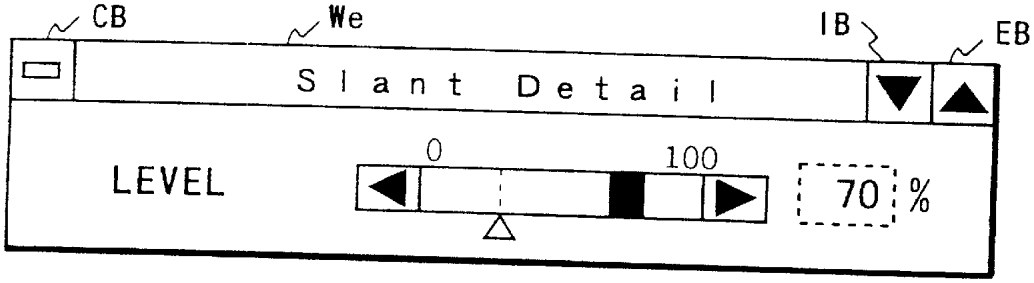


FIG. 44A

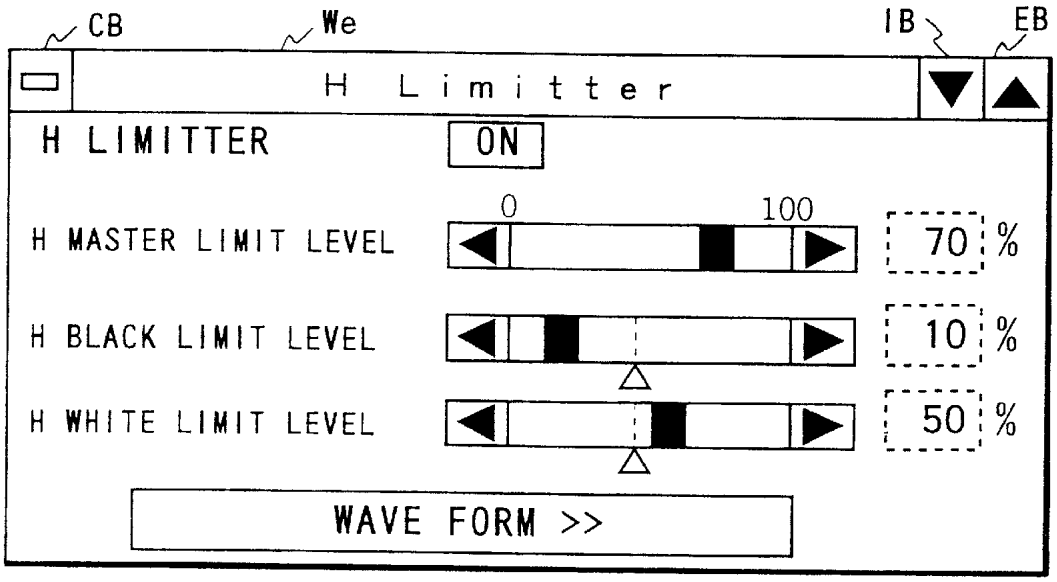


FIG. 44B

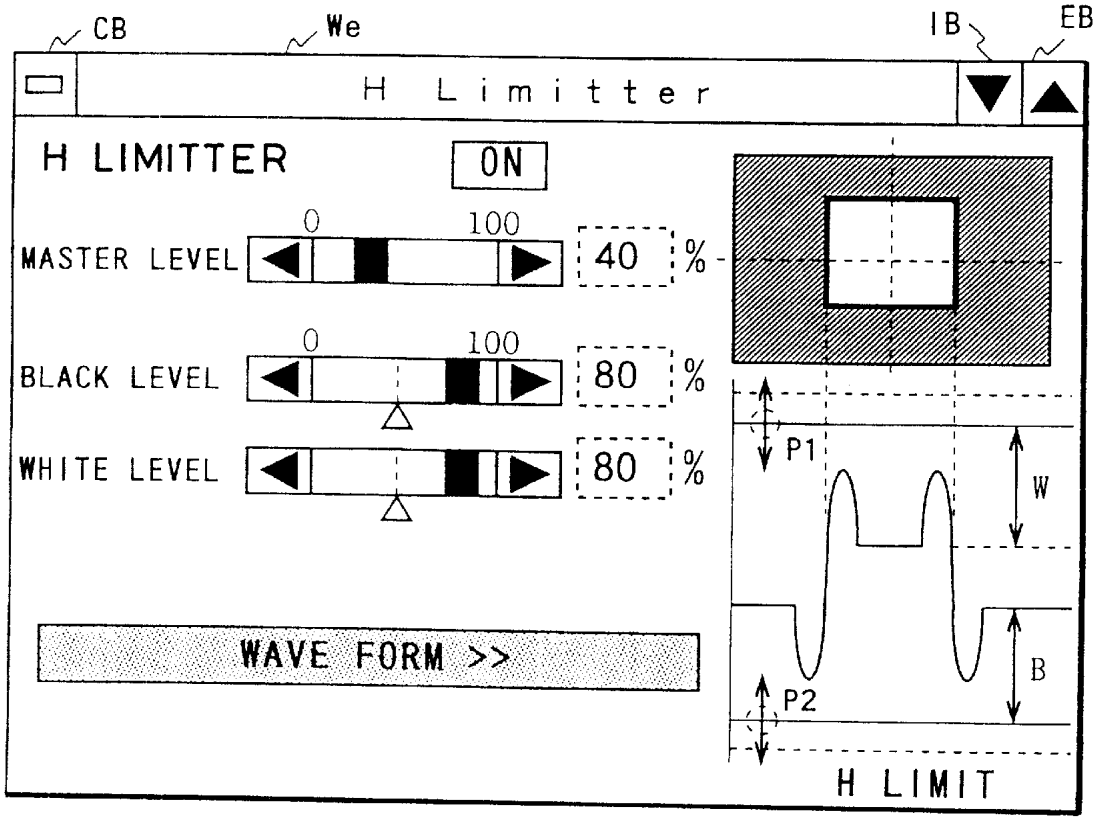


FIG. 45A

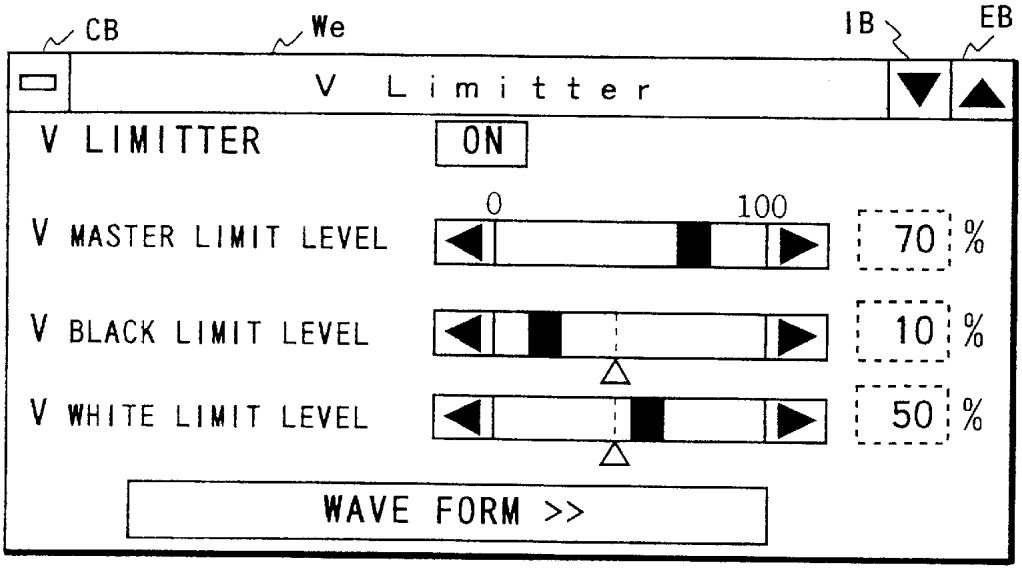


FIG. 45B

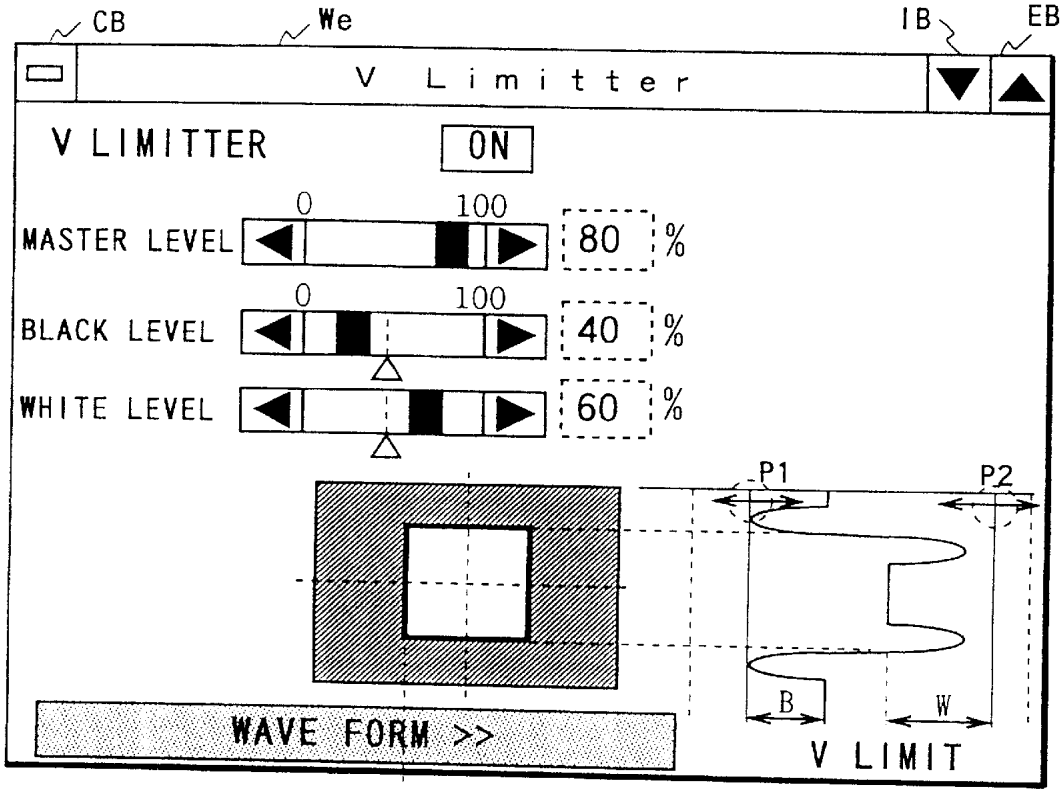


FIG. 46

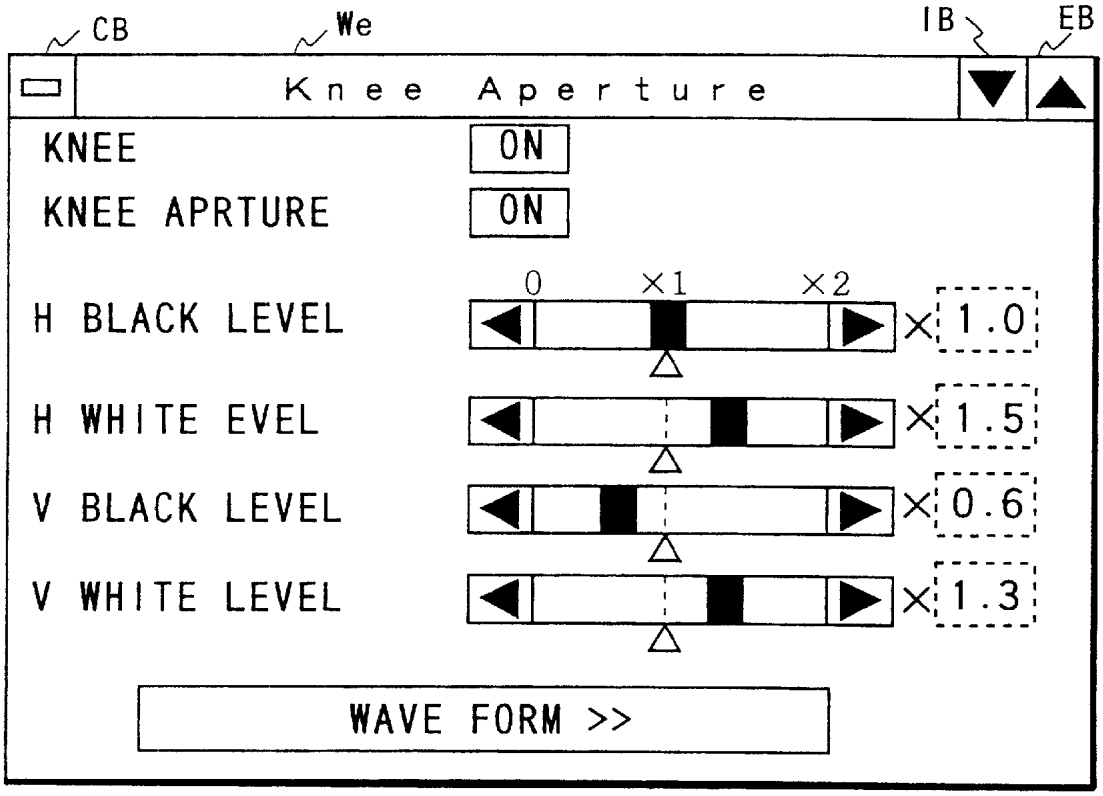

CB
We
IB
EB
Knee Aperture
KNEE
ON
KNEE APRTURE
ON
0
×1
×2
H BLACK LEVEL
×1.0
H WHITE EVEL
×1.5
V BLACK LEVEL
×0.6
V WHITE LEVEL
×1.3
WAVE FORM >>

FIG. 47

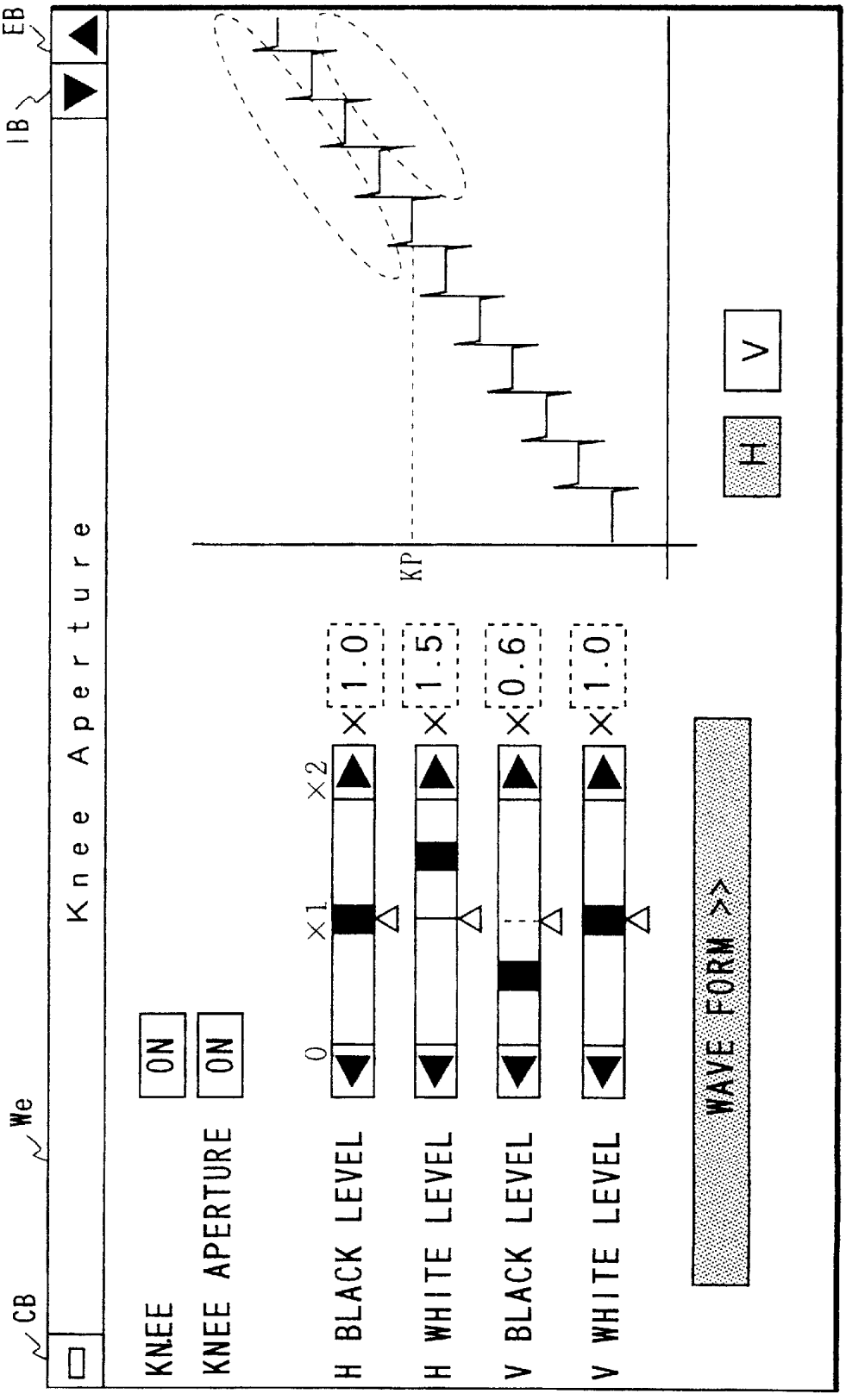

EB
IB
We
CB
Knee Aperture
KP
V
H
KNEE
ON
KNEE APERTURE
ON
H BLACK LEVEL
H WHITE LEVEL
V BLACK LEVEL
V WHITE LEVEL
0
×1
×2
×1.0
×1.5
×0.6
×1.0
WAVE FORM >>

FIG. 48

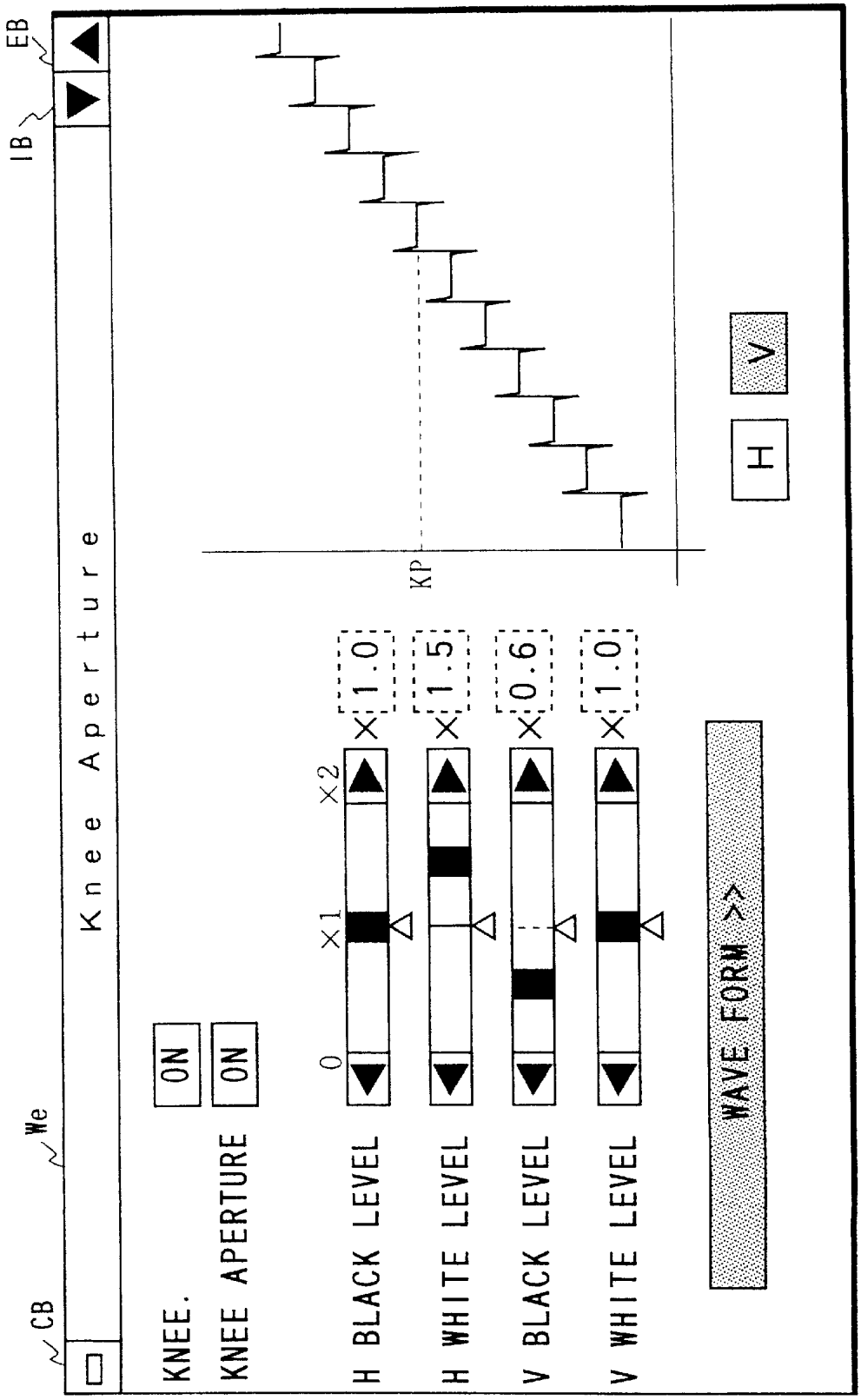

EB
IB
Knee Aperture
CB
We
KNEE.
KNEE APERTURE
ON
ON
0
×1
×2
H BLACK LEVEL
H WHITE LEVEL
V BLACK LEVEL
V WHITE LEVEL
×1.0
×1.5
×0.6
×1.0
KP
H
V
WAVE FORM >>

FIG. 49A

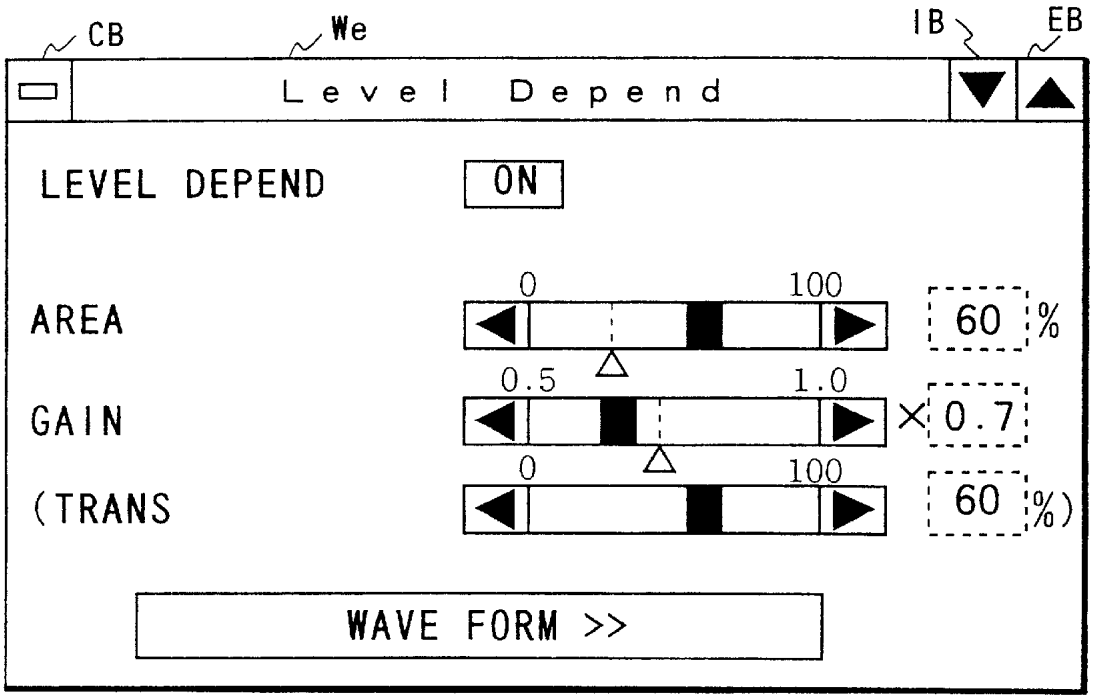


FIG. 49B

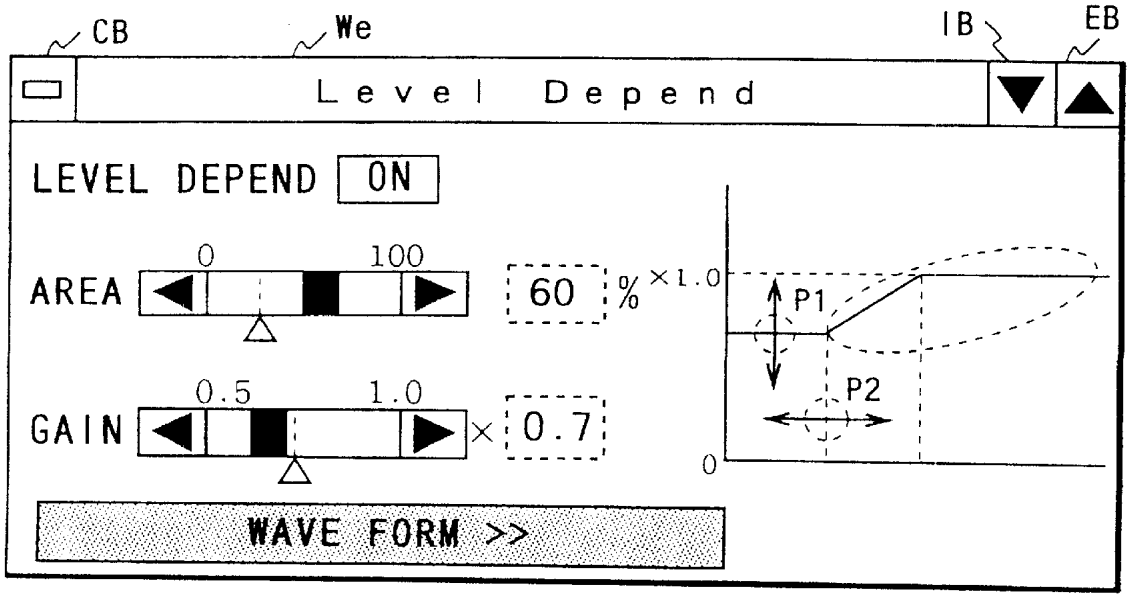


FIG. 50

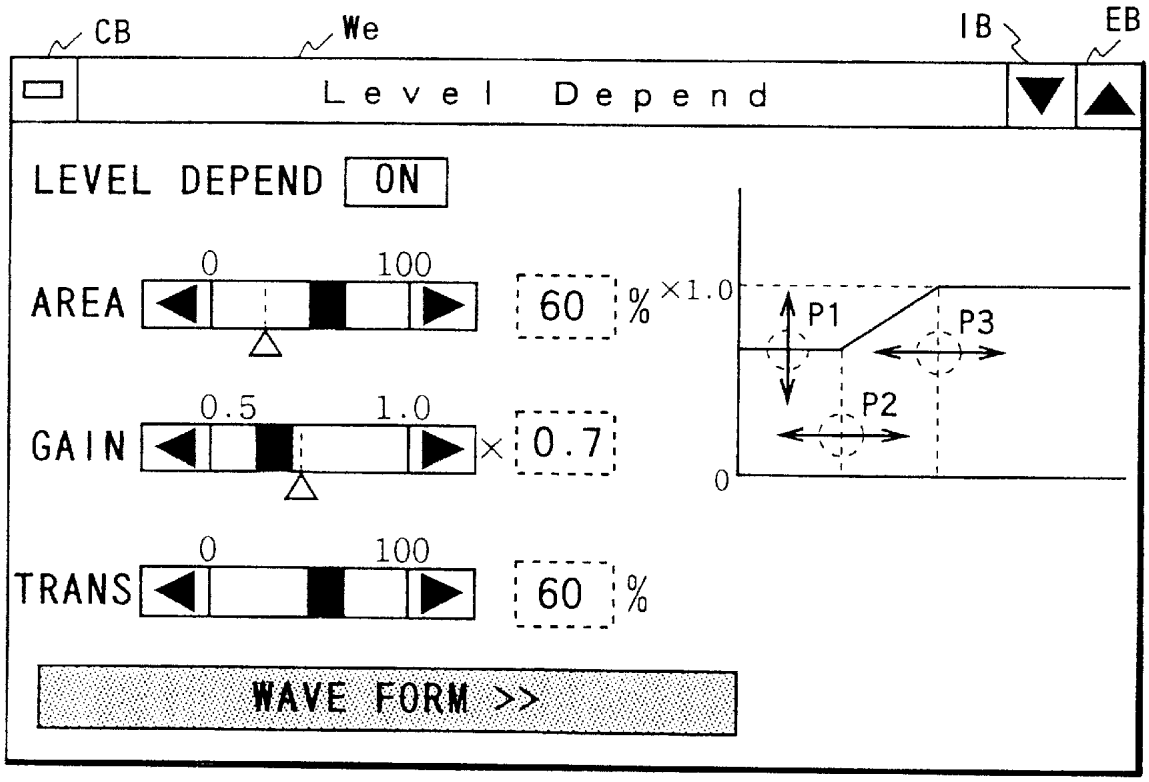

CB
We
IB
EB
Level Depend
LEVEL DEPEND
ON
AREA
0
100
60
%
×1.0
P1
P3
P2
0
GAIN
0.5
1.0
×
0.7
TRANS
0
100
60
%
WAVE FORM >>

FIG. 51A

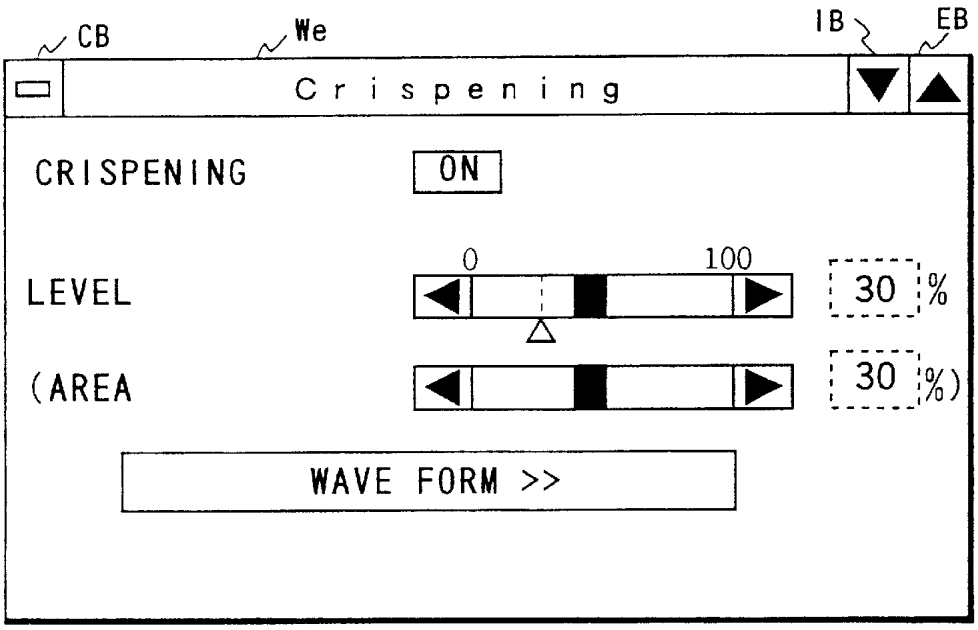


FIG. 51B

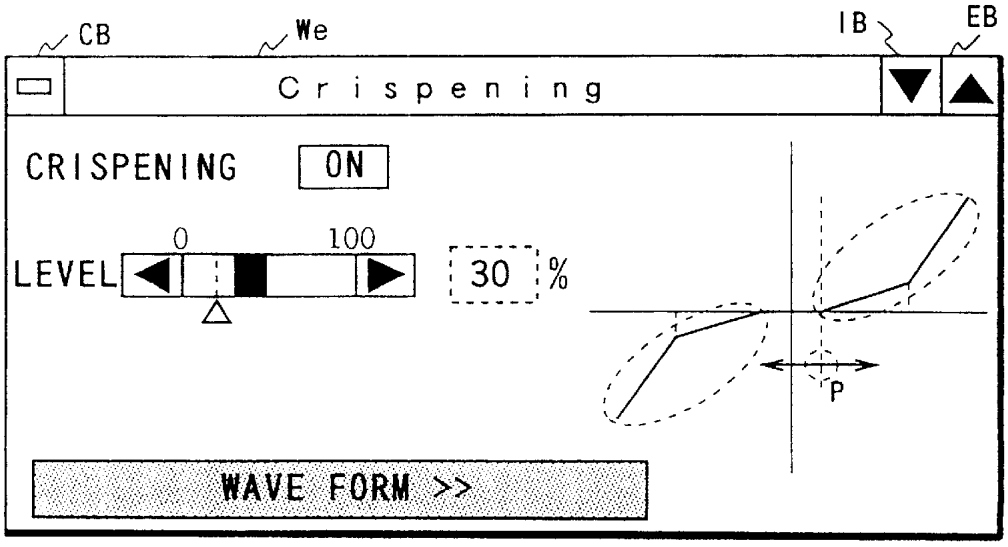


FIG. 52

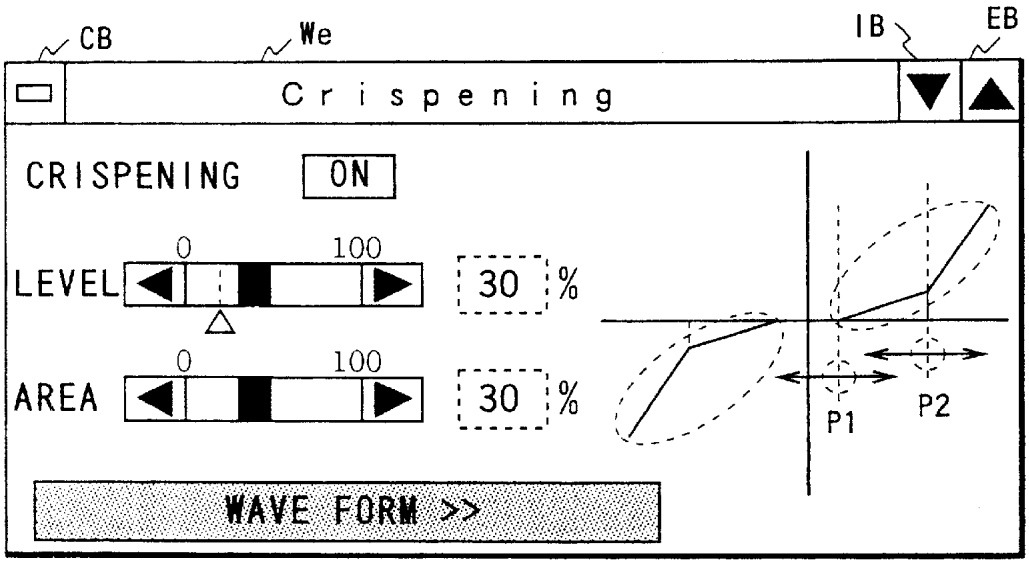

CB
We
IB
EB
Crispening
CRISPENING
ON
LEVEL
0
100
30
%
AREA
0
100
30
%
P1
P2
WAVE FORM >>

FIG. 53

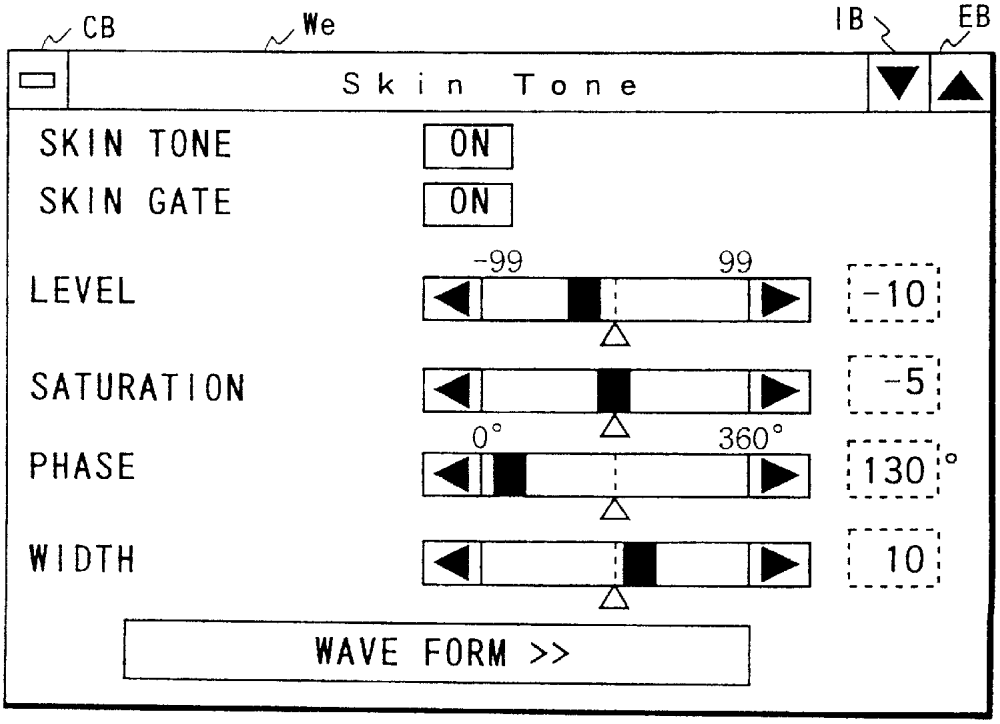

CB
We
IB
EB
Skin Tone
SKIN TONE
ON
SKIN GATE
ON
LEVEL
-99
99
-10
SATURATION
-5
PHASE
0°
360°
130
°
WIDTH
10
WAVE FORM >>

FIG. 54

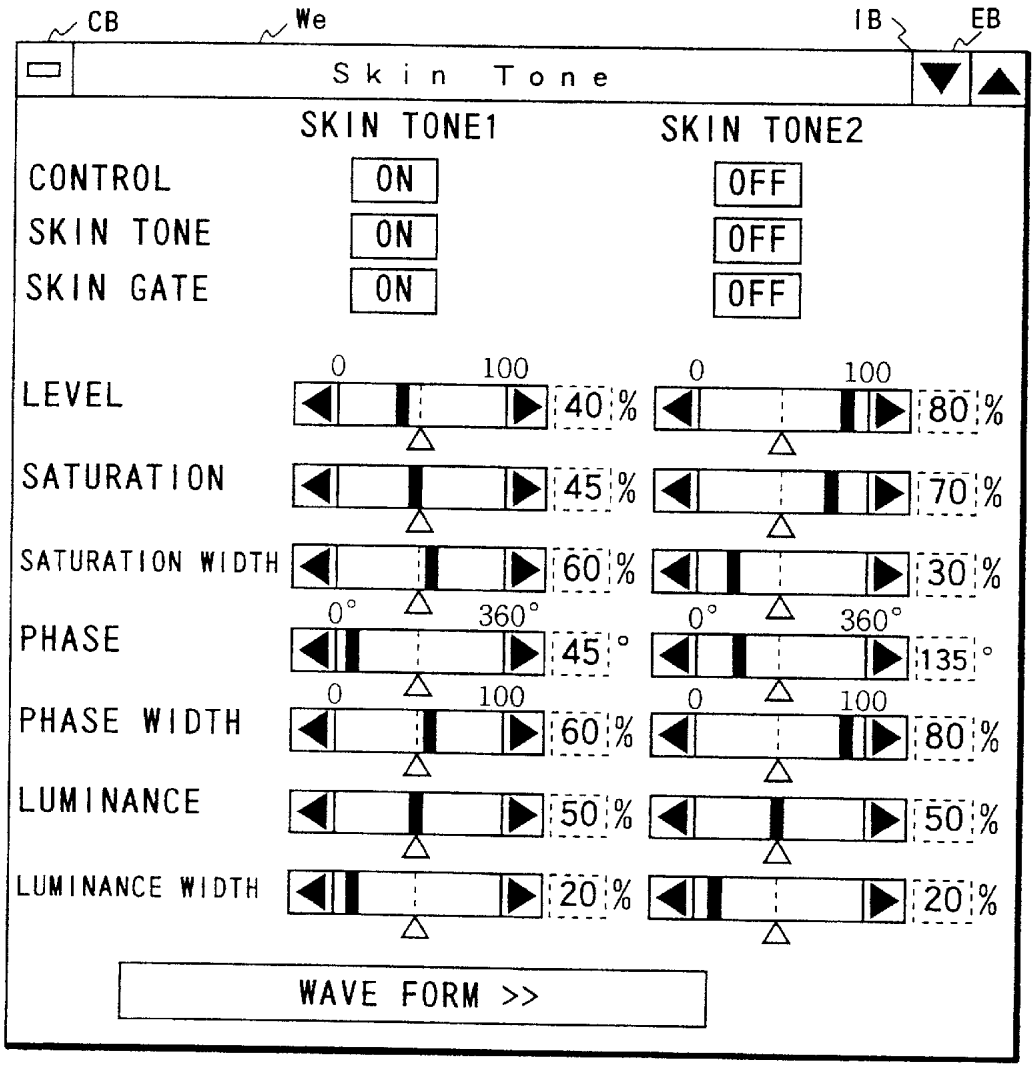

CB
We
IB
EB
Skin Tone
SKIN TONE1
SKIN TONE2
CONTROL
ON
OFF
SKIN TONE
ON
OFF
SKIN GATE
ON
OFF
LEVEL
0
100
40 %
0
100
80 %
SATURATION
45 %
70 %
SATURATION WIDTH
60 %
30 %
PHASE
0°
360°
45 °
0°
360°
135 °
PHASE WIDTH
0
100
60 %
0
100
80 %
LUMINANCE
50 %
50 %
LUMINANCE WIDTH
20 %
20 %
WAVE FORM >>

FIG. 55

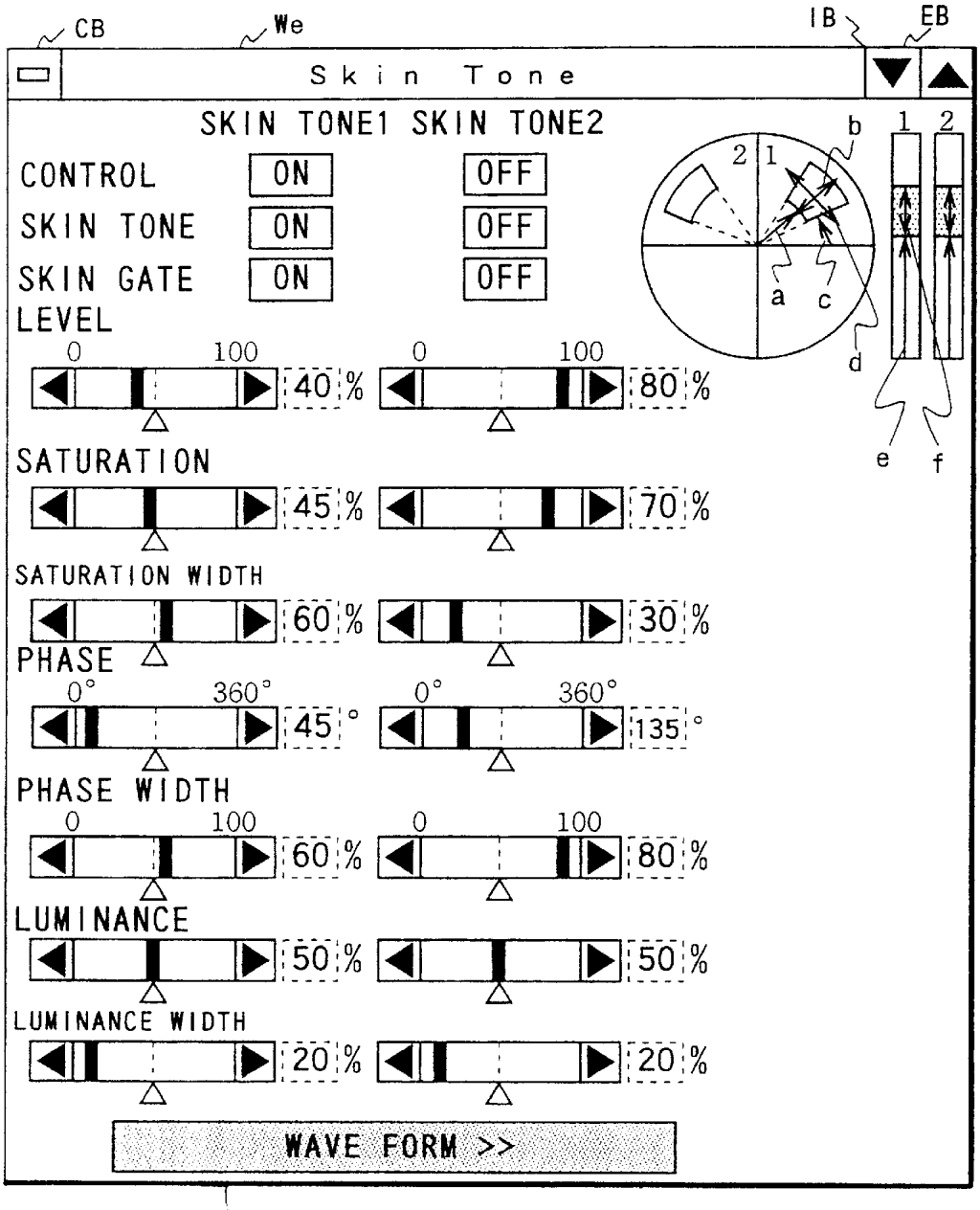

CB
We
IB
EB
Skin Tone
SKIN TONE1 SKIN TONE2
CONTROL
ON
OFF
SKIN TONE
ON
OFF
SKIN GATE
ON
OFF
LEVEL
0
100
40 %
0
100
80 %
SATURATION
45 %
70 %
SATURATION WIDTH
60 %
30 %
PHASE
0°
360°
45 °
0°
360°
135 °
PHASE WIDTH
0
100
60 %
0
100
80 %
LUMINANCE
50 %
50 %
LUMINANCE WIDTH
20 %
20 %
WAVE FORM >>
a
b
c
d
e
f
1
2

FIG. 56

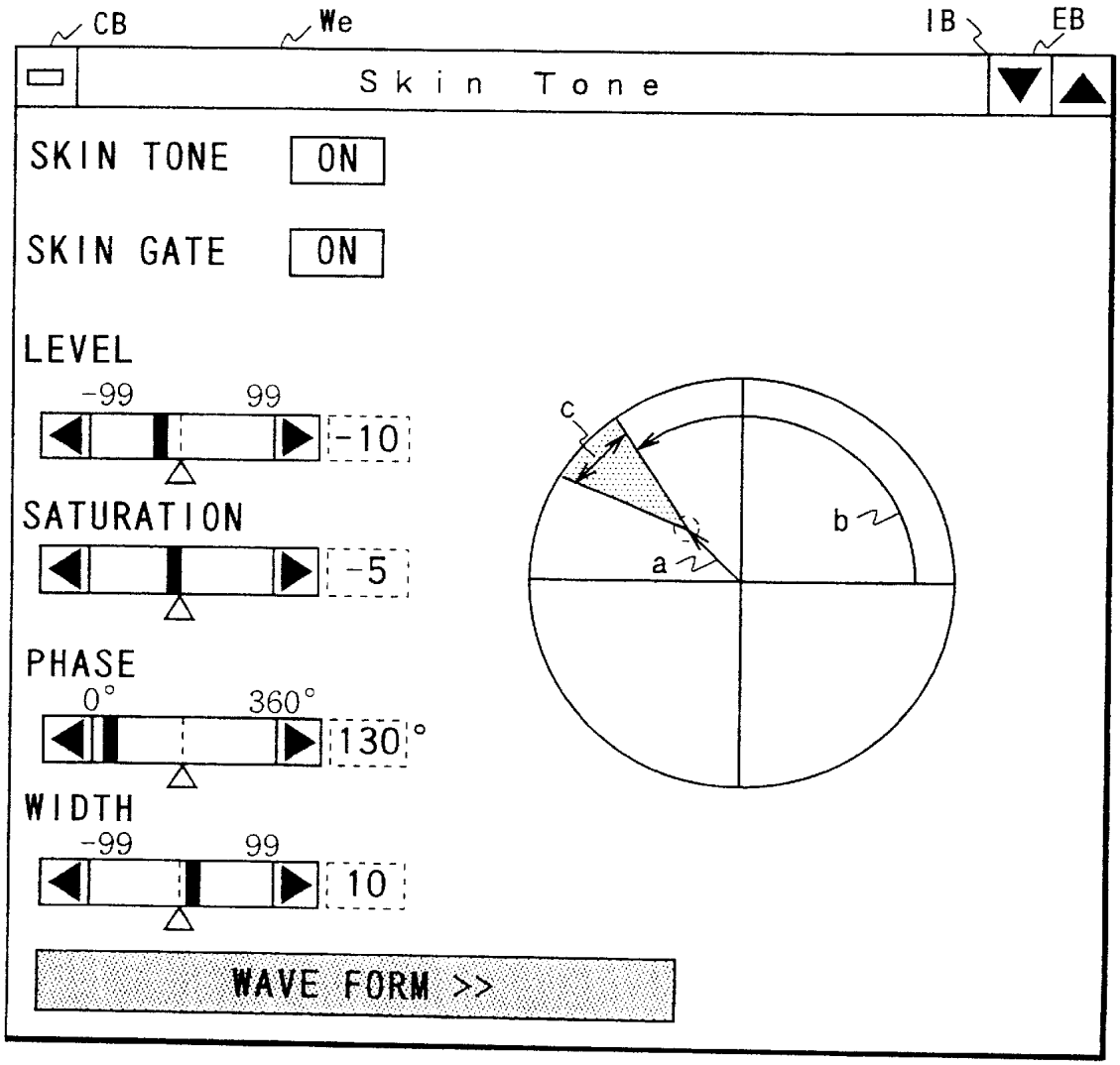

CB
We
IB
EB
Skin Tone
SKIN TONE
ON
SKIN GATE
ON
LEVEL
-99
99
-10
SATURATION
-5
PHASE
0°
360°
130°
WIDTH
-99
99
10
WAVE FORM >>
c
b
a

FIG. 57A

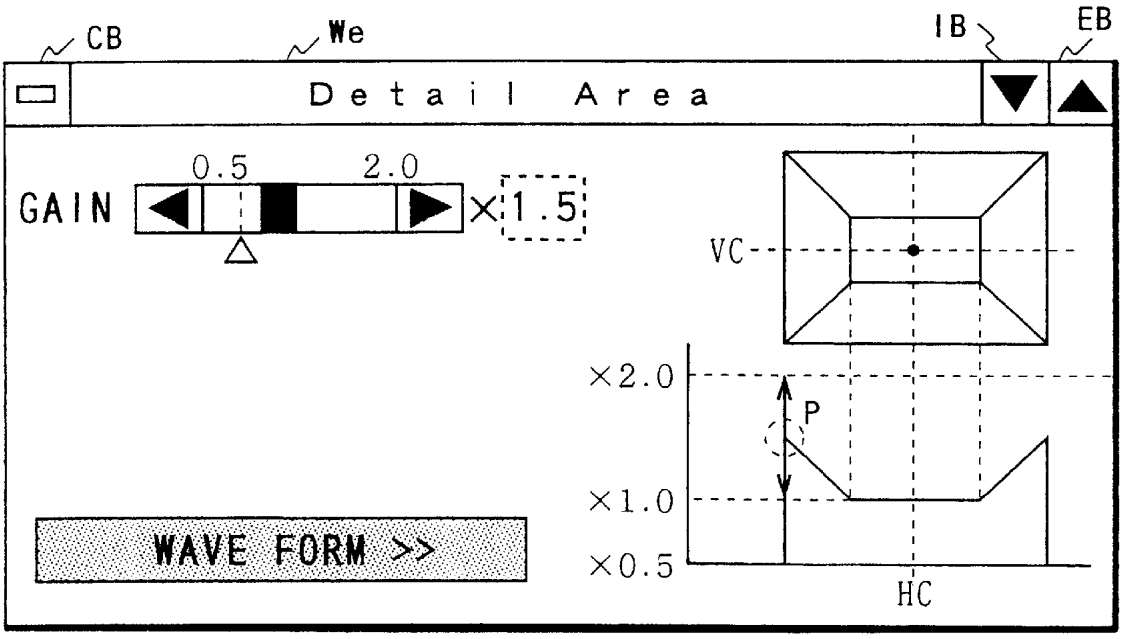


FIG. 57B

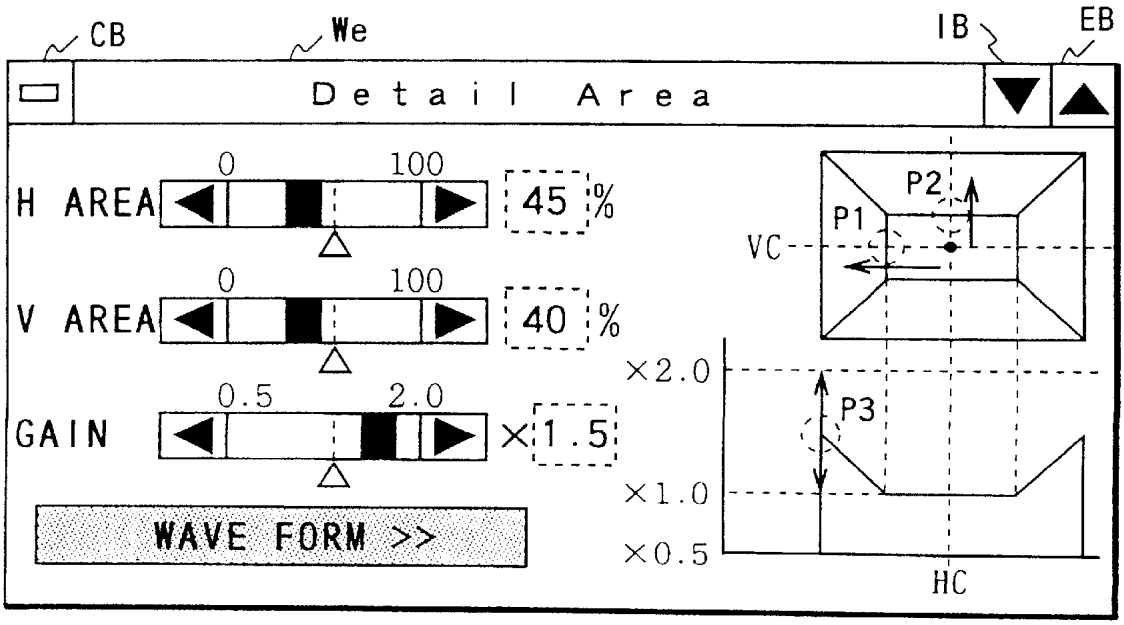


FIG. 58A

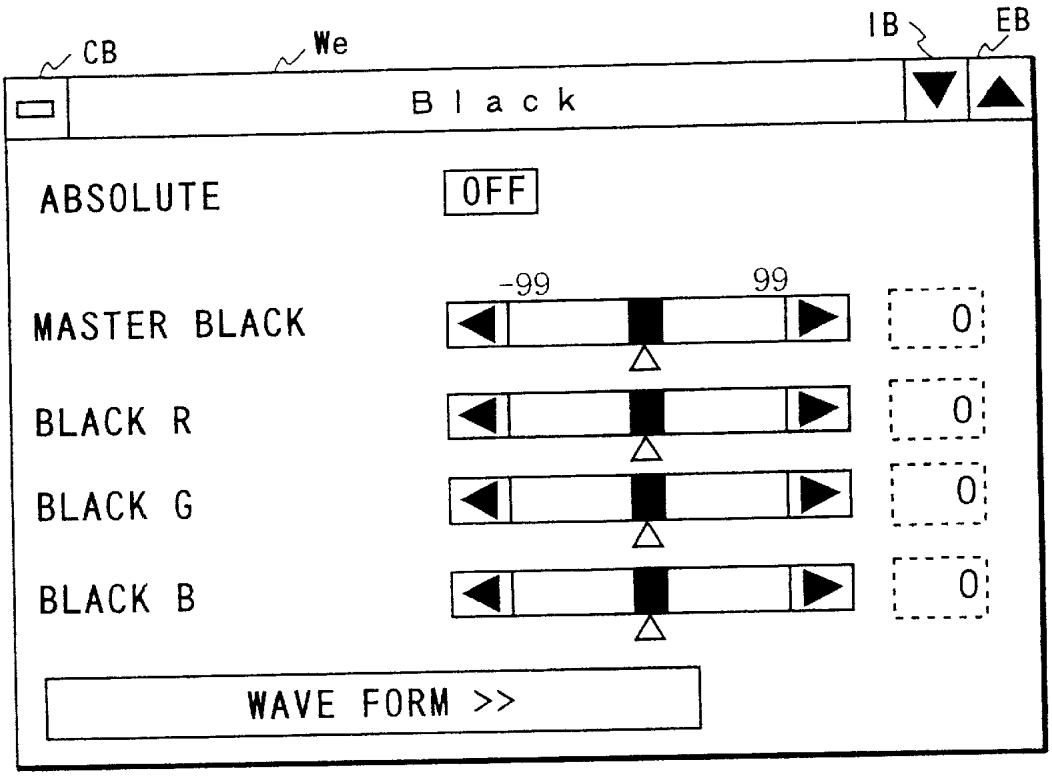


FIG. 58B

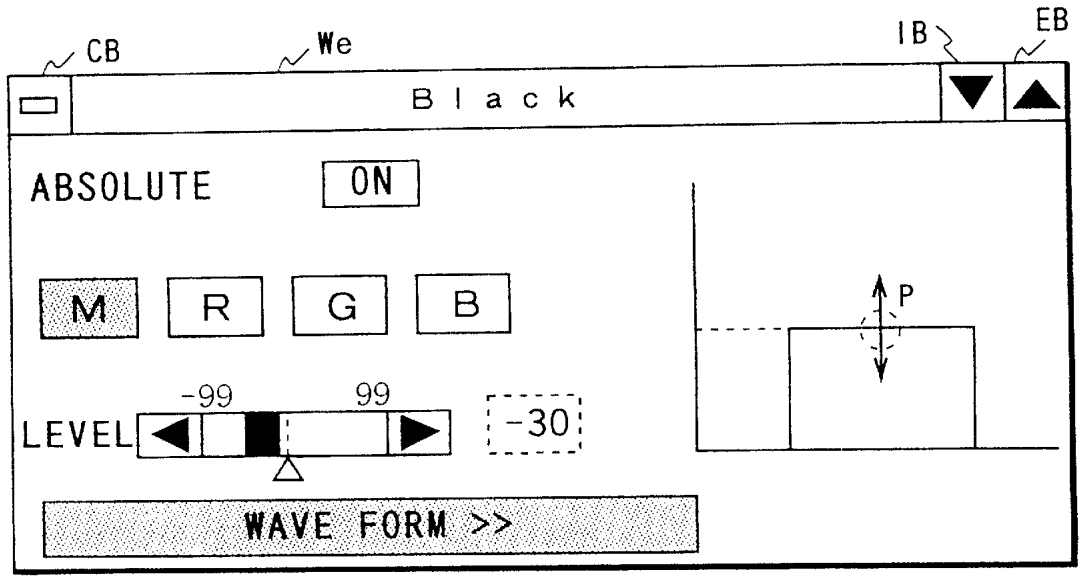


FIG. 59

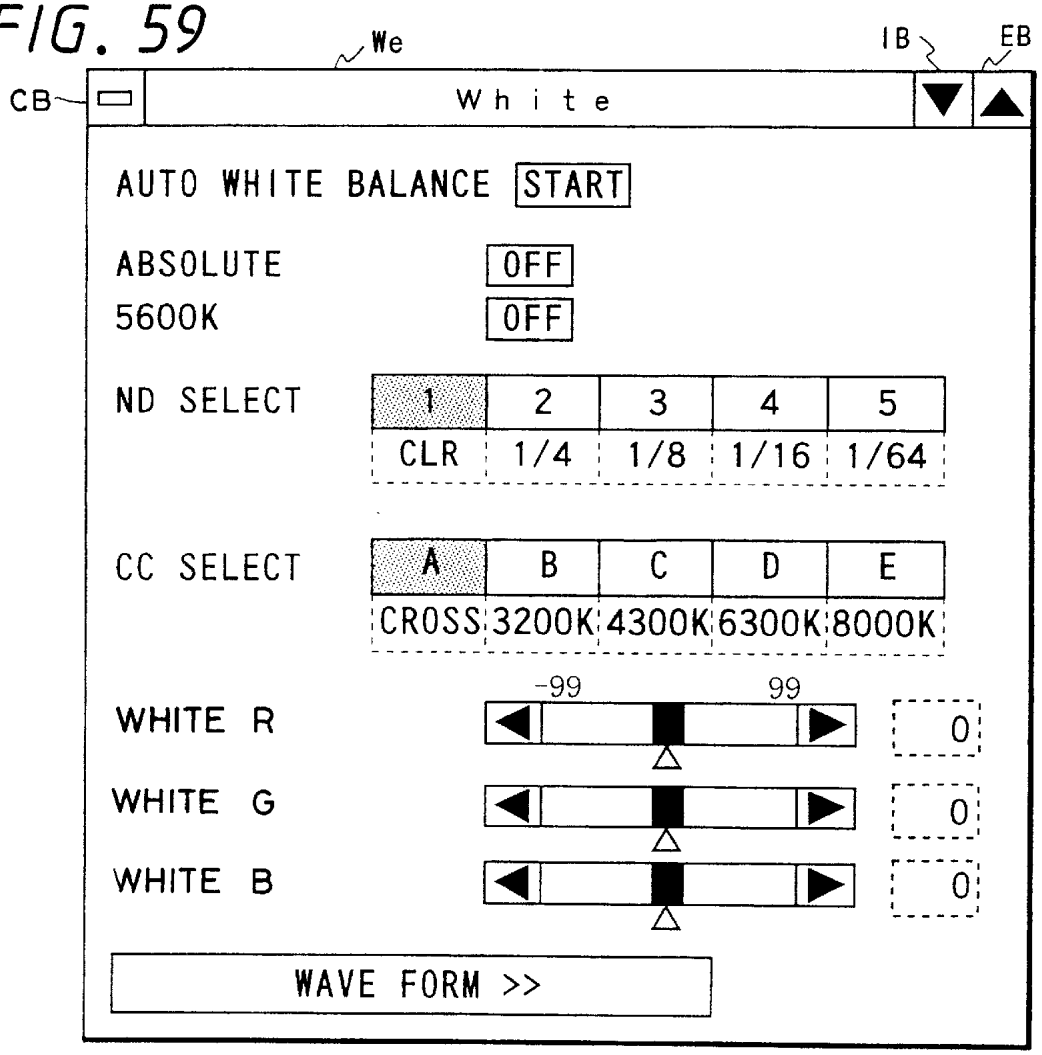

We
IB
EB
CB
White
AUTO WHITE BALANCE
START
ABSOLUTE
OFF
5600K
OFF
ND SELECT
1
2
3
4
5
CLR
1/4
1/8
1/16
1/64
CC SELECT
A
B
C
D
E
CROSS
3200K
4300K
6300K
8000K
-99
99
WHITE R
0
WHITE G
0
WHITE B
0
WAVE FORM >>

FIG. 60

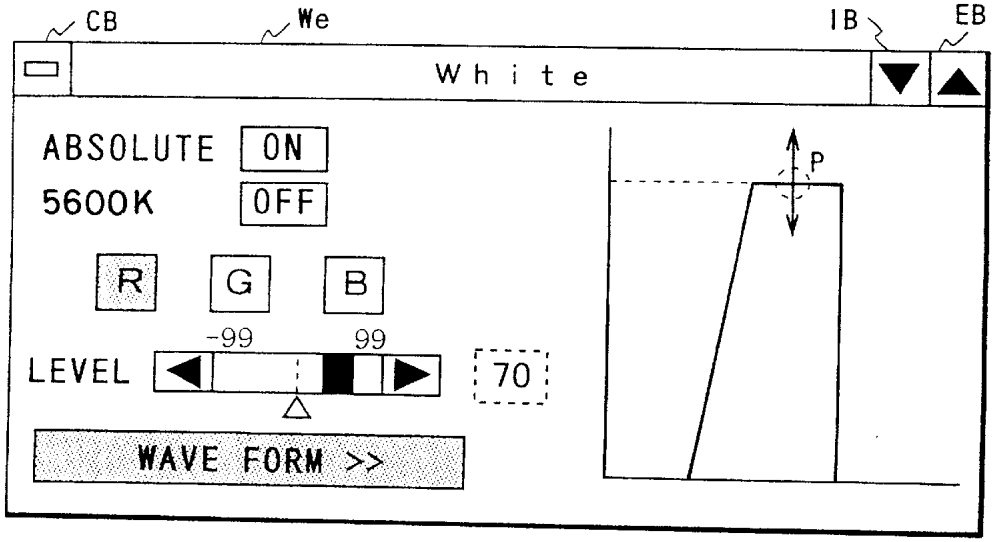

CB
We
IB
EB
White
ABSOLUTE
ON
5600K
OFF
R
G
B
-99
99
LEVEL
70
WAVE FORM >>
P

FIG. 61

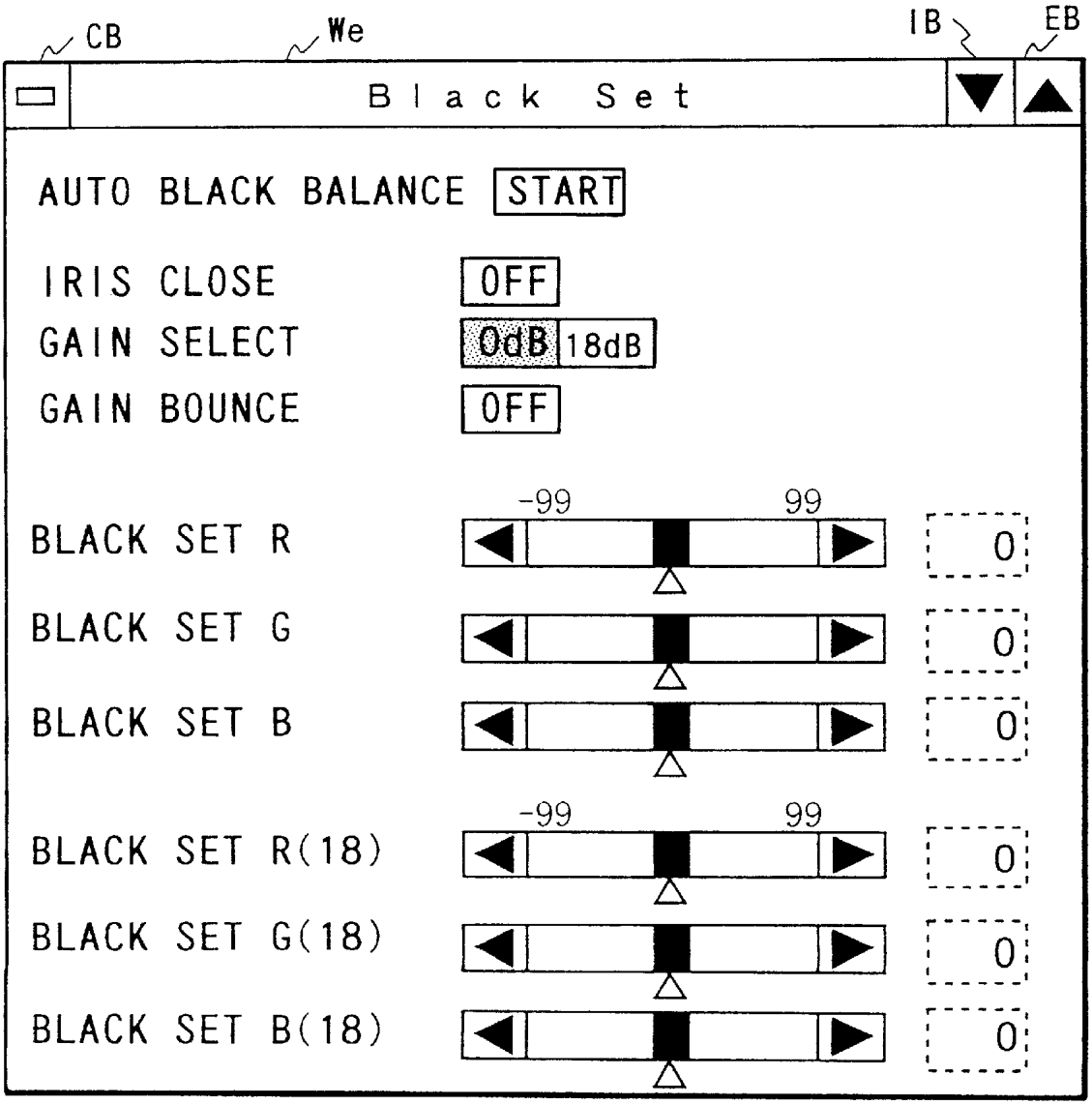

CB
We
IB
EB
Black Set
AUTO BLACK BALANCE
START
IRIS CLOSE
OFF
GAIN SELECT
0dB
18dB
GAIN BOUNCE
OFF
-99
99
BLACK SET R
0
BLACK SET G
0
BLACK SET B
0
-99
99
BLACK SET R(18)
0
BLACK SET G(18)
0
BLACK SET B(18)
0

FIG. 62

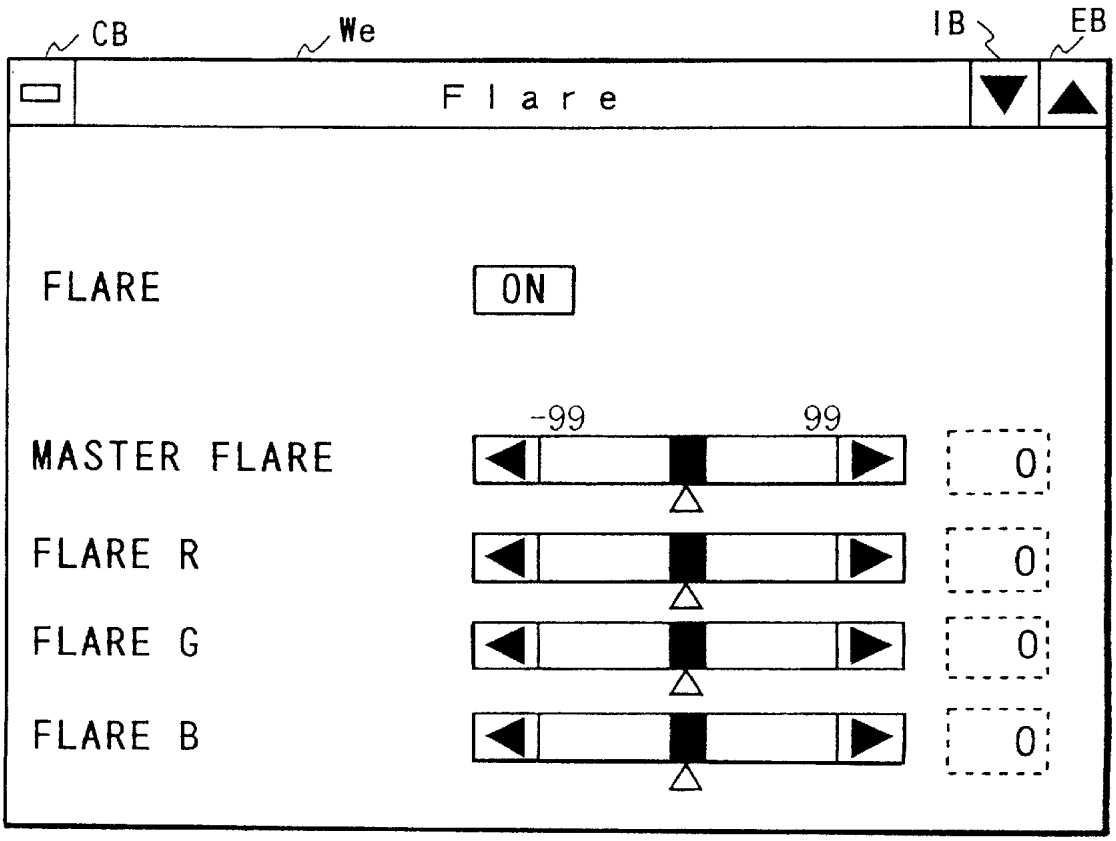

CB
We
IB
EB
Flare
FLARE
ON
-99
99
MASTER FLARE
0
FLARE R
0
FLARE G
0
FLARE B
0

FIG. 63

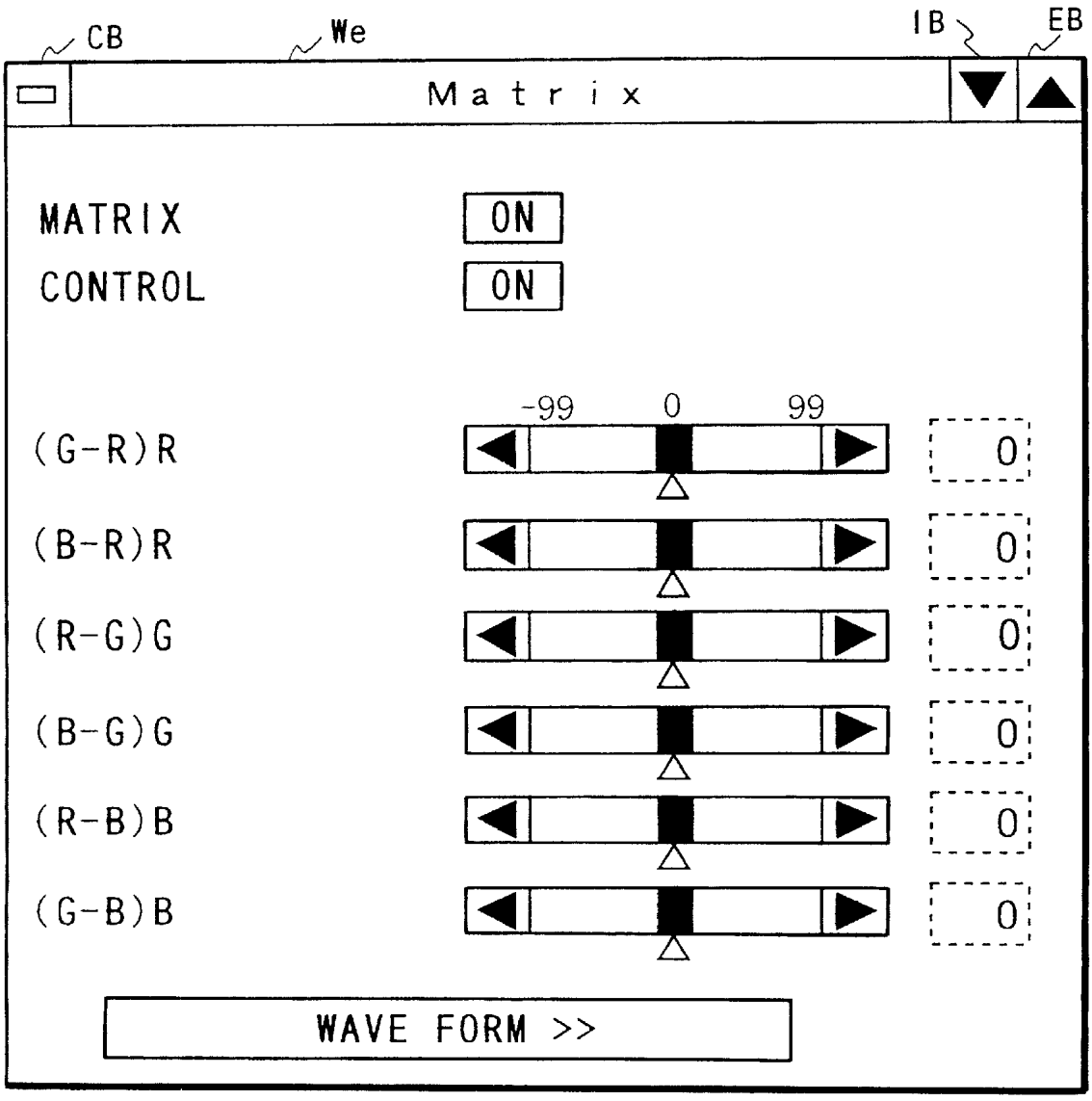

CB
We
IB
EB
Matrix
MATRIX
ON
CONTROL
ON
-99
0
99
(G-R)R
0
(B-R)R
0
(R-G)G
0
(B-G)G
0
(R-B)B
0
(G-B)B
0
WAVE FORM >>

FIG. 64

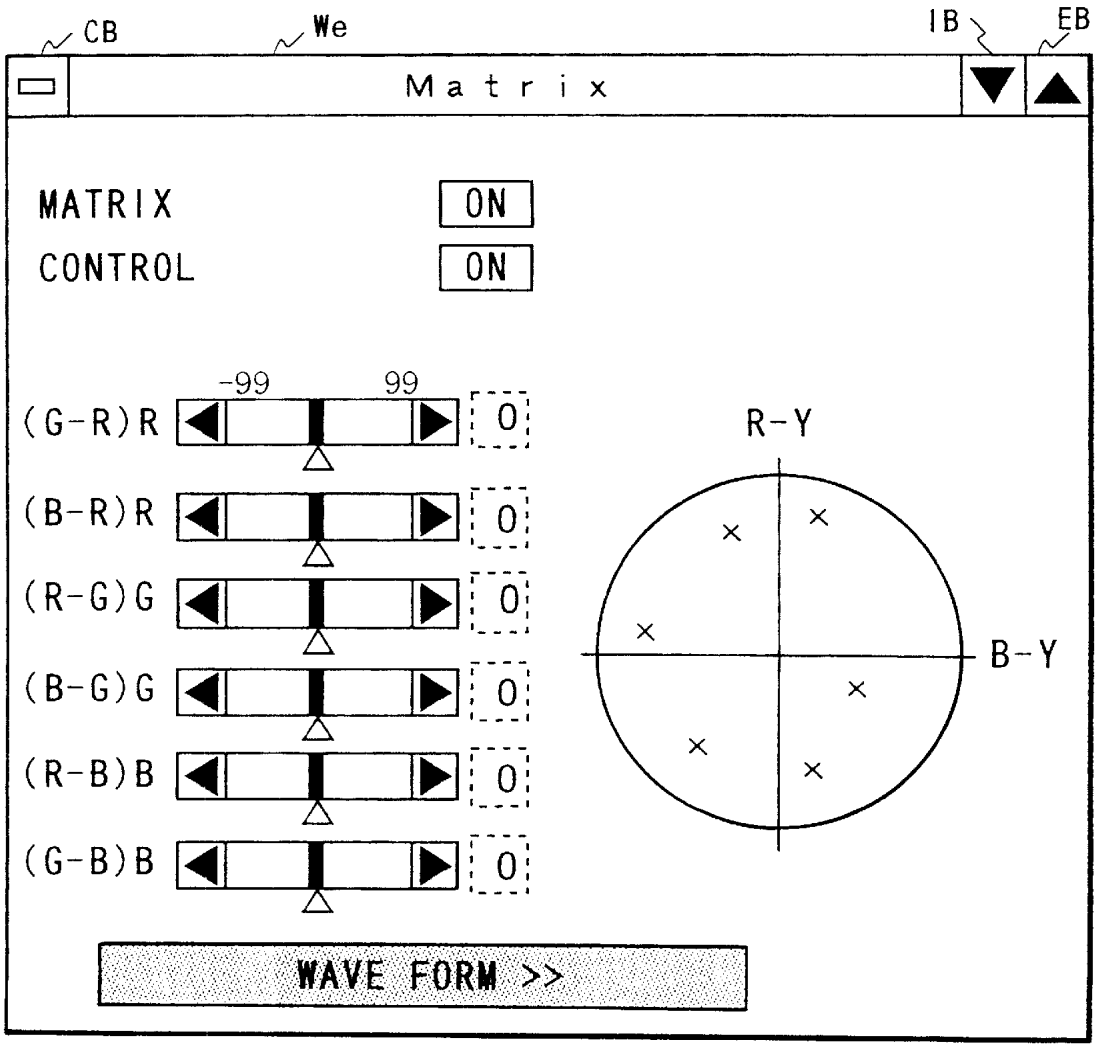

CB
We
IB
EB
Matrix
MATRIX
ON
CONTROL
ON
-99
99
(G-R)R
0
(B-R)R
0
(R-G)G
0
(B-G)G
0
(R-B)B
0
(G-B)B
0
R-Y
B-Y
WAVE FORM >>

FIG. 65A

	Gray	Yellow	Cyan	Green	Magenta	Red	Blue	Black
R	1	1	0	0	1	1	0	0
G	1	1	1	1	0	0	0	0
B	1	0	1	0	1	0	1	0
Y	1.000	0.886	0.701	0.587	0.413	0.299	0.114	0
R − Y	0	0.114	−0.701	−0.587	0.587	0.701	−0.114	0
B − Y	0	−0.886	0.209	−0.587	0.587	−0.299	0.886	0

FIG. 65B

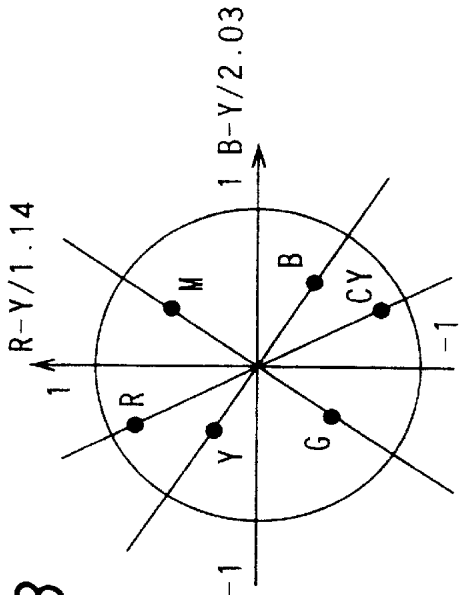


FIG. 66A

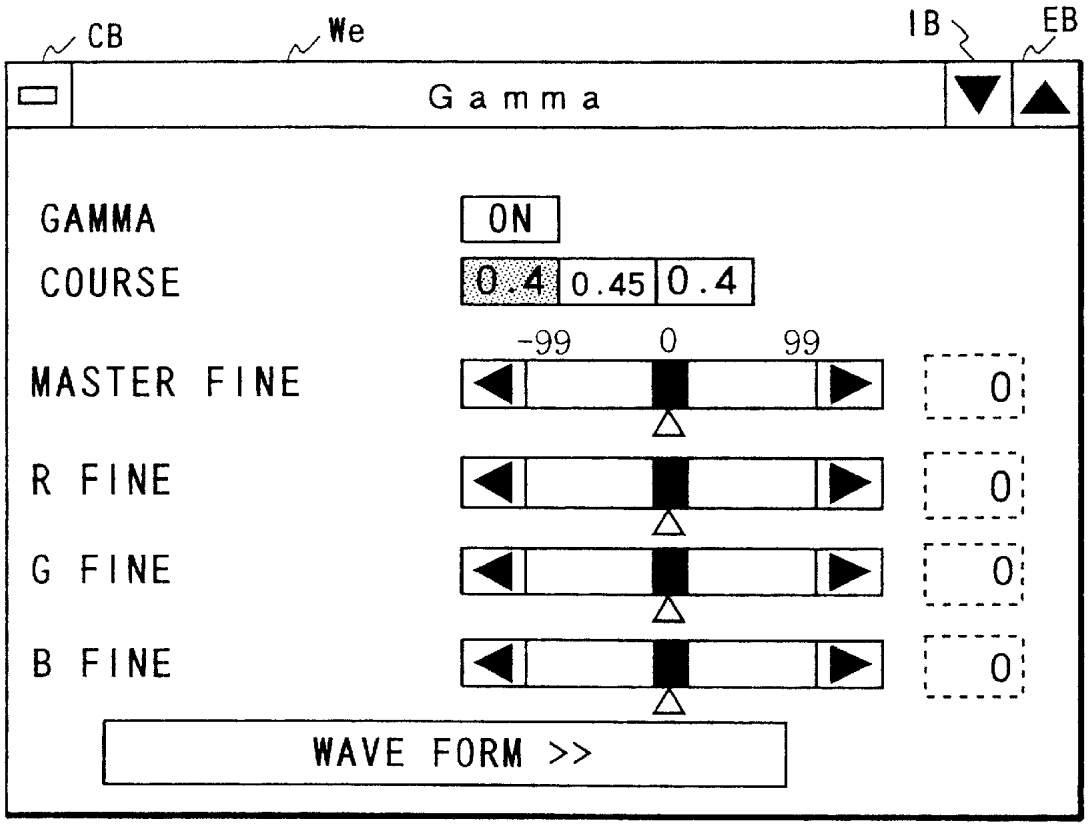


FIG. 66B

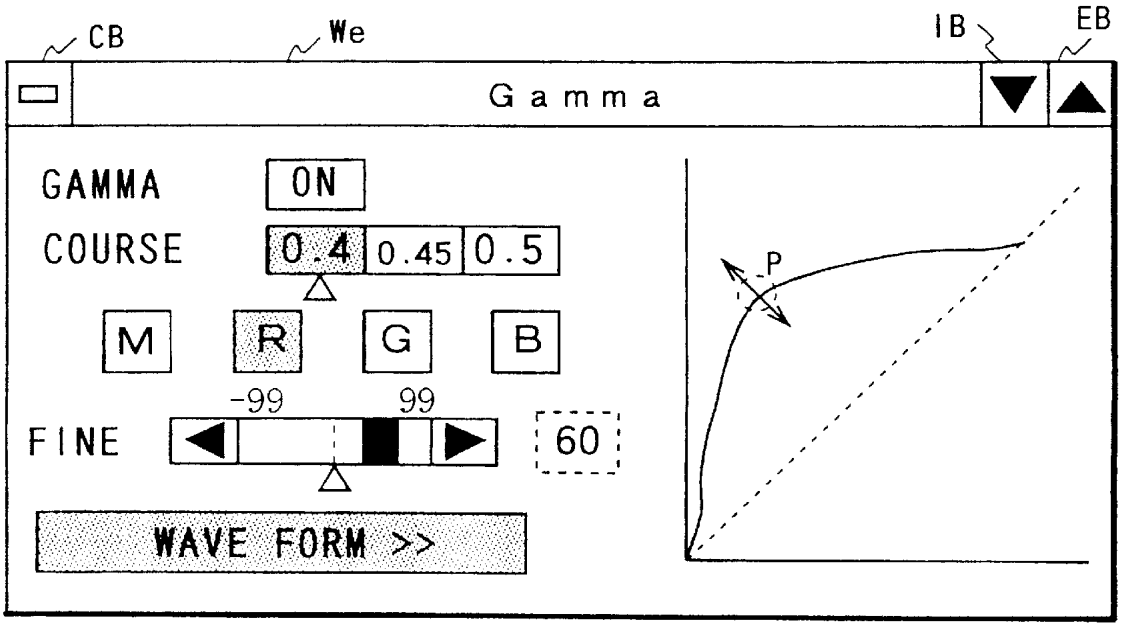


FIG. 67A

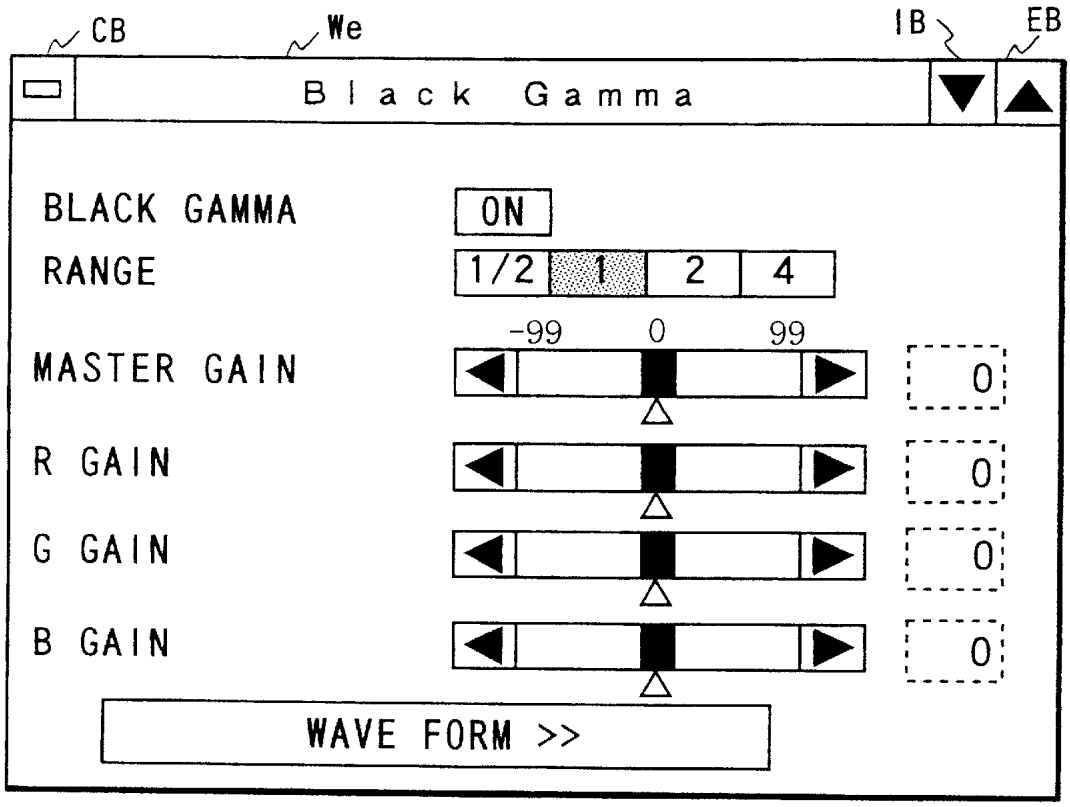


FIG. 67B

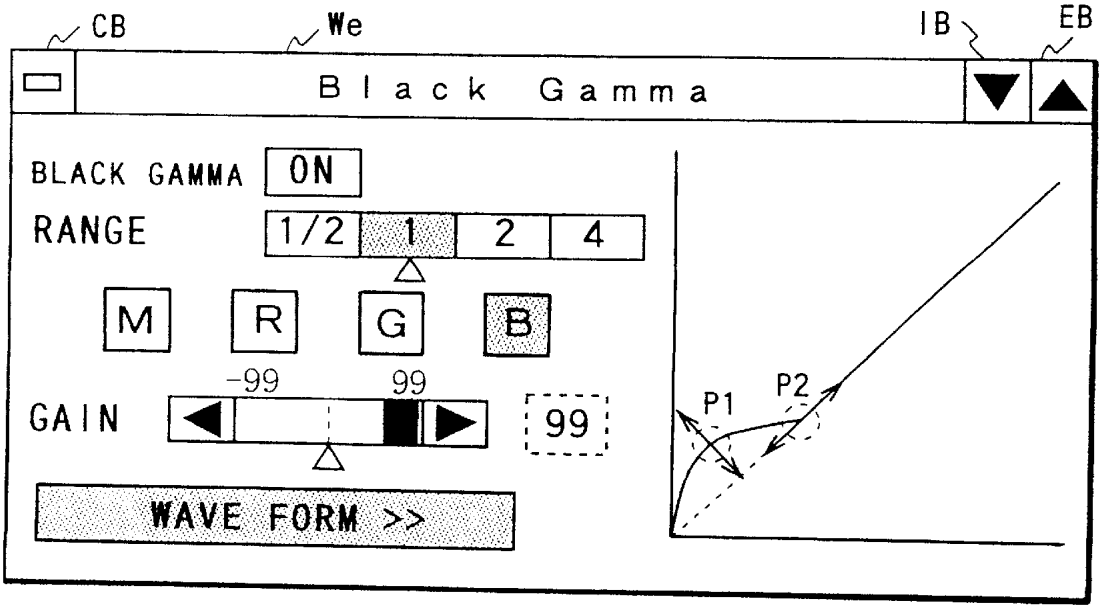


FIG. 68

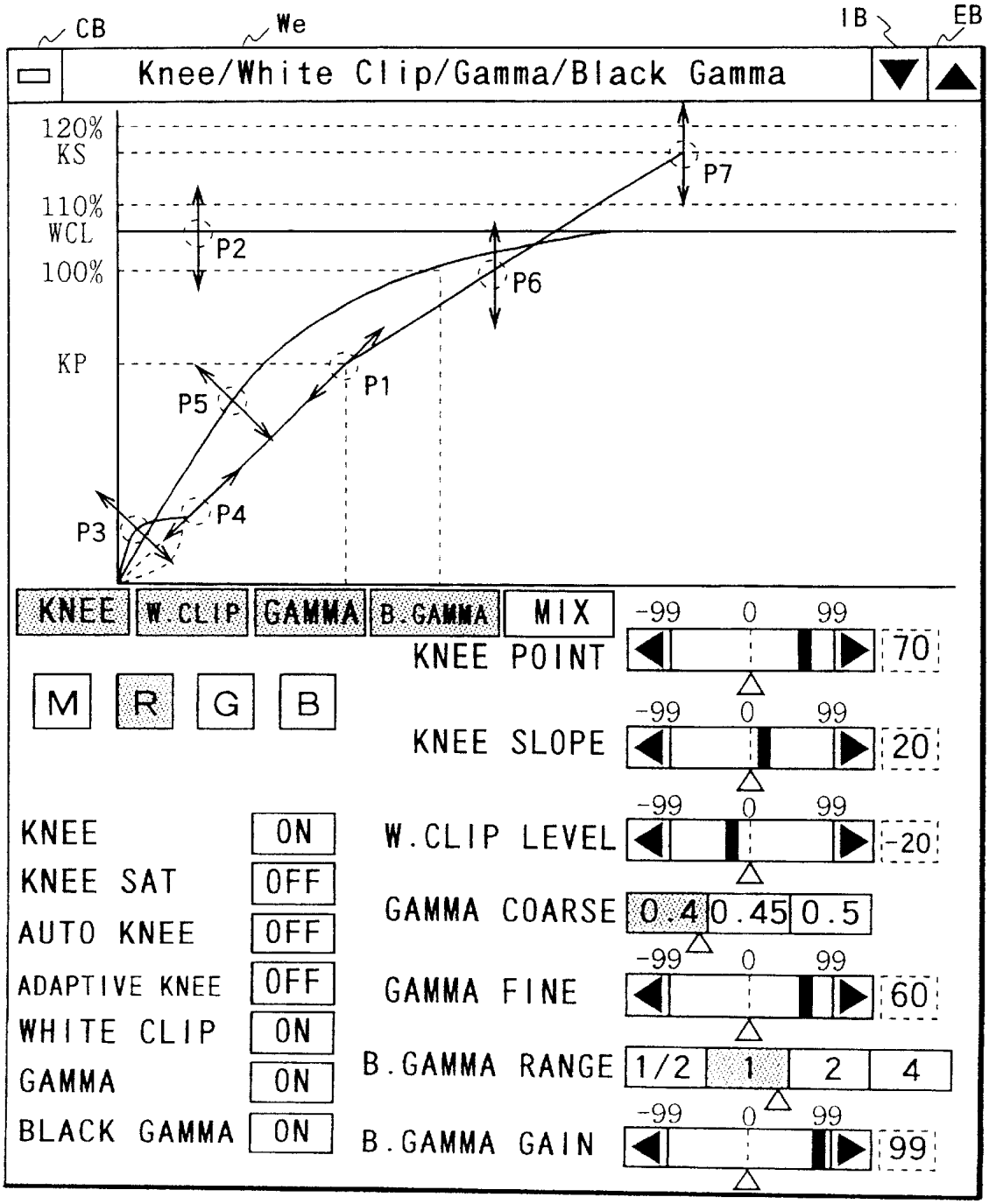

CB
We
IB
EB
Knee/White Clip/Gamma/Black Gamma
120%
KS
110%
WCL
100%
KP
P1
P2
P3
P4
P5
P6
P7
KNEE
W.CLIP
GAMMA
B.GAMMA
MIX
M
R
G
B
KNEE ON
KNEE SAT OFF
AUTO KNEE OFF
ADAPTIVE KNEE OFF
WHITE CLIP ON
GAMMA ON
BLACK GAMMA ON
KNEE POINT -99 0 99 70
KNEE SLOPE -99 0 99 20
W.CLIP LEVEL -99 0 99 -20
GAMMA COARSE 0.4 0.45 0.5
GAMMA FINE -99 0 99 60
B.GAMMA RANGE 1/2 1 2 4
B.GAMMA GAIN -99 0 99 99

FIG. 69

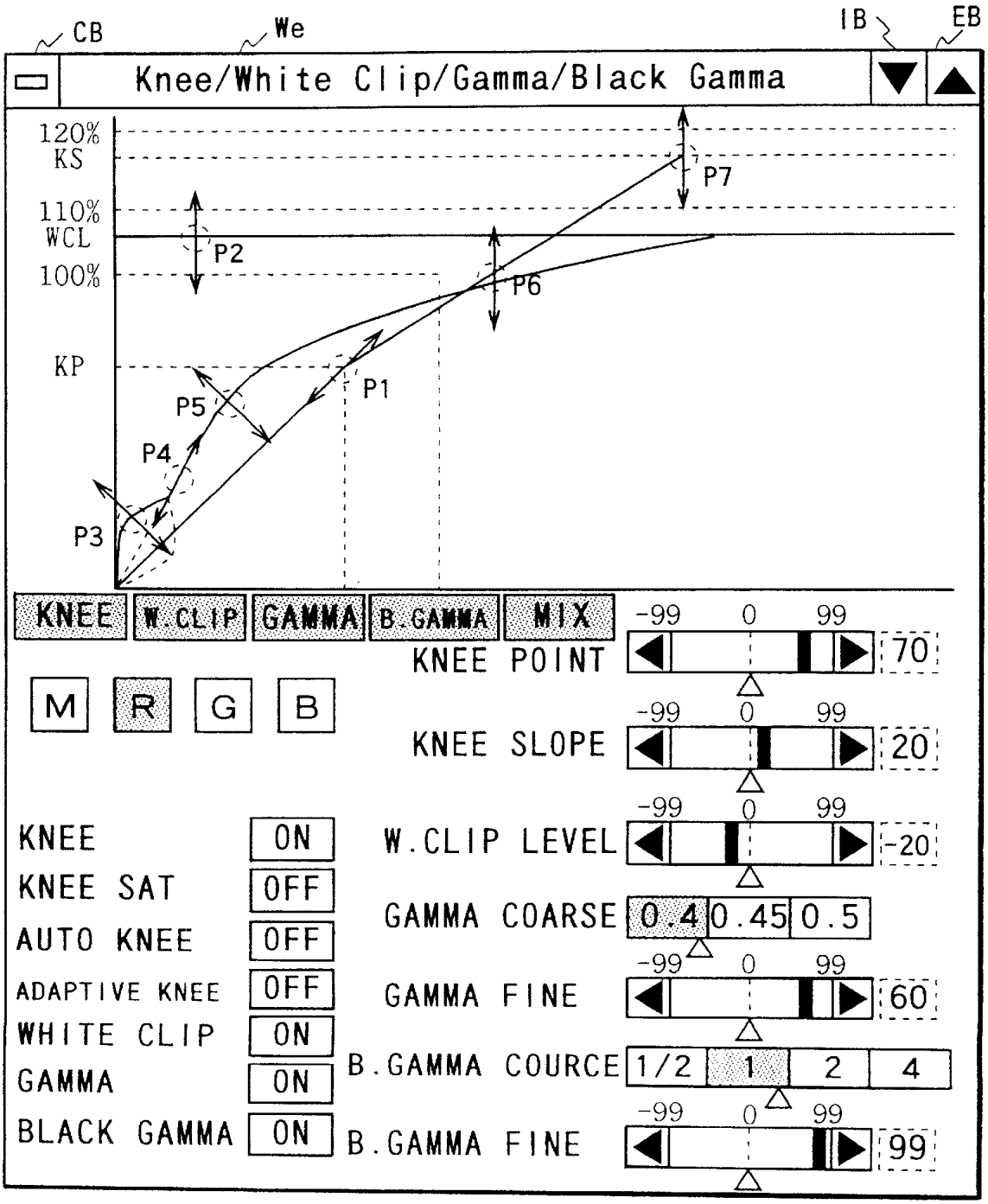

CB
We
IB
EB
Knee/White Clip/Gamma/Black Gamma
120%
KS
110%
WCL
100%
KP
P1
P2
P3
P4
P5
P6
P7
KNEE
W.CLIP
GAMMA
B.GAMMA
MIX
M
R
G
B
KNEE ON
KNEE SAT OFF
AUTO KNEE OFF
ADAPTIVE KNEE OFF
WHITE CLIP ON
GAMMA ON
BLACK GAMMA ON
KNEE POINT -99 0 99 70
KNEE SLOPE -99 0 99 20
W.CLIP LEVEL -99 0 99 -20
GAMMA COARSE 0.4 0.45 0.5
GAMMA FINE -99 0 99 60
B.GAMMA COURCE 1/2 1 2 4
B.GAMMA FINE -99 0 99 99

FIG. 70

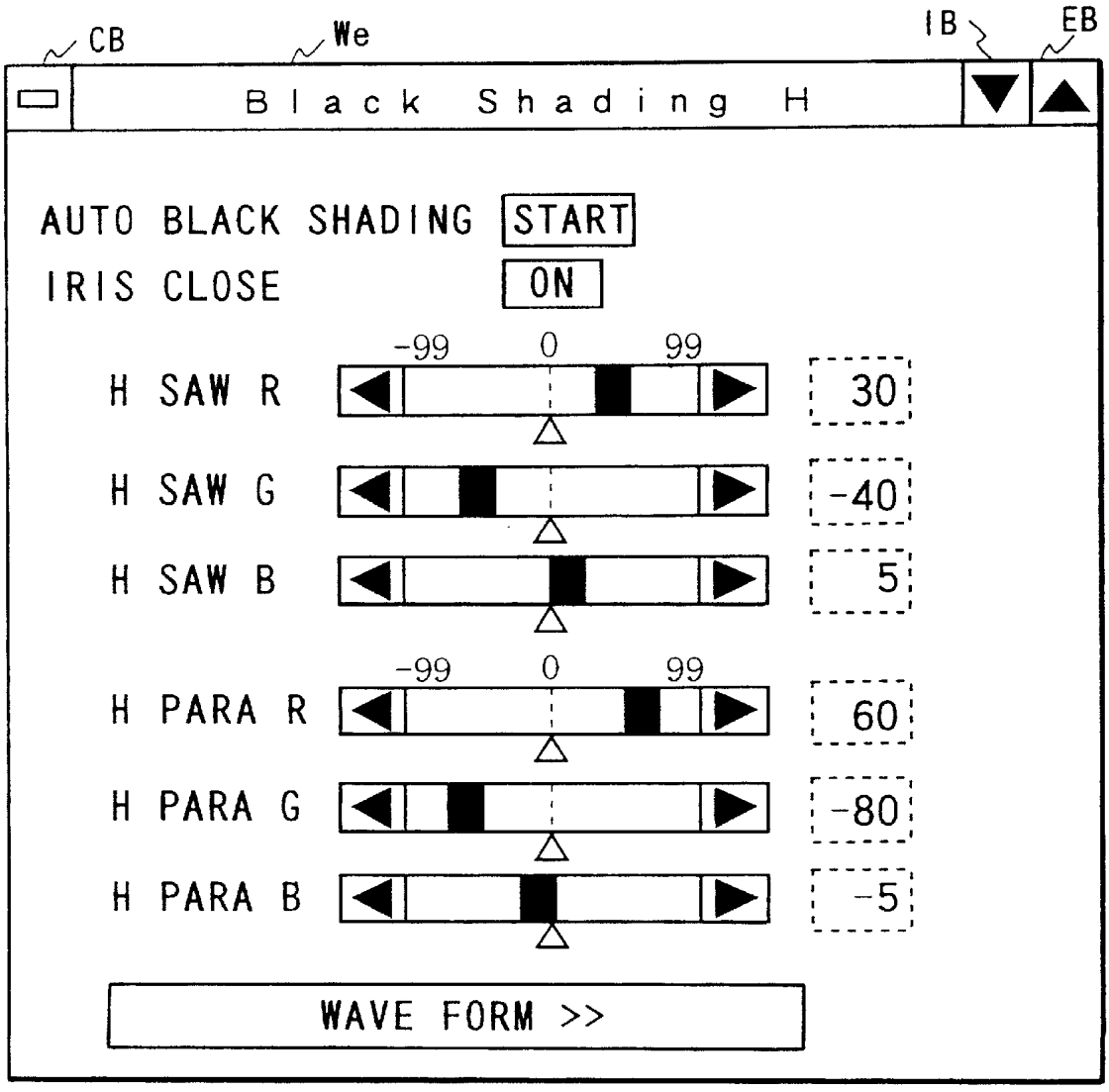

CB
We
IB
EB
Black Shading H
AUTO BLACK SHADING
START
IRIS CLOSE
ON
-99
0
99
H SAW R
30
H SAW G
-40
H SAW B
5
-99
0
99
H PARA R
60
H PARA G
-80
H PARA B
-5
WAVE FORM >>

FIG. 71

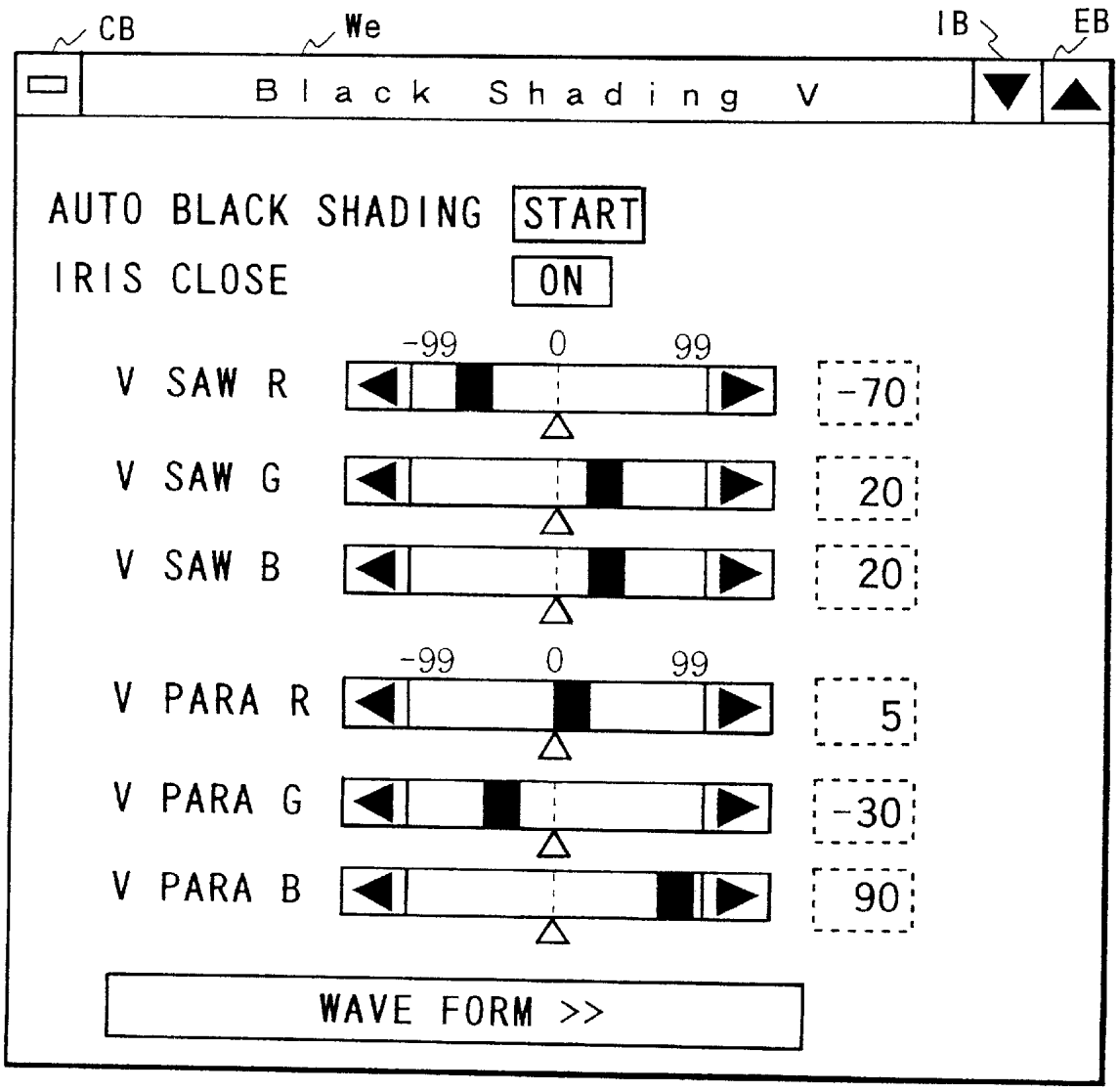

CB
We
IB
EB
Black Shading V
AUTO BLACK SHADING
START
IRIS CLOSE
ON
-99
0
99
V SAW R
-70
V SAW G
20
V SAW B
20
-99
0
99
V PARA R
5
V PARA G
-30
V PARA B
90
WAVE FORM >>

FIG. 72

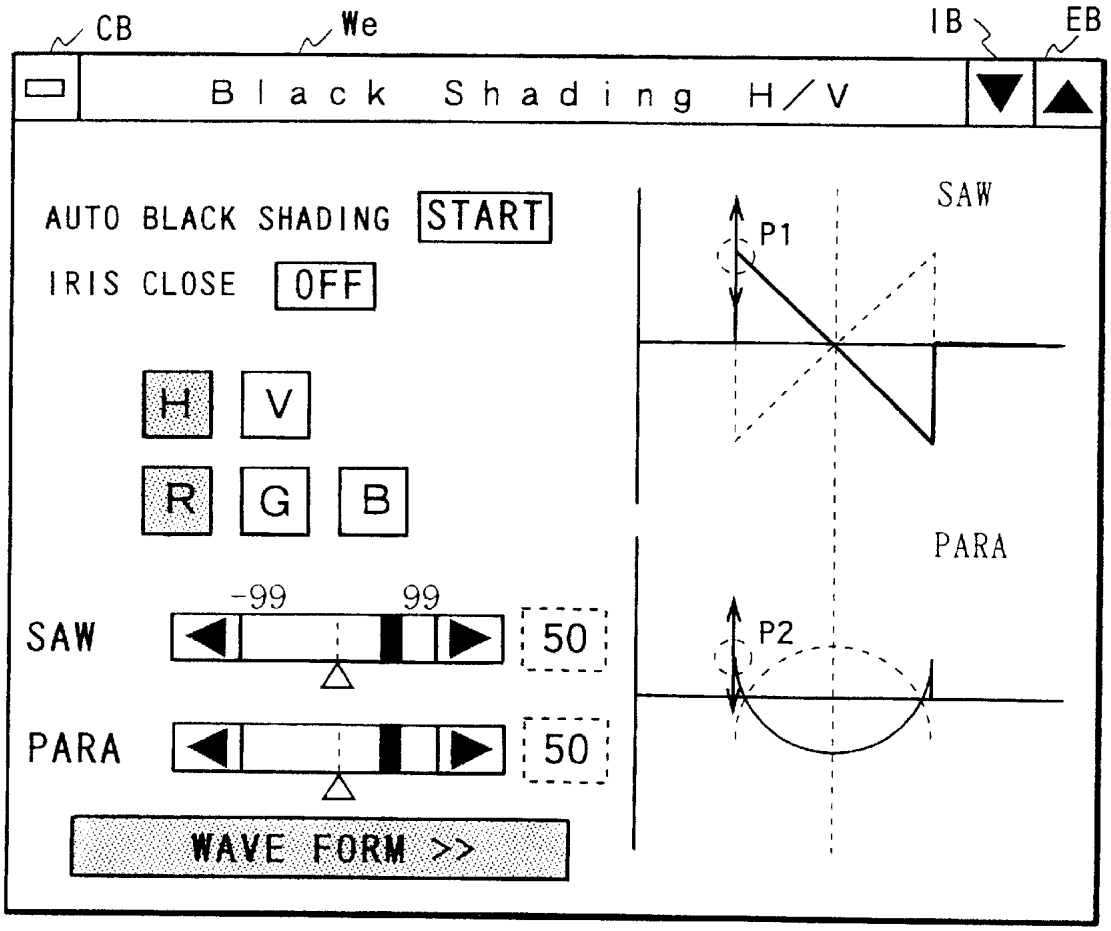

CB
We
IB
EB
Black Shading H/V
AUTO BLACK SHADING
START
IRIS CLOSE
OFF
H
V
R
G
B
-99
99
SAW
50
PARA
50
WAVE FORM >>
SAW
P1
PARA
P2

FIG. 73

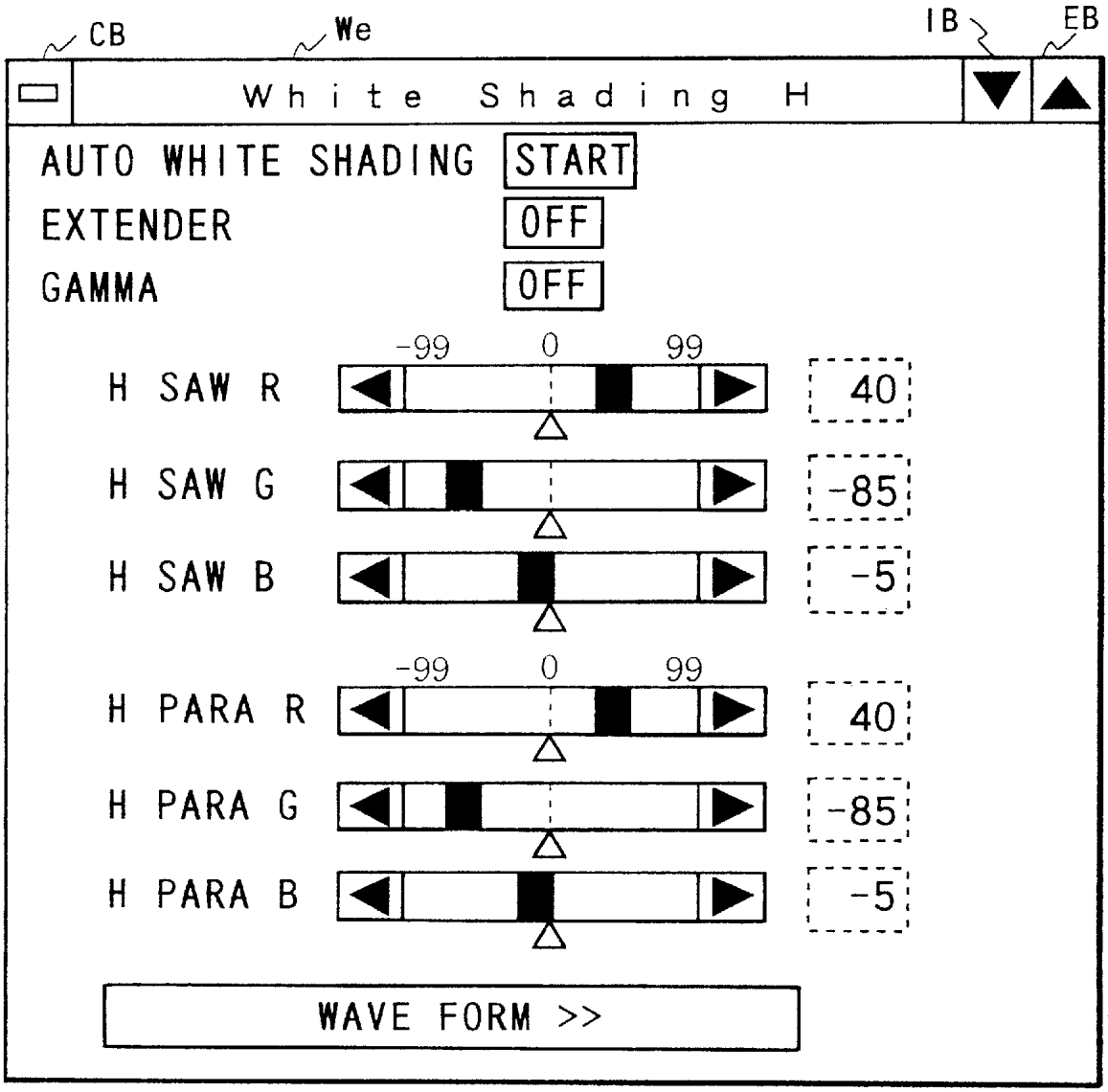

CB
We
IB
EB
White Shading H
AUTO WHITE SHADING
START
EXTENDER
OFF
GAMMA
OFF
-99
0
99
H SAW R
40
H SAW G
-85
H SAW B
-5
-99
0
99
H PARA R
40
H PARA G
-85
H PARA B
-5
WAVE FORM >>

FIG. 74

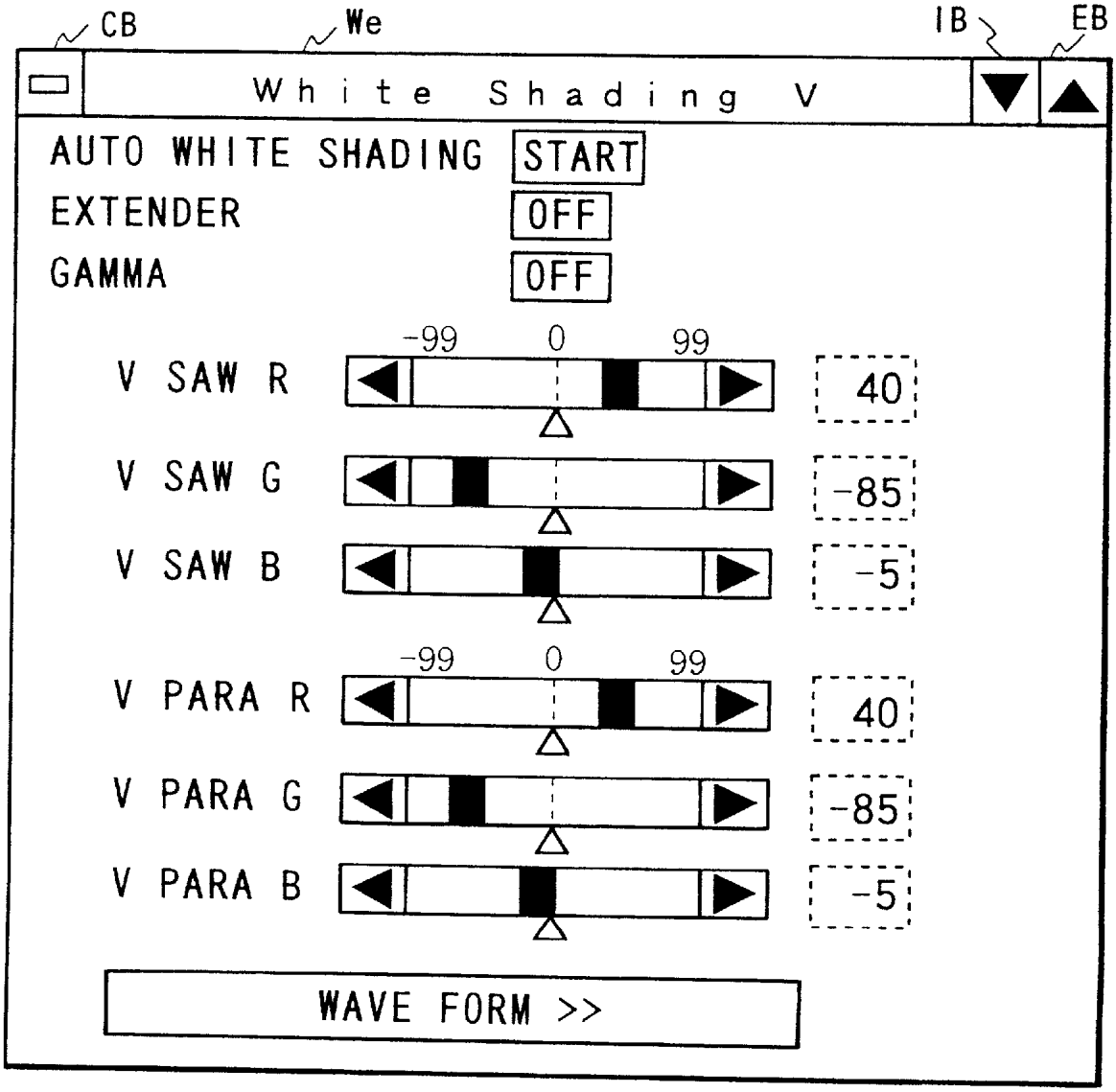

CB
We
IB
EB
White Shading V
AUTO WHITE SHADING
START
EXTENDER
OFF
GAMMA
OFF
-99
0
99
V SAW R
40
V SAW G
-85
V SAW B
-5
-99
0
99
V PARA R
40
V PARA G
-85
V PARA B
-5
WAVE FORM >>

FIG. 75

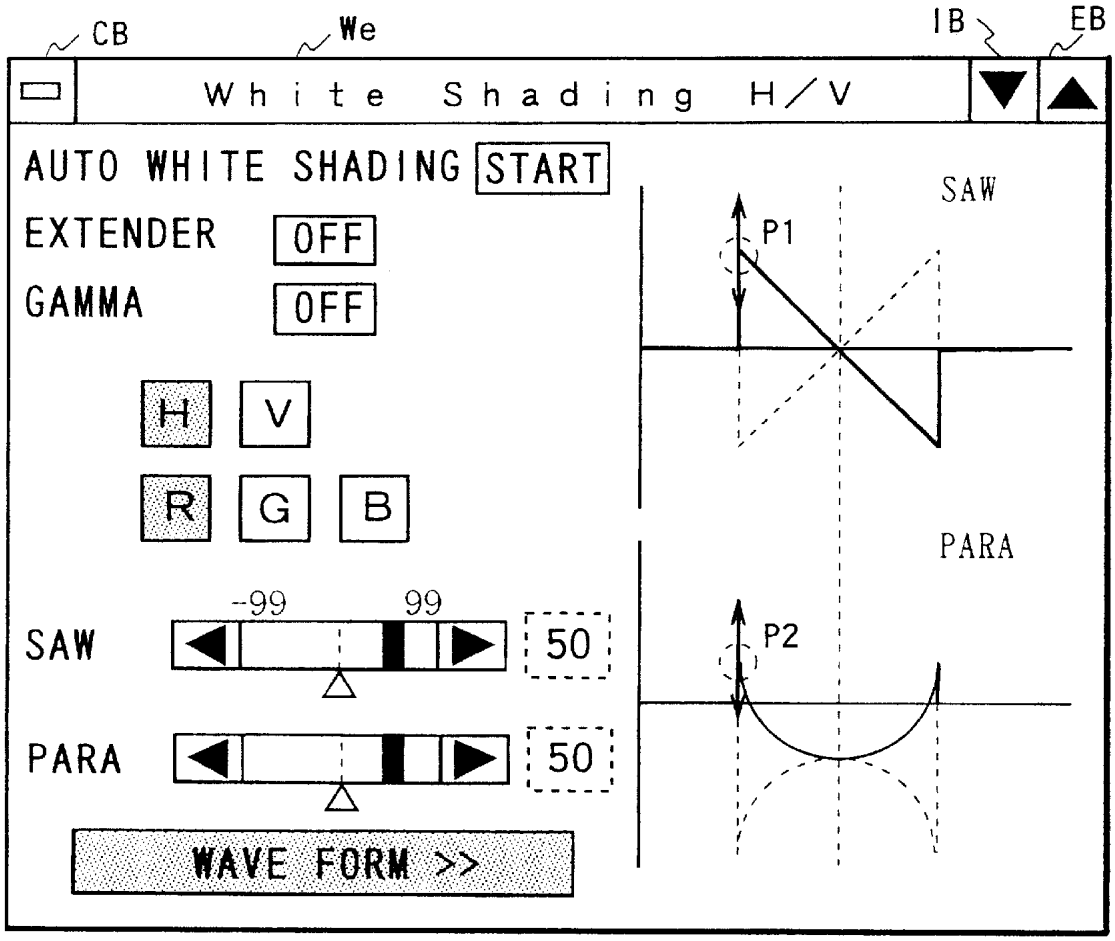

CB
We
IB
EB
White Shading H/V
AUTO WHITE SHADING
START
EXTENDER
OFF
GAMMA
OFF
H
V
R
G
B
-99
99
SAW
50
PARA
50
WAVE FORM >>
SAW
P1
PARA
P2

FIG. 76A

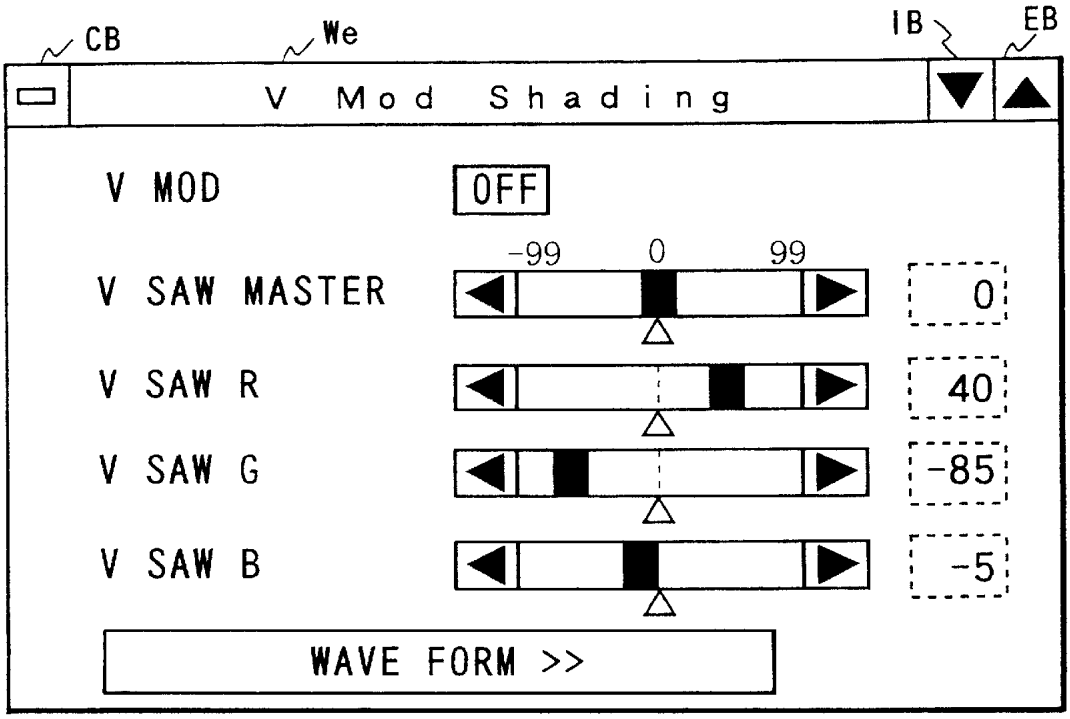


FIG. 76B

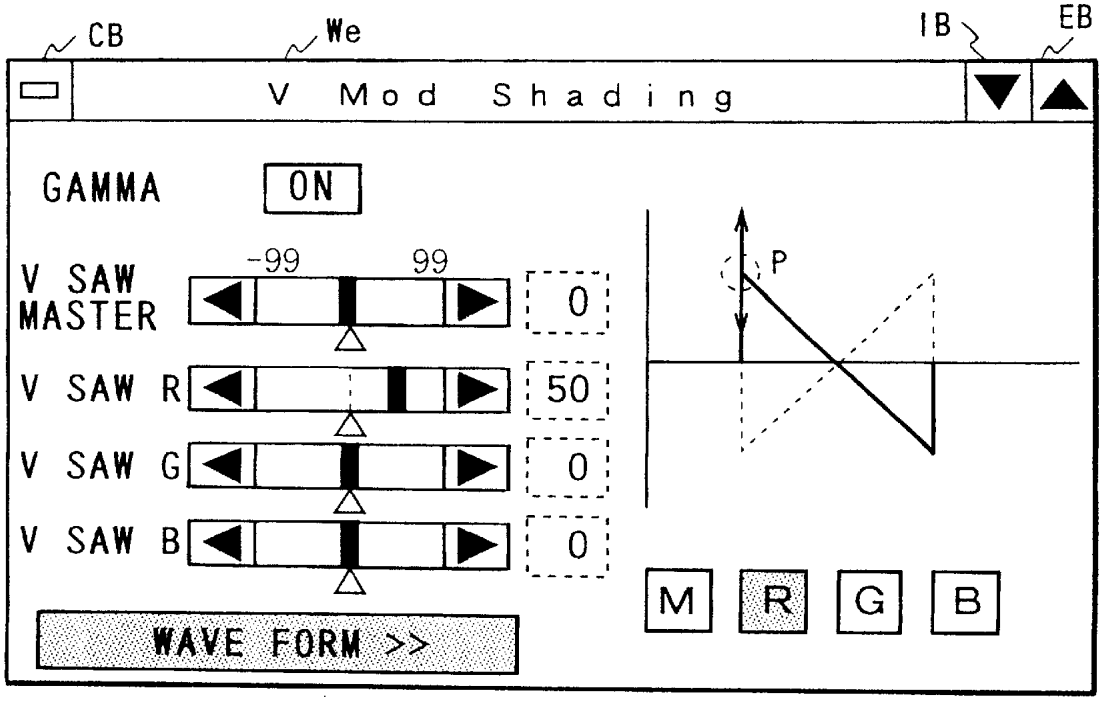


FIG. 77A

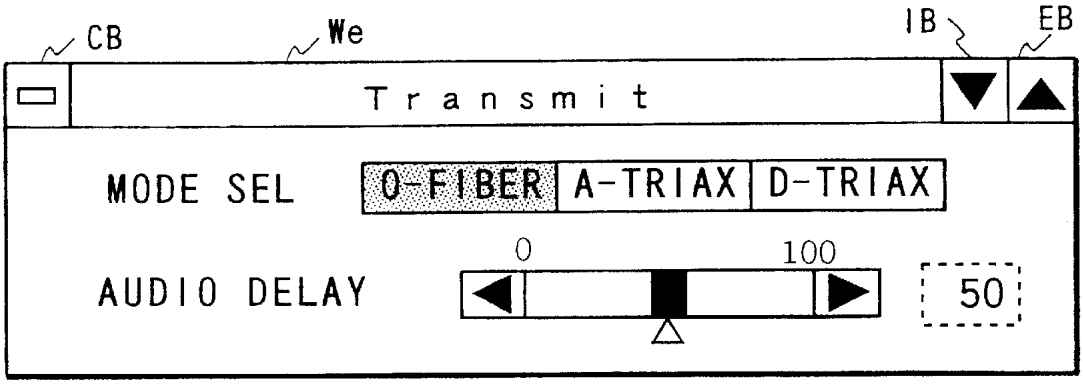


FIG. 77B

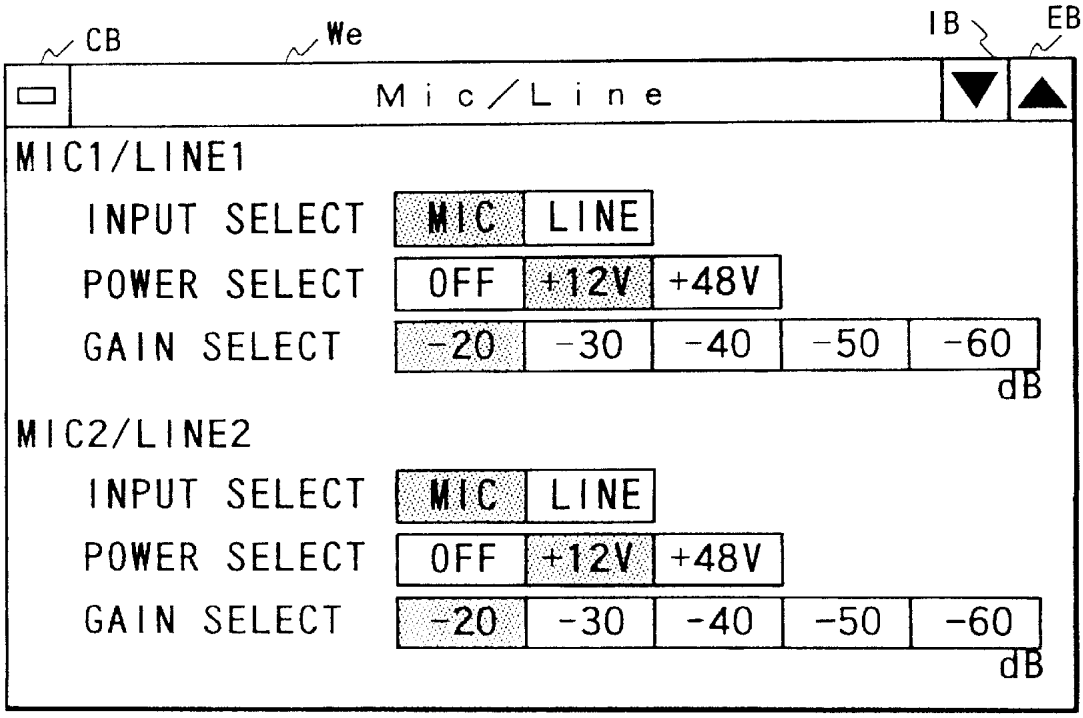


FIG. 78

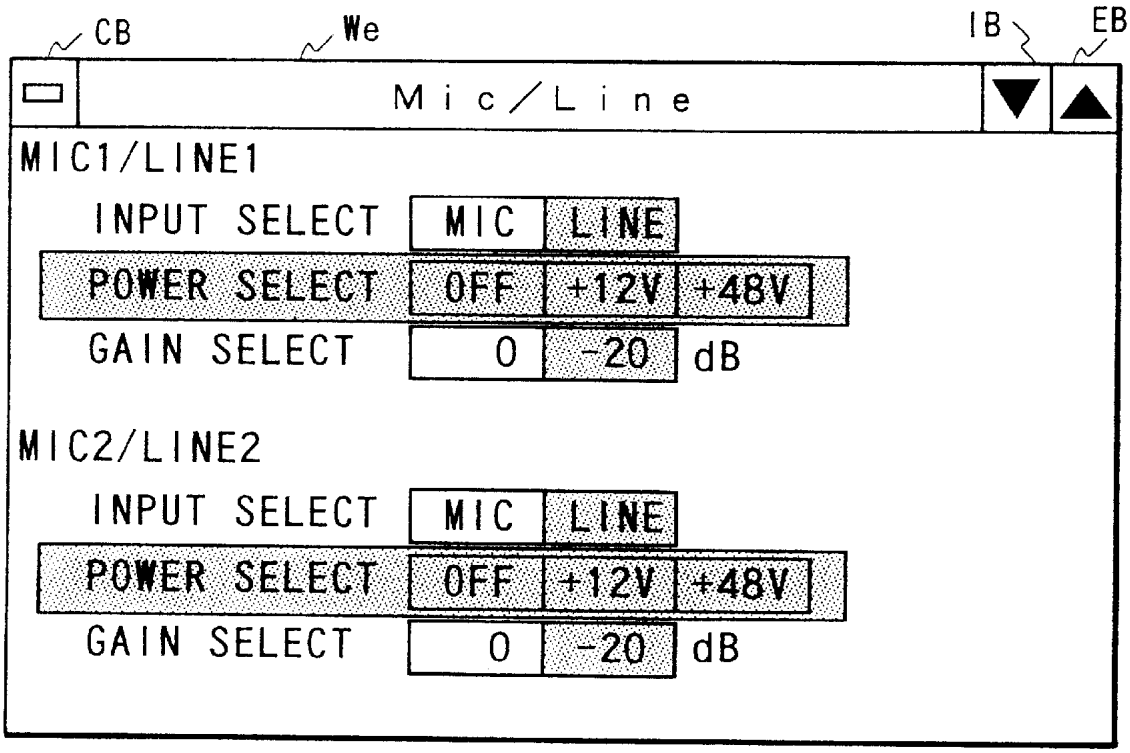

CB
We
IB
EB
Mic/Line
MIC1/LINE1
INPUT SELECT
MIC
LINE
POWER SELECT
OFF
+12V
+48V
GAIN SELECT
0
-20
dB
MIC2/LINE2
INPUT SELECT
MIC
LINE
POWER SELECT
OFF
+12V
+48V
GAIN SELECT
0
-20
dB

FIG. 79

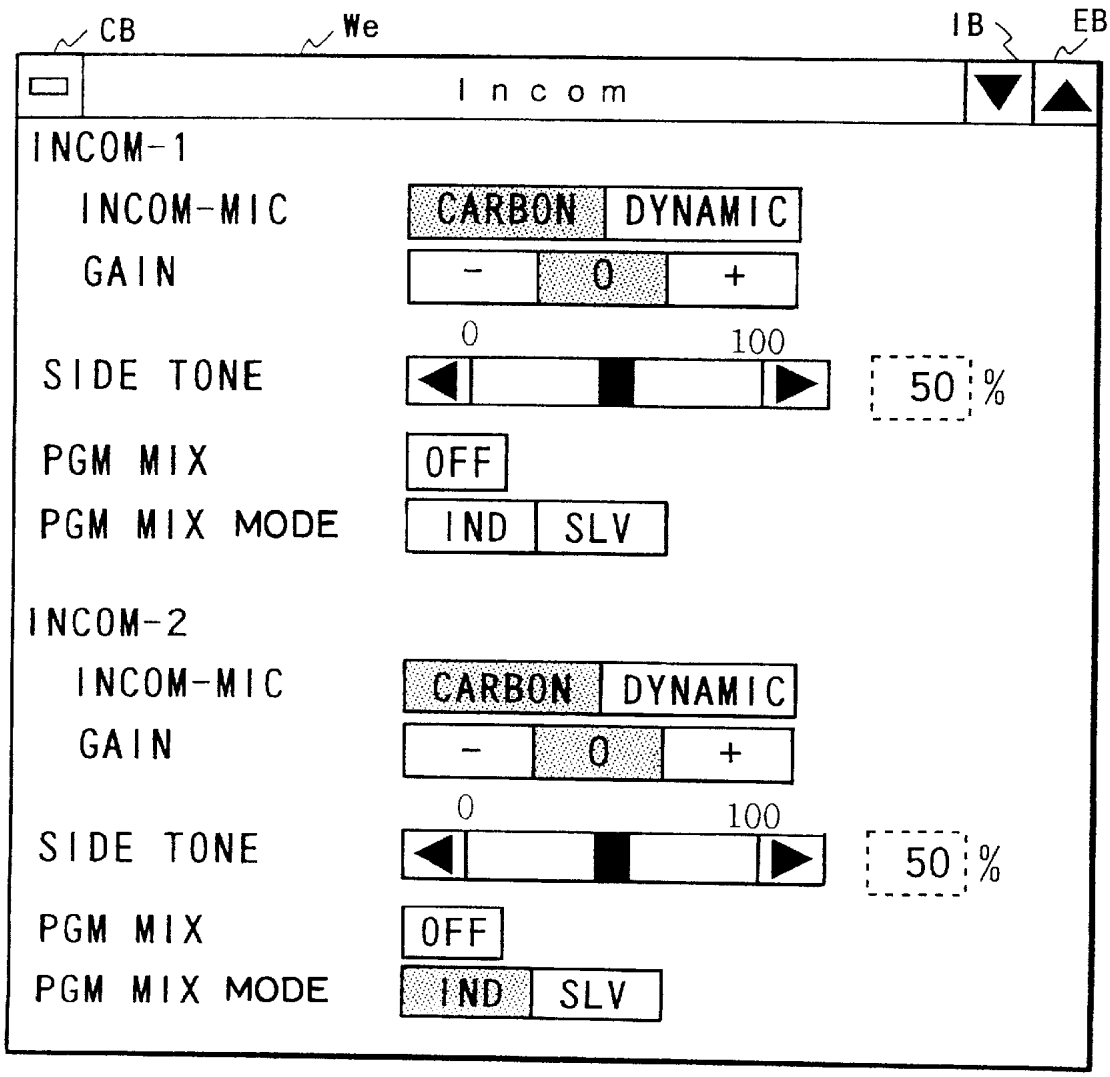

CB
We
IB
EB
Incom
INCOM-1
INCOM-MIC
CARBON
DYNAMIC
GAIN
-
0
+
SIDE TONE
0
100
50
%
PGM MIX
OFF
PGM MIX MODE
IND
SLV
INCOM-2
INCOM-MIC
CARBON
DYNAMIC
GAIN
-
0
+
SIDE TONE
0
100
50
%
PGM MIX
OFF
PGM MIX MODE
IND
SLV

FIG. 80A

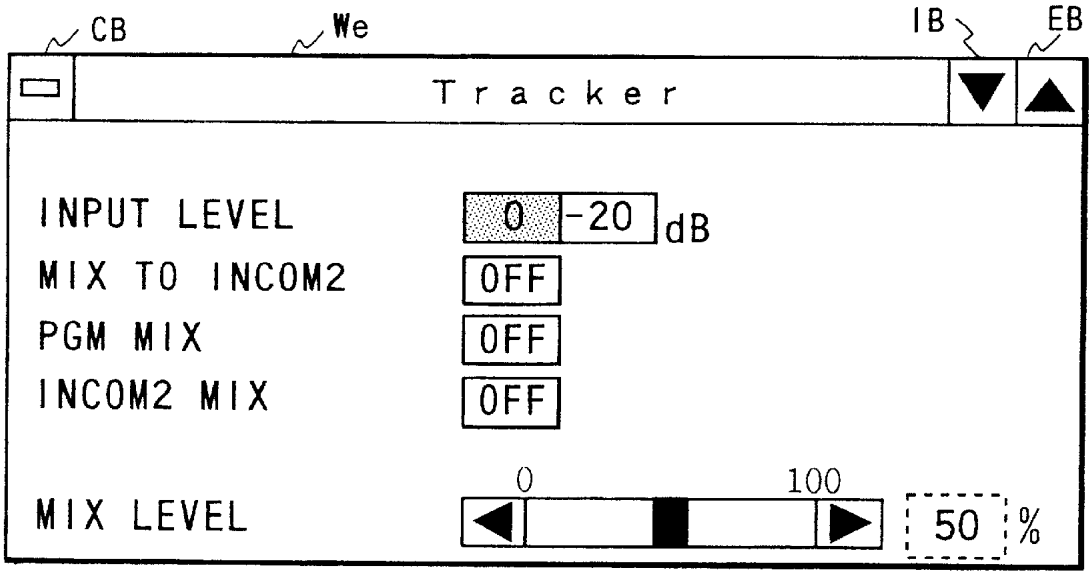


FIG. 80B

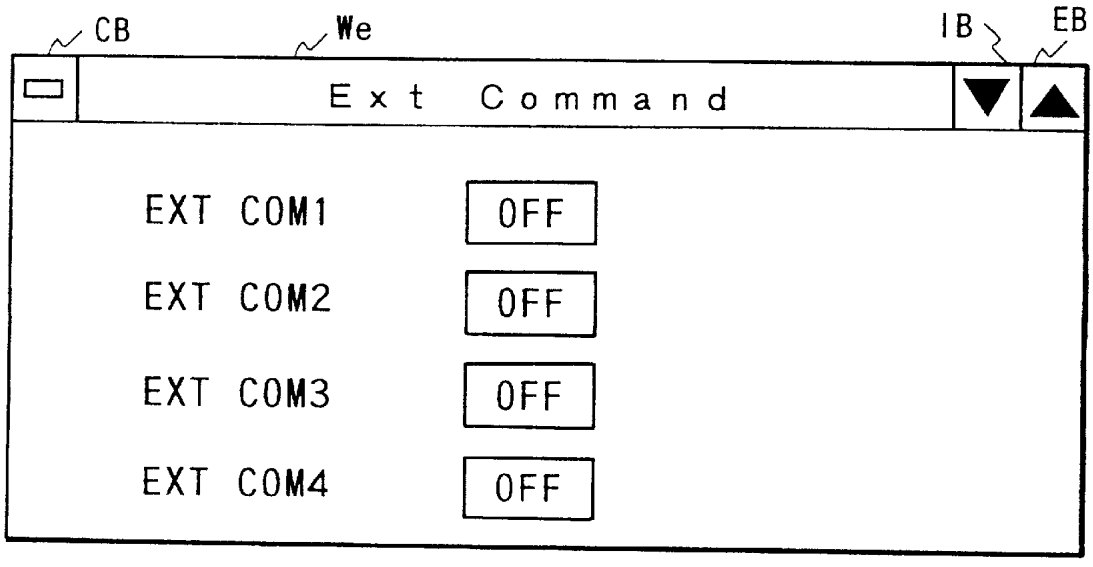


FIG. 81

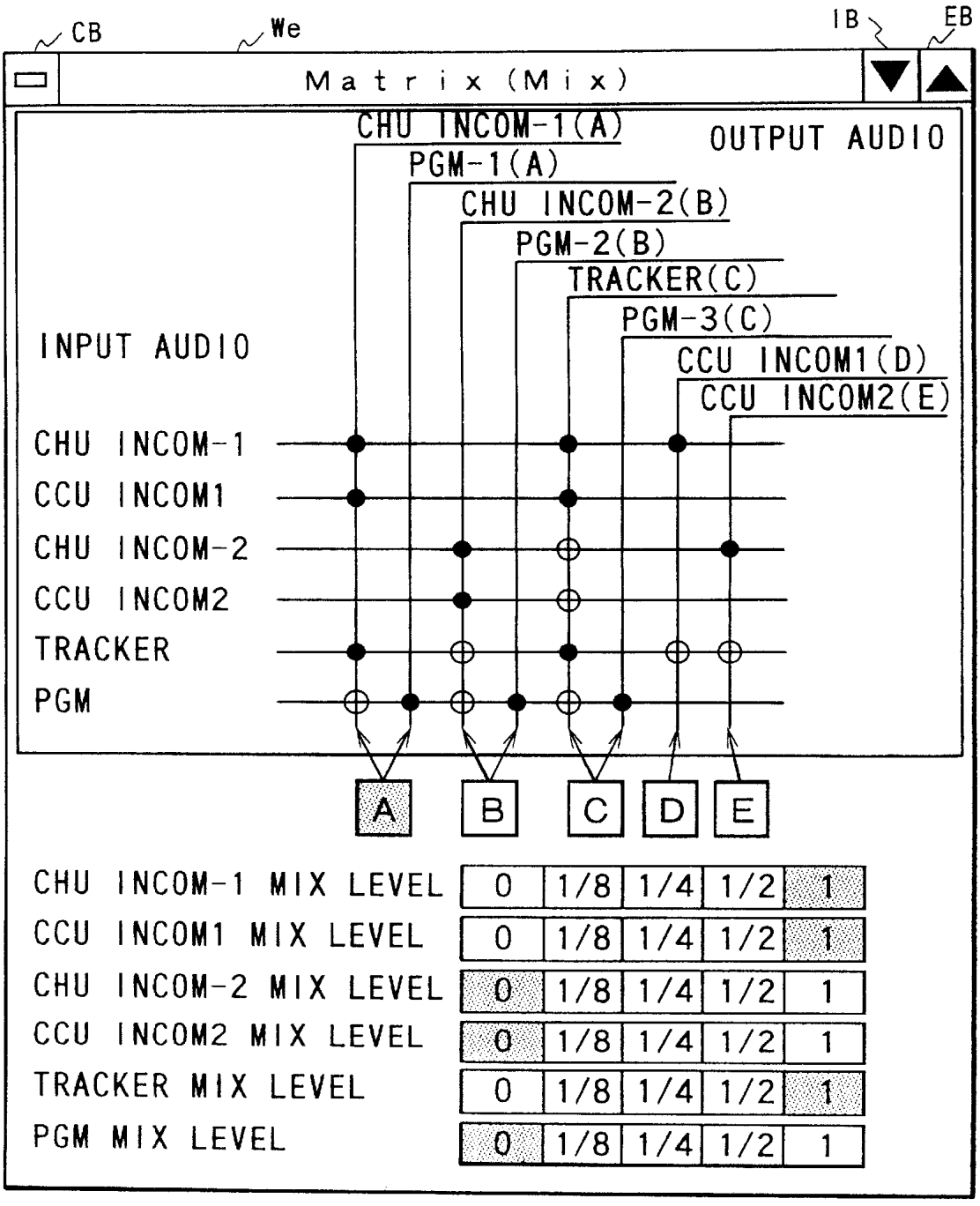

CB
We
IB
EB
Matrix (Mix)
CHU INCOM-1(A)
PGM-1(A)
CHU INCOM-2(B)
PGM-2(B)
TRACKER(C)
PGM-3(C)
CCU INCOM1(D)
CCU INCOM2(E)
OUTPUT AUDIO
INPUT AUDIO
CHU INCOM-1
CCU INCOM1
CHU INCOM-2
CCU INCOM2
TRACKER
PGM
A
B
C
D
E
CHU INCOM-1 MIX LEVEL 0 1/8 1/4 1/2 1
CCU INCOM1 MIX LEVEL 0 1/8 1/4 1/2 1
CHU INCOM-2 MIX LEVEL 0 1/8 1/4 1/2 1
CCU INCOM2 MIX LEVEL 0 1/8 1/4 1/2 1
TRACKER MIX LEVEL 0 1/8 1/4 1/2 1
PGM MIX LEVEL 0 1/8 1/4 1/2 1

FIG. 82

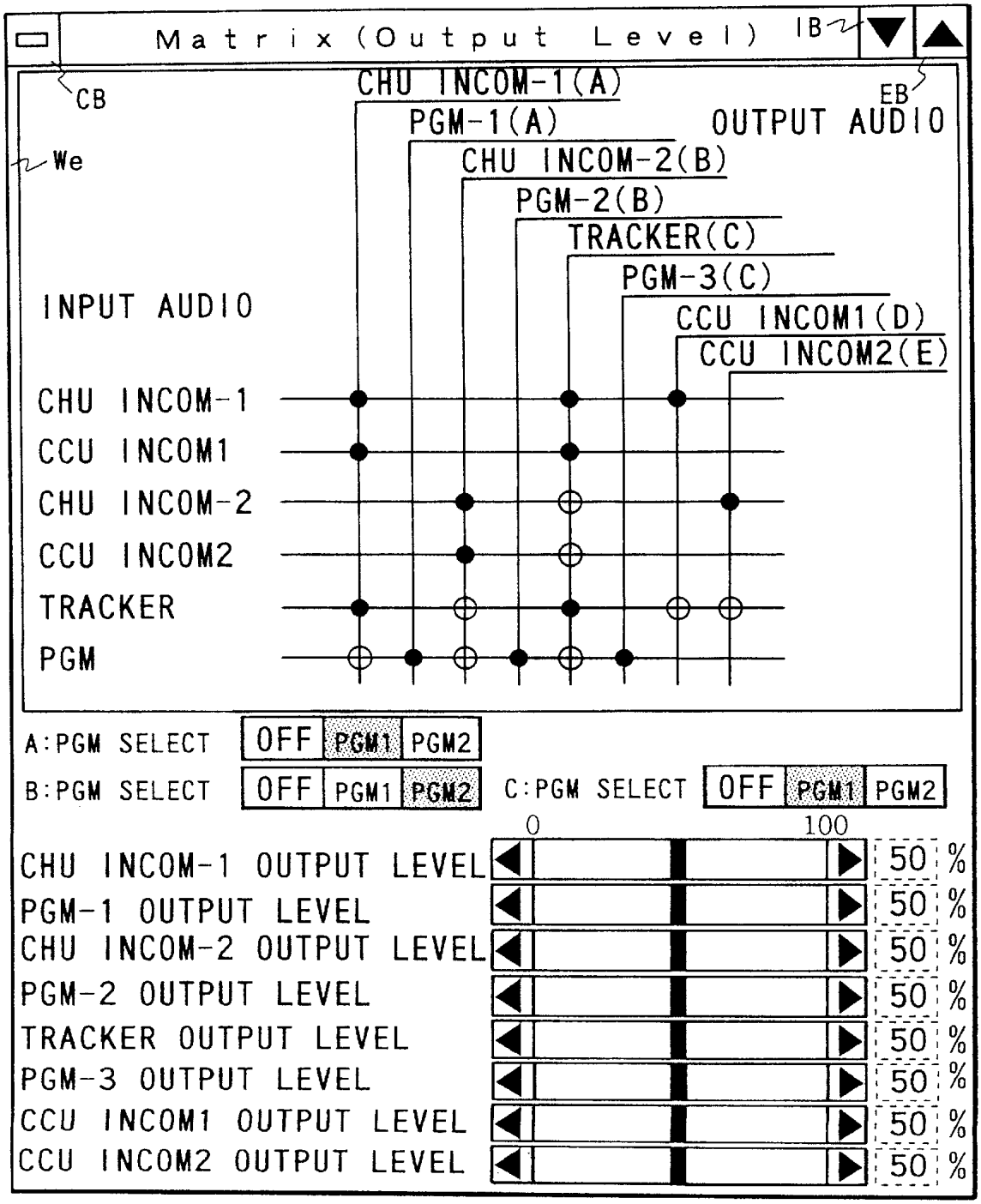

Matrix (Output Level)
IB
CB
EB
We
CHU INCOM-1(A)
PGM-1(A)
OUTPUT AUDIO
CHU INCOM-2(B)
PGM-2(B)
TRACKER(C)
PGM-3(C)
CCU INCOM1(D)
CCU INCOM2(E)
INPUT AUDIO
CHU INCOM-1
CCU INCOM1
CHU INCOM-2
CCU INCOM2
TRACKER
PGM
A:PGM SELECT OFF PGM1 PGM2
B:PGM SELECT OFF PGM1 PGM2
C:PGM SELECT OFF PGM1 PGM2
0
100
CHU INCOM-1 OUTPUT LEVEL 50 %
PGM-1 OUTPUT LEVEL 50 %
CHU INCOM-2 OUTPUT LEVEL 50 %
PGM-2 OUTPUT LEVEL 50 %
TRACKER OUTPUT LEVEL 50 %
PGM-3 OUTPUT LEVEL 50 %
CCU INCOM1 OUTPUT LEVEL 50 %
CCU INCOM2 OUTPUT LEVEL 50 %

FIG. 83

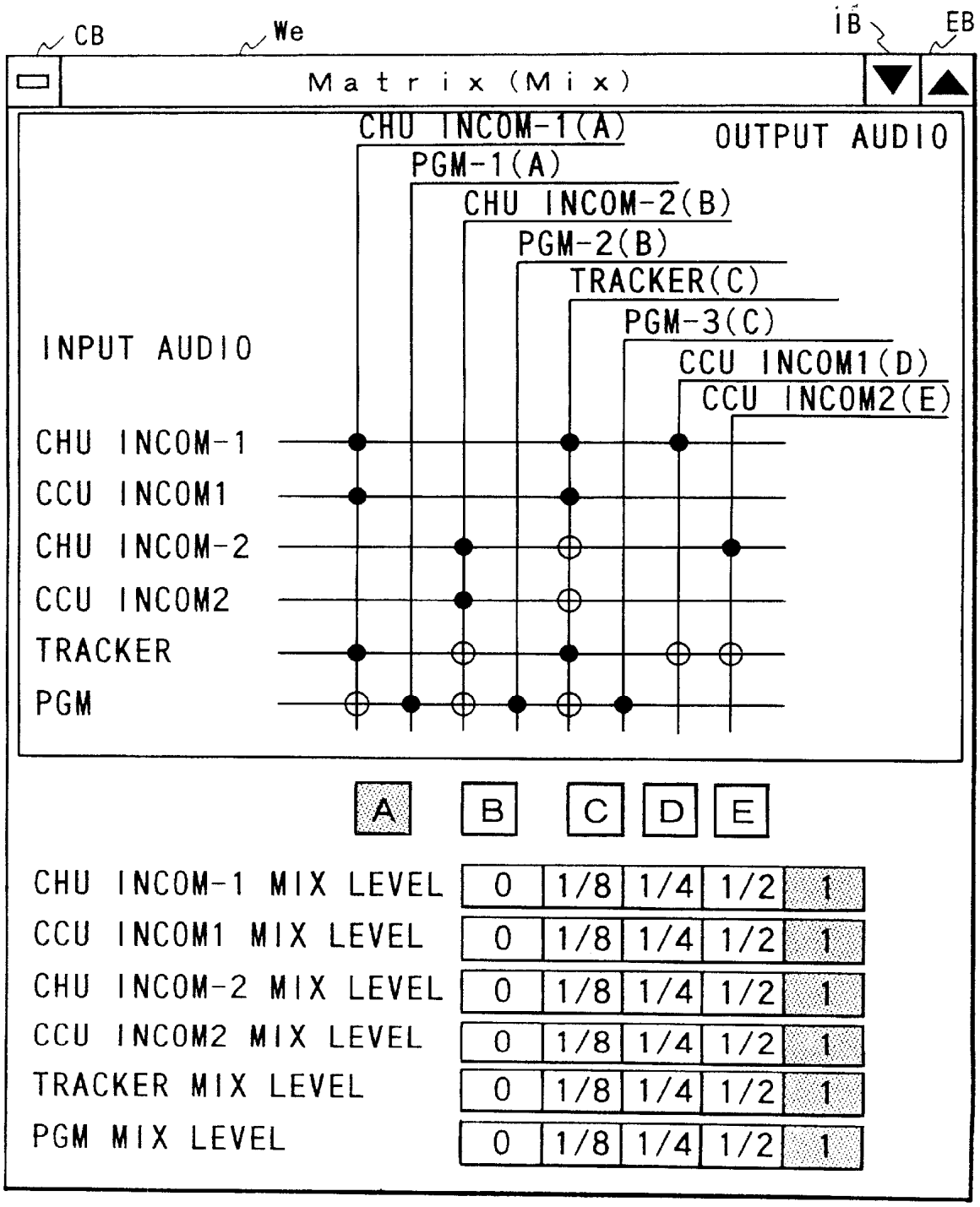

CB
We
IB
EB
Matrix (Mix)
CHU INCOM-1(A)
PGM-1(A)
CHU INCOM-2(B)
PGM-2(B)
TRACKER(C)
PGM-3(C)
CCU INCOM1(D)
CCU INCOM2(E)
OUTPUT AUDIO
INPUT AUDIO
CHU INCOM-1
CCU INCOM1
CHU INCOM-2
CCU INCOM2
TRACKER
PGM
A
B
C
D
E
CHU INCOM-1 MIX LEVEL
CCU INCOM1 MIX LEVEL
CHU INCOM-2 MIX LEVEL
CCU INCOM2 MIX LEVEL
TRACKER MIX LEVEL
PGM MIX LEVEL
0
1/8
1/4
1/2
1

FIG. 84

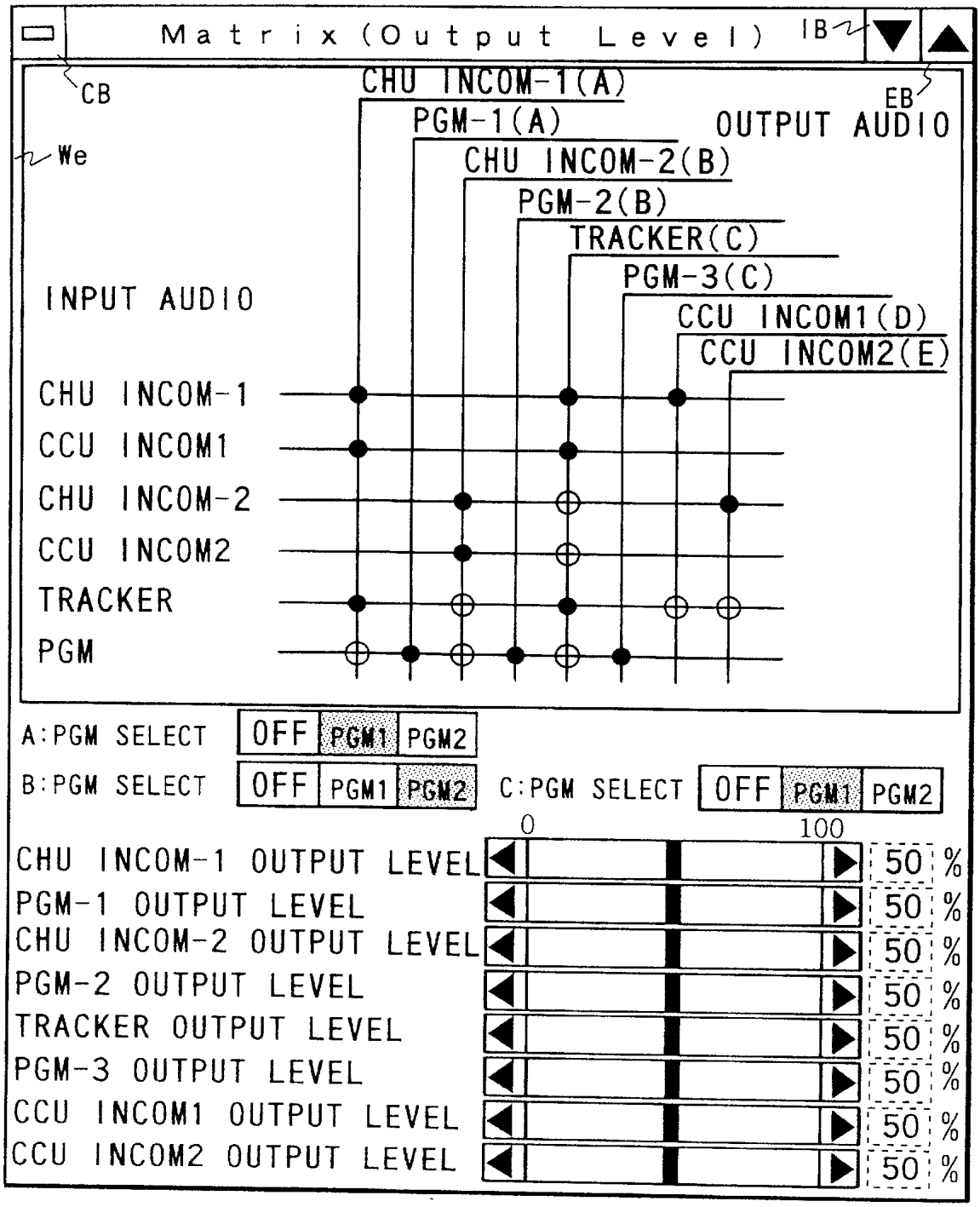
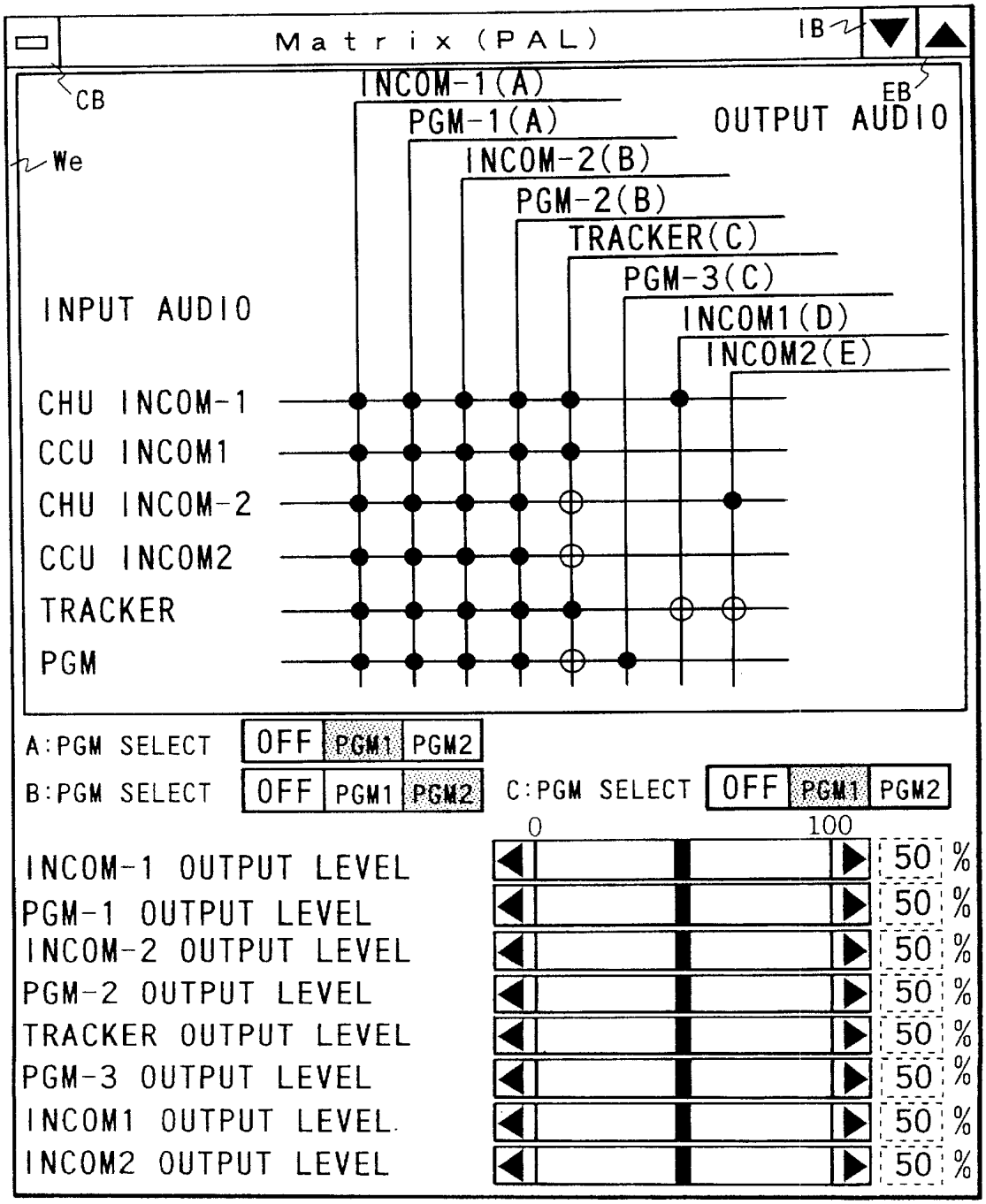

Matrix (Output Level)
IB
CB
EB
We
CHU INCOM-1(A)
PGM-1(A)
CHU INCOM-2(B)
PGM-2(B)
TRACKER(C)
PGM-3(C)
CCU INCOM1(D)
CCU INCOM2(E)
OUTPUT AUDIO
INPUT AUDIO
CHU INCOM-1
CCU INCOM1
CHU INCOM-2
CCU INCOM2
TRACKER
PGM
A:PGM SELECT OFF PGM1 PGM2
B:PGM SELECT OFF PGM1 PGM2
C:PGM SELECT OFF PGM1 PGM2
0
100
CHU INCOM-1 OUTPUT LEVEL 50 %
PGM-1 OUTPUT LEVEL 50 %
CHU INCOM-2 OUTPUT LEVEL 50 %
PGM-2 OUTPUT LEVEL 50 %
TRACKER OUTPUT LEVEL 50 %
PGM-3 OUTPUT LEVEL 50 %
CCU INCOM1 OUTPUT LEVEL 50 %
CCU INCOM2 OUTPUT LEVEL 50 %

FIG. 85


Matrix (PAL)
IB
CB
EB
We
INCOM-1(A)
PGM-1(A)
INCOM-2(B)
PGM-2(B)
TRACKER(C)
PGM-3(C)
INCOM1(D)
INCOM2(E)
OUTPUT AUDIO
INPUT AUDIO
CHU INCOM-1
CCU INCOM1
CHU INCOM-2
CCU INCOM2
TRACKER
PGM
A:PGM SELECT
OFF PGM1 PGM2
B:PGM SELECT
OFF PGM1 PGM2
C:PGM SELECT
OFF PGM1 PGM2
0
100
INCOM-1 OUTPUT LEVEL 50 %
PGM-1 OUTPUT LEVEL 50 %
INCOM-2 OUTPUT LEVEL 50 %
PGM-2 OUTPUT LEVEL 50 %
TRACKER OUTPUT LEVEL 50 %
PGM-3 OUTPUT LEVEL 50 %
INCOM1 OUTPUT LEVEL 50 %
INCOM2 OUTPUT LEVEL 50 %

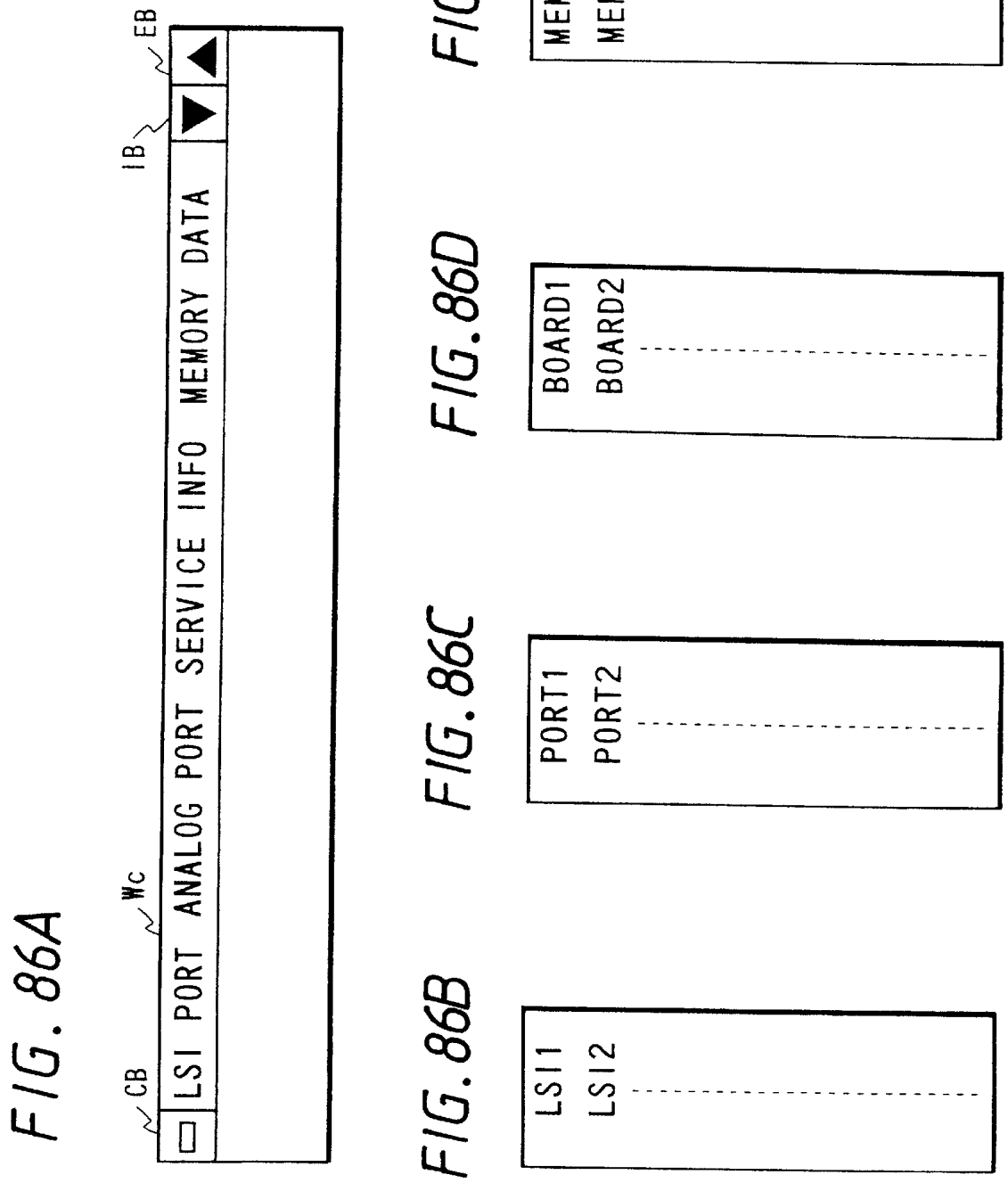


FIG. 86A
CB
Wc
LSI PORT ANALOG PORT SERVICE INFO MEMORY DATA
IB
EB
FIG. 86B
LSI1
LSI2
FIG. 86C
PORT1
PORT2
FIG. 86D
BOARD1
BOARD2
FIG. 86E
MEMORY1
MEMORY2

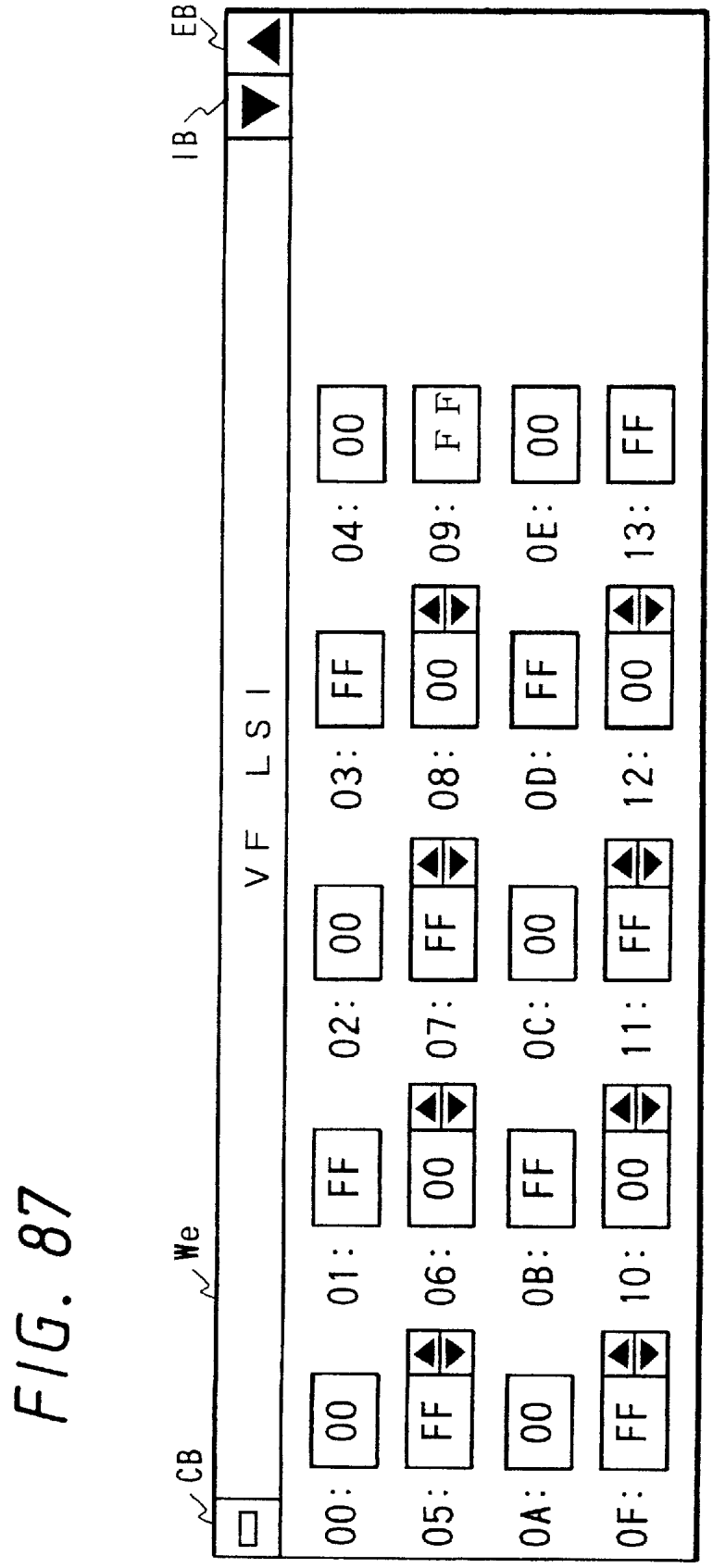

EB
IB
VF LSI
We
CB
00: 00
01: FF
02: 00
03: FF
04: 00
05: FF
06: 00
07: FF
08: 00
09: FF
0A: 00
0B: FF
0C: 00
0D: FF
0E: 00
0F: FF
10: 00
11: FF
12: 00
13: FF

FIG. 87

METHOD OF AND APPARATUS FOR SETTING UP ELECTRONIC DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of and an apparatus for setting up an electronic device such as a video camera (including a video tape recorder integrally combined with a video camera) for home use or a video camera for use in broadcasting stations.

2. Description of the Related Art

Video cameras have many parameters including white, black, gamma, knee, detail and other parameters to be established. It has been customary for the user of a video camera to establish those parameters by adjusting volumes or variable resistors in the video camera or pressing an incremental or decremental button on the video camera to increment or decrement parameter settings.

However, the conventional practice to establish many parameters of an electronic device such as a video camera is not an efficient process. Furthermore, when there are stringent standards imposed on video images outputted from video cameras for use in broadcasting stations, the user is required to actually shoot a reference image with the video camera and judge the reference image thus shot in order to confirm whether the parameters that have been established satisfy those standards which have been intended or imposed.

There has been a demand for a process of establishing parameters for an electronic device such as a video camera more efficiently, reliably, and accurately than before.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method of and an apparatus for setting up an electronic device such as a video camera by establishing parameters thereof more efficiently, reliably, and accurately than before.

According to the present invention, there is provided a method of setting up an electronic device by transmitting parameters indicated by a controller to a controlled device to set up the controlled device, comprising the steps of displaying a parameter setting image of a plurality of parameters that can be established with respect to the controlled device, deciding whether input information is entered or not while the parameter setting image is being displayed, changing a portion of the parameter setting image which corresponds to input information if such input information is entered, establishing parameter data according to the input information, and transmitting the established parameter data or a change in the parameter data to the controlled device to change a parameter in the controlled device.

According to the present invention, there is also provided an apparatus for setting up an electronic device, comprising storage means for storing parameter setting image data for establishing one or more parameters with respect to a controlled device, the parameter setting image including parameter changing switch image data and setting state display image data, display means for displaying a parameter setting image based on the parameter setting image data read from the storage means, input means for entering input information indicating changes in display states of a parameter changing switch image data and a setting state display image which are displayed by the display means and a parameter to be established, and control means for changing the display states of the parameter changing switch image data and the setting state display image which are displayed by the display means and the parameter to be established, based on the input information entered by the input means, and transmitting changed parameter data or a change in the parameter to the controlled device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of an electronic device setup system for setting up an electronic device, which embodies a method of and an apparatus for setting up an electronic device according to the present invention;

FIG. **2** is a flowchart of an operation sequence of the an electronic device setup system shown in FIG. **1**;

FIG. **3** is a block diagram of a camera setup system which incorporates the principles of the electronic device setup system shown in FIG. **1**;

FIG. **4** is a block diagram of a computer in the camera setup system shown in FIG. **3**;

FIG. **5** is a flowchart of a control sequence according to a main routine of the computer shown in FIG. **4**;

FIGS. **6**A and **6**B are views showing initial images produced by an operating system in the computer shown in FIG. **4**;

FIG. **7** is a view of a connection configuration window which is displayed at first when the camera setup system shown in FIG. **3** starts to operate;

FIG. **8** is a view of a parameter icon window of the camera setup system;

FIGS. **9**A through **9**F are views of main pull-down menus which can be displayed from a menu bar in the connection configuration window shown in FIG. **7**;

FIGS. **10**A through **10**C are views of pull-down menus for a CHU (camera head unit), which can also be displayed from one of the pull-down menus shown in FIGS. **9**A through **9**F;

FIGS. **11**A and **11**B are views of pull-down menus for the CHU, which can also be displayed from one of the pull-down menus shown in FIGS. **9**A through **9**F;

FIGS. **12**A through **12**D are views of pull-down menus for a CCU (camera control unit), which can also be displayed from one of the pull-down menus shown in FIGS. **9**A through **9**F;

FIG. **13** is a view illustrative of basics of a parameter setting window which can be displayed from the parameter icon window shown in FIG. **8** or the pull-down menus shown in FIGS. **9**A through **9**F;

FIGS. **14** through **16** are flowcharts of a main processing sequence of the camera setup system, which is executed by the computer shown in FIG. **4**;

FIGS. **17** and **18** are flowcharts of a setup process in the main processing sequence shown in FIG. **16**;

FIG. **19** is a flowchart of a change process with a switch in the setup process shown in FIG. **17**;

FIG. **20** is a flowchart of a change process with a slide lever in the setup process shown in FIG. **18**;

FIG. **21** is a flowchart of a change process with a numerical value in the setup process shown in FIG. **18**;

FIG. **22** is a flowchart of a change process with a waveform in the setup process shown in FIG. **18**;

FIGS. **23**A through **23**E are views of a transmission data format and file formats used in the computer shown in FIG. **4**;

FIG. **24** is a block diagram of a data converter in the camera setup system shown in FIG. **3**;

FIGS. **25** through **27** are flowcharts of a control sequence of the data converter shown in FIG. **24**;

FIG. **28** is a block diagram of a video system of a camera shown in FIG. **3**;

FIG. **29** is a block diagram of an audio system of a camera shown in FIG. **3**;

FIG. **30**A is a view showing, by way of example, a displayed image for establishing shutter parameters;

FIG. **30**B is a view showing, by way of example, a displayed image for establishing filter parameters;

FIG. **31**A is a view showing, by way of example, a displayed image for establishing a test pattern and bars;

FIG. **31**B is a view showing, by way of example, a displayed image for establishing an automatic setup process;

FIG. **32**A is a view showing, by way of example, a displayed image for establishing iris parameters;

FIG. **32**B is a view showing, by way of example, a displayed image for establishing master black parameters;

FIG. **32**C is a view showing, by way of example, a displayed image for establishing a master gain parameter;

FIG. **33** is a view showing, by way of example, a displayed image for establishing knee saturation parameters;

FIG. **34** is a view showing, by way of example, a displayed image for establishing knee and knee saturation parameters;

FIG. **35** is a view showing, by way of example, a displayed image for establishing knee and knee saturation parameters for servicing;

FIG. **36**A is a view showing, by way of example, a displayed image for establishing master V modulation parameters;

FIG. **36**B is a view showing, by way of example, a displayed image for establishing knee parameters;

FIG. **37**A is a view showing, by way of example, a displayed image for establishing white clip parameters;

FIG. **37**B is a view showing, by way of example, a displayed image for establishing white clip parameters, the displayed image including a displayed waveform;

FIG. **38**A is a view showing, by way of example, a displayed image for establishing detail level parameters;

FIG. **38**B is a view showing, by way of example, a displayed image for establishing detail level parameters, the displayed image including a displayed waveform;

FIG. **39**A is a view showing, by way of example, a displayed image for establishing ratio parameters;

FIG. **39**B is a view showing, by way of example, a displayed image for establishing a gamma mix ratio parameter;

FIG. **40** is a view showing, by way of example, a displayed image for establishing a gamma mix ratio parameter, the displayed image including a displayed waveform;

FIG. **41** is a view showing, by way of example, a displayed image for establishing a gamma mix ratio parameter, the displayed image including a displayed waveform;

FIG. **42** is a view showing, by way of example, a displayed image for establishing R, G, B mix parameters;

FIG. **43**A is a view showing, by way of example, a displayed image for establishing a slim detail parameter;

FIG. **43**B is a view showing, by way of example, a displayed image for establishing a slim detail parameter, the displayed image including a displayed waveform;

FIG. **43**C is a view showing, by way of example, a displayed image for establishing a slant detail parameter;

FIG. **44**A is a view showing, by way of example, a displayed image for establishing H limiter parameters;

FIG. **44**B is a view showing, by way of example, a displayed image for establishing H limiter parameters, the displayed image including a displayed waveform;

FIG. **45**A is a view showing, by way of example, a displayed image for establishing V limiter parameters;

FIG. **45**B is a view showing, by way of example, a displayed image for establishing V limiter parameters, the displayed image including a displayed waveform;

FIG. **46** is a view showing, by way of example, a displayed image for establishing knee aperture parameters;

FIG. **47** is a view showing, by way of example, a displayed image for establishing knee aperture parameters, the displayed image including a displayed waveform;

FIG. **48** is a view showing, by way of example, a displayed image for establishing knee aperture parameters, the displayed image including a displayed waveform;

FIG. **49**A is a view showing, by way of example, a displayed image for establishing level depend parameters;

FIG. **49**B is a view showing, by way of example, a displayed image for establishing level depend parameters, the displayed image including a displayed waveform;

FIG. **50** is a view showing, by way of example, a displayed image for establishing level depend parameters for servicing, the displayed image including a displayed waveform;

FIG. **51**A is a view showing, by way of example, a displayed image for establishing crispening parameters;

FIG. **51**B is a view showing, by way of example, a displayed image for establishing crispening parameters, the displayed image including a displayed waveform;

FIG. **52** is a view showing, by way of example, a displayed image for establishing crispening parameters for servicing, the displayed image including a displayed waveform;

FIG. **53** is a view showing, by way of example, a displayed image for establishing skin tone parameters;

FIG. **54** is a view showing, by way of example, a displayed image for establishing skin tone parameters;

FIG. **55** is a view showing, by way of example, a displayed image for establishing skin tone parameters, the displayed image including a displayed waveform;

FIG. **56** is a view showing, by way of example, a displayed image for establishing skin tone parameters, the displayed image including a displayed waveform;

FIG. **57**A is a view showing, by way of example, a displayed image for establishing a detail area parameter, the displayed image including a displayed waveform;

FIG. **57**B is a view showing, by way of example, a displayed image for establishing a detail area parameter, the displayed image including a displayed waveform;

FIG. **58**A is a view showing, by way of example, a displayed image for establishing black parameters;

FIG. **58**B is a view showing, by way of example, a displayed image for establishing black parameters, the displayed image including a displayed waveform;

FIG. **59** is a view showing, by way of example, a displayed image for establishing white parameters;

FIG. **60** is a view showing, by way of example, a displayed image for establishing white parameters, the displayed image including a displayed waveform;

FIG. **61** is a view showing, by way of example, a displayed image for establishing black set parameters;

FIG. **62** is a view showing, by way of example, a displayed image for establishing flare parameters;

FIG. **63** is a view showing, by way of example, a displayed image for establishing matrix parameters;

FIG. **64** is a view showing, by way of example, a displayed image for establishing matrix parameters, the displayed image including a displayed waveform;

FIGS. **65**A and **65**B are diagrams illustrative of a matrix;

FIG. **66**A is a view showing, by way of example, a displayed image for establishing gamma parameters;

FIG. **66**B is a view showing, by way of example, a displayed image for establishing gamma parameters, the displayed image including a displayed waveform;

FIG. **67**A is a view showing, by way of example, a displayed image for establishing black gamma parameters;

FIG. **67**B is a view showing, by way of example, a displayed image for establishing black gamma parameters, the displayed image including a displayed waveform;

FIG. **68** is a view showing, by way of example, a displayed image for establishing knee, white clip, gamma, black gamma parameters, the displayed image including a displayed waveform;

FIG. **69** is a view showing, by way of example, a displayed image for establishing knee, white clip, gamma, black gamma parameters, the displayed image including a displayed waveform;

FIG. **70** is a view showing, by way of example, a displayed image for establishing black shading H parameters;

FIG. **71** is a view showing, by way of example, a displayed image for establishing black shading V parameters;

FIG. **72** is a view showing, by way of example, a displayed image for establishing black shading H/V parameters, the displayed image including displayed waveforms;

FIG. **73** is a view showing, by way of example, a displayed image for establishing white shading H parameters;

FIG. **74** is a view showing, by way of example, a displayed image for establishing white shading V parameters;

FIG. **75** is a view showing, by way of example, a displayed image for establishing white shading H/V parameters, the displayed image including displayed waveforms;

FIG. **76**A is a view showing, by way of example, a displayed image for establishing V modulation shading parameters;

FIG. **76**B is a view showing, by way of example, a displayed image for establishing V modulation shading parameters, the displayed image including displayed waveforms;

FIG. **77**A is a view showing, by way of example, a displayed image for establishing transmit parameters;

FIG. **77**B is a view showing, by way of example, a displayed image for establishing mic/line parameters;

FIG. **78** is a view showing, by way of example, a displayed image for establishing mic/line parameters;

FIG. **79** is a view showing, by way of example, a displayed image for establishing incom parameters;

FIG. **80**A is a view showing, by way of example, a displayed image for establishing tracker parameters;

FIG. **80**B is a view showing, by way of example, a displayed image for establishing external command parameters;

FIG. **81** is a view showing, by way of example, a displayed image for establishing NTSC matrix (mix) parameters, the displayed image including a displayed graph;

FIG. **82** is a view showing, by way of example, a displayed image for establishing NTSC matrix (mix) parameters, the displayed image including a displayed graph;

FIG. **83** is a view showing, by way of example, a displayed image for establishing PAL matrix (mix) parameters, the displayed image including a displayed graph;

FIG. **84** is a view showing, by way of example, a displayed image for establishing PAL matrix (mix) parameters, the displayed image including a displayed graph;

FIG. **85** is a view showing, by way of example, a displayed image for establishing PAL matrix (mix) parameters, the displayed image including a displayed graph;

FIGS. **86**A through **86**E are views showing, by way of example, displayed images for processing memory accesses; and

FIG. **87** is a view showing, by way of example, a displayed image for establishing LSI ports.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A method of and an apparatus for setting up an electronic device according to the present invention will be described below with respect to various items thereof which will be given under the headings below in the order named.

A. Arrangement and operation of an electronic device setup system (see FIG. **1**);

B. Operation of the electronic device setup system (see FIG. **2**);

C. Arrangement of a camera setup system (see FIG. **3**);

D. Arrangement of a computer in the camera setup system shown in FIG. **3** (see FIG. **4**);

E. Control operation according to a main routine of the computer shown in FIG. **4** (see FIG. **5**);

F. Initial images produced by an operating system in the computer shown in FIG. **4** (see FIGS. **6**A and **6**B);

G. Connection configuration window which is displayed at first when the camera setup system shown in FIG. **3** starts to operate (see FIG. **7**);

H. Parameter icon window of the camera setup system (see FIG. **8**);

I. Main pull-down menus which can be displayed from a menu bar in the connection configuration window of the camera setup system (see FIGS. **9**A through **9**F);

J. Pull-down menus for a CHU (camera head unit) of the camera setup system (see FIGS. **10**A through **10**C and FIGS. **11**A and **11**B);

K. Pull-down menus for a CCU (camera control unit) or the camera setup system (see FIGS. **12**A through **12**D);

L. Basics of a parameter setting window of the camera setup system (see FIG. **13**);

M. A main processing sequence of the camera setup system (see FIGS. **14** through **16**);

N. A setup process of the camera setup system (see FIGS. **17** and **18**);

O. A change process with a switch of the camera setup system (see FIG. **19**);

P. A change process with a slide lever of the camera setup system (see FIG. **20**);

Q. A change process with a numerical value of the camera setup system (see FIG. **21**);

R. A change process with a waveform of the camera setup system (see FIG. **22**);

S. A transmission data format and file formats used in the camera set up system (see FIGS. **23**A through **23**E);

T. A data converter in the camera setup system shown in FIG. **3** (see FIG. **24**);

U. A control sequence of the data converter shown in FIG. **24** (see FIGS. **25** through **27**);

V. A video system of a camera shown in FIG. **3** (see FIG. **28**);

W. An audio system of a camera shown in FIG. **3** (see FIG. **29**);

X. Displayed images for establishing parameters in the camera setup system (see FIGS. **30**A and **30**B through **87**).

A. Arrangement and Operation of an Electronic Device Setup System (see FIG. **1**)

FIG. **1** shows in block form an electronic device setup system for setting up an electronic device, which embodies a method of and an apparatus for setting up an electronic device according to the present invention.

Connections and Structure

The electronic device setup system shown in FIG. **1** comprises a controller **1** for establishing parameters of a controlled device **13**, a display unit **6** for displaying a parameter setting image **7** for use in establishing parameters of the controlled device **13**, an external memory **8** for storing the data of the parameter setting image **7**, a data input unit **10** for entering input data to establish parameters into the controller **1**, a position indicator **11** for indicating the position of a pointer in the parameter setting image **7**, a protocol converter **12** for converting a communication protocol for parameter data from the controller **1** into a communication protocol that can be received by the controlled device **13**, and the controlled device **13** which automatically establishes parameters of its own according to parameter data transmitted prom the controller **1** through the protocol converter **12**.

The controller **1** comprises a parameter setting image display device **2** for displaying the parameter setting image **7** on the display unit **6**, an input value recognizer **4** for recognizing an input value represented by input data entered from the data input unit **10**, a position recognizer **3** for recognizing the position of a pointer, indicated by positional data from the position indicator **11**, in the parameter setting image **7** which is being displayed on the display unit **6**, and a parameter data generator **5** for generating or modifying parameter data represented by the parameter setting image **7** displayed on the display unit **6**, based on the input data entered from the data input unit **10** or the positional data entered from the position indicator **11**.

The parameter setting image **7** comprises an image group **7***a* for displaying a setting status based on parameter settings, and a switch image group **7***b* for changing parameters. The image group **7***a* comprises graphic images such as tables, graphs, or the like which correspond to the parameters of the controlled device **13**, and the switch image group **7***b* comprises visual switch images.

The electronic device setup system has two operation modes. In one of the operation modes, the displayed state of the image group **7***a* for parameter values and parameter settings is changed when the displayed state of the switch image group **7***b* is changed by the data input unit **10** or the position indicator **11**.

Specifically, when input data are entered from the data input unit **10** or positional data are entered from the position indicator **11**, the switch image group **7***b* displayed on the display unit **6** is changed depending on the entered input data or positional data as if a real switch or lever were moved by the operator, and the parameter data generator **5** generates or modifies the corresponding parameter data for changing the displayed state of the image group **7***a*.

In the other operation mode, the displayed state of the image group **7***a* is changed by the data input unit **10** or the position indicator **11**, the parameter values and the displayed state of the switch image group **7***b* is changed.

Specifically, when input data are entered from the data input unit **10** or positional data are entered from the position indicator **11**, the image group **7***a* displayed on the display unit **2** is changed depending on the entered input data or positional data, the corresponding parameter data are generated or modified by the parameter data generator **5**, and the displayed state of the switch image group **7***b* is changed. Thus, the input data entered from the data input unit **10** or the positional data entered from the position indicator **11** are used as parameter setting information as shown in FIG. **1**.

The protocol converter **12** is indicated by the broken line in FIG. **1** because the protocol converter **12** will not be required if a protocol converting process is carried out by the controlled device **13** rather than the protocol converter **12**. Stated otherwise, the protocol converter **12** is required only if the controlled device **13** is incapable of carrying out a protocol converting process.

For the sake of brevity, image data for selecting parameters are omitted from illustration. A parameter selection image is an image for selecting the setting of a parameter among many parameters of the controlled device **13**, and its data are held in the external memory **8**.

Operation

When a parameter of the controlled device **13** is selected by the data input unit **10** or the position indicator **11**, the controller **1** reads parameter setting image data **9** corresponding to the selected parameter from the external memory **8** as indicated by the solid-line arrow Y**1**, and supplies the read parameter setting image data **9** to the display unit **6** as indicated by the solid-line arrow Y**2**. The display unit **6** displays on its display panel a parameter setting image **7** represented by the parameter setting image data **9**.

Then, when input data are entered from the data input unit **10** as indicated by the solid-line arrow Y**3**, the input value recognizer **4** recognizes the value of the entered input data. When positional data are entered from the position indicator **11**, the position recognizer **3** recognizes the position of a pointer in the parameter setting image **7**, which corresponds to the entered positional data.

Based on the pointer position recognized by the position recognizer **3** and the value of the entered input data recognized by the input value recognizer **4**, the parameter setting image display device **2** changes corresponding data of the parameter setting image data **9** representing the parameter setting image **7** displayed on the display unit **2**, i.e., data of the image group **7***a* and data of the switch image group **7***b*, and supplies the changed parameter setting image data **9** to the display unit **6** as indicated by the solid-line arrow Y**2**,

thereby changing the displayed state of the image group **7***a* and the switch image group **7***b* on the display unit **2**.

The parameter data generator **5** generates or modifies parameter data based on the pointer position recognized by the position recognizer **3** and the value of the entered input data recognized by the input value recognizer **4**, and supplies the generated or modified parameter data to the protocol converter **12** as indicated by the solid-line arrow **Y4**.

The protocol converter **12** converts the communication protocol of the parameter data supplied from the controller **1** into a communication protocol which can be received by the controlled device **13**. The parameter data converted by the protocol converter **12** are supplied therefrom to the controlled device **13** as indicated by the solid-line arrow **Y5**. The controlled device **13** changes the corresponding value of parameters of its own using the parameter data supplied from the protocol converter **12**.

B. Operation of the Electronic Device Setup System (see FIG. **2**)

FIG. **2** shows an operation sequence of the an electronic device setup system shown in FIG. **1**. The operation sequence comprises steps Sa**1**~Sa**8** which are executed by the controller **1**, steps Sb**1**~Sb**11** which are executed by the protocol converter **12**, and steps Sc**1**~Sc**13** which are executed by the controlled device **13**. The greater the numerals contained in the reference characters which denote the above steps, the more subsequent the corresponding steps are in the entire operation sequence.

B1. Processing Operation of the Controller **1**

In the step Sa**1**, the parameter setting image display device **2** reads parameter selecting image data from the external memory **8**, and supplies the read parameter selecting image data to the display unit **6**. The display unit **6** now displays on its display panel a parameter selection image for selecting one or more of many parameters of the controlled device **13**. Thereafter, control proceeds to the step Sa**2**.

In the step Sa**2**, the position recognizer **3** and the input value recognizer **4** decide whether parameter setting information is entered from the data input unit **10** and the position indicator **11**. If parameter setting information is entered (YES), then control proceeds to the step Sa**3**.

In the step Sa**3**, the parameter setting image display device **2** reads parameter setting image data **9** corresponding to the selected parameter or parameters from the external memory **8** based on the data recognized by the position recognizer **3** and the input value recognizer **4**, and supplies the read parameter setting image data **9** to the display unit **6**. The display unit **6** now displays on its display panel a parameter setting image represented by the supplied parameter setting image data **9**. Thereafter, control proceeds to the step Sa**4**.

In the step Sa**4**, the position recognizer **3** and the input value recognize **4** decide whether parameter setting information is entered from the data input unit **10** and the position indicator **11**. If parameter setting information is entered (YES), then control proceeds to the step Sa**5**.

In the step Sa**5**, the parameter data generator **5** generates or modifies parameter data based on the data recognized by the position recognizer **3** and the input value recognizer **4**. Then, control proceeds to the step Sa**6**.

In the step Sa**6**, the parameter setting image display device **2** changes the image, displayed on the display unit **2**, of the corresponding displayed data. Then, control proceeds to the step Sa**7**.

In the step Sa**7**, the parameter setting image display device **2** transmits the parameter data to the protocol converter **12**. Then, control proceeds to the step Sa**8**.

In the step Sa**8**, the position recognizer **3** and the input value recognizer **4** decide whether the entering of parameter setting information is from the data input unit **10** and the position indicator **11** is finished or not. If the entering of parameter setting information is finished (YES), then the processing comes to an end.

B2. Processing Operation of the Protocol Converter **12**

In the step Sb**1**, the protocol converter **12** is held in a standby condition. Then, control proceeds to the step Sb**2**.

In the step Sb**2**, the protocol converter **12** decides whether parameter data are transmitted from the controller **1** or not. If parameter data are transmitted (YES), then control proceeds to the step Sb**9**. If parameter data are not transmitted (NO), then control returns to the step Sb**1**.

In the step Sb**9**, the protocol converter **12** receives the parameter data transmitted from the controller **1**. Then, control proceeds to the step Sb**10**. The step number jumps from "2" in the step Sb**2** to "9" in the step Sb**9** because the numerals contained in the steps represent the operating sequence and the step Sb**9** is carried out after the step Sa**7**.

In the step Sb**10**, the protocol converter **12** converts the communication protocol of the parameter data received in the step Sb**9** into a communication protocol which can be received by the controlled device **13**. Then, control proceeds to the step Sb**11**.

In the step Sb**11**, the protocol converter **12** transmits the converted parameter data to the controlled device **13**. Thereafter, control goes back to the step Sb**1**.

B**3**. Processing Operation of the Controlled Device **13**

In the step Sc**1**, the controlled device **13** is held in a standby condition. Then, control proceeds to the step Sc**2**.

In the step Sc**2**, the controlled device **13** decides whether parameter data are transmitted from the protocol converter **12** or not. If parameter data are transmitted (YES), then control proceeds to the step Sc**12**. If parameter data are not transmitted (NO), then control returns to the step Sc**1**.

In the step Sc**12**, the controlled device **13** receives the parameter data transmitted from the protocol converter **12**. Then, control proceeds to the step Sc**13**. The step number jumps from "2" in the step Sc**2** to "12" in the step Sc**12** because the numerals contained in the steps represent the operating sequence and the step Sc**12** is carried out after the step Sb**11**.

In the step Sc**13**, the controlled device **13** changes the value of the parameter or parameters of a corresponding circuit or circuits based on the received parameter data. Then, control goes back to the step Sc**1**. Advantages offered by the electronic device setup system shown in FIGS. **1** and **2**.

As described above, for establishing a parameter or parameters of the controlled device **13** with the controller **1**, the electronic device setup system operates in either an operation mode in which the displayed state of the image group **7***a* is changed when the displayed state of the switch image group **7***b* is changed by the data input unit **10** or the position indicator **11**, or an operation mode in which the displayed state of the switch image group **7***b* is changed when the displayed state of the image group **7***a* is changed by the data input unit **10** or the position indicator **11**, for thereby changing the parameter or parameters in a graphical environment. Consequently, the environment for establishing parameters is improved, and the operator is prevented from changing parameters in error and allowed to confirm changed parameters.

Specific details of the method of and the apparatus for setting up an electronic device according to the present invention will be described below.

C. Arrangement and Operation of a Camera Setup System (see FIG. **3**)

FIG. **3** shows in block form a camera setup system which incorporates the principles of the electronic device setup system shown in FIG. **1**.

Connections and Structure

The camera setup system shown in FIG. **3** comprises a display unit **50** for displaying a parameter setting image **51** and a monitor image **52**, a computer **100**, a keyboard **250**, a pointing device **300**, a disk drive **350** for storing data of the parameter setting image **51** and program data, a data converter **400** for converting the protocol of data transmitted from the computer **100**, a system controller **1100**, a plurality of controllers **1200-1**, . . . , **1200-*n*** (one shown) connected to the system controller **1100**, and a plurality of cameras **1000** (one shown) connected respectively to the controllers **1200-1**, . . . , **1200-*n***. The system controller **1100** serves to supply data outputted from the data converter **400** selectively to the controllers **1200-1**, . . . , **1200-*n*** and the cameras **1000**.

The computer **100** and the disk drive **350** are interconnected by a cable CA**1**. The computer **100** and the data converter **400** are interconnected by a cable CA**2**. The data converter **400** and the system controller **1100** are interconnected by a cable CA**3**. The system controller **1100** and the controllers **1200-1**, . . . , **1200-*n*** are interconnected by cables CA**4**. The controllers **1200-1**, . . . , **1200-*n*** and the cameras **1000** are interconnected by cables CA**5**. The computer **100** and the cameras **1000** are interconnected by cables CA**6**.

The parameter setting image **51** corresponds to the parameter setting image **7** shown in FIG. **1**. The display unit **50** corresponds to the display unit **6** shown in FIG. **1**. The computer **100** corresponds to the controller **1** shown in FIG. **1**. The keyboard **250** corresponds to the data input unit **10** shown in FIG. **1**. The pointing device **300** corresponds to the position indicator **11** shown in FIG. **1**. The disk drive **350** corresponds to the external memory **8** shown in FIG. **1**. The data converter **400** corresponds to the protocol converter **12** shown in FIG. **1**. The controllers **1200-1**, . . . , **1200-*n*** and the cameras **1000** correspond to the controlled device **13** shown in FIG. **1**.

As with the protocol converter **12** shown in FIG. **1**, the data converter **40** may be dispensed with if the system controller **1100** has a protocol conversion capability.

Each of the controllers **1200-1**, . . . , **1200-*n*** is generally referred to as a CCU (Camera Control Unit). These controllers **1200-1**, . . . , **1200-*n*** serve to control the cameras **1000** and handle part of a signal processing operation for processing video and audio signals produced by the cameras **1000**.

Camera systems which comprise the controllers **1200-1**, . . . , **1200-*n*** and the cameras **1000** are not used as single systems as is the case with VTRs integral with video cameras for home use. For this reason, each of the cameras **1000** is referred to as a CHU (Camera Head Unit) in broadcasting stations.

In FIG. **3**, each of the camera systems in the camera setup system comprises a CCU and a CHU. However, the camera setup system may be used with respect to a video camera which is used as a single unit. In such a modification, the controllers **1200-1**, . . . , **1200-*n*** may be dispensed with.

The pointing device **300** may comprise a digitizer, a mouse, a track ball, a cursor key, a joy stick, or the like, for example.

Each of the cameras **1000** has a video system **500** and an audio system **600** disposed inside of its housing, and also has an LCD (Liquid Crystal Display) unit **700**, a control key group **750**, a lens assembly **800**, and a microphone **850** mounted on its housing.

The disk drive **350** should preferably comprise a hard disk drive in view of its high access speed. Of course, the disk drive **350** may comprise an optical disk drive employing an recordable and reproducible optical disk which also has a relatively high access speed, or a magnetic disk drive.

The monitor image **52** is displayed on the display unit **50** based on a video signal captured by each of the cameras **1000**.

Operation

When a parameter or parameters are selected, the computer **100** reads parameter setting image data stored in the disk drive **350**. The parameter setting image data read from the disk drive **350** are supplied through the cable CA**1** and the computer **100** to the display unit **50**, which displays the parameter setting image **51** on its display panel based on the supplied parameter setting image data.

When a parameter change is indicated in the parameter setting image **51** by the keyboard **250** or the pointing device **300**, the computer **100** changes parameter data and the displayed state of a corresponding portion of the parameter setting image **51** based on the controlling information from the keyboard **250** or the pointing device **300**.

The computer **100** transmits the changed parameter data (absolute data) or data (relative data) indicative of the change through the cable CA**2** to the data converter **400**. The parameter data or the data indicative of the change which are supplied to the data converter **400** are converted in protocol, and then supplied to the system controller **1100**, which supplies the data to one of the controllers **1200-1**, . . . , **1200-*n*** or more of the cameras **1000**.

The manner in which the system controller **1100** recognizes one of the controllers **1200-1**, . . . , **1200-*n*** or one of the cameras **1000** to which it should transmit the data will be described later on with respect to a data transmission format with reference to FIGS. **23**A through **23**E.

While parameters are being established with respect to one of the controllers **1200-1**, . . . , **1200-*n*** or one of the cameras **1000** based on the parameter data, an output video signal from the camera **1000** is supplied to the computer **100**. Alternatively, an output video signal from one of the controllers **1200-1**, . . . , **1200-*n*** may be supplied to the computer **100**.

After the output video signal from the camera **1000** is supplied to the computer **100**, it is supplied to the display unit **50**, which then displays the monitor image **52** based on the supplied output video signal.

Internal arrangements and operations of the individual components of the camera setup system shown in FIG. **3** will be described below.

D. Arrangement of the Computer **100** in the Camera Setup System Shown in FIG. **3** (see FIG. **4**)

FIG. **4** shows in block form the computer **100** in the camera setup system shown in FIG. **3**.

Connections and Structure

The computer **100** comprises a CPU **101**, a bus assembly **102** connected to the CPU **101** and comprising address, data, and control buses, a ROM (Read-Only Memory) **103** connected to the bus assembly **102** for storing a basic input/output control system, etc., a working RAM (Random-Access Memory) **104** connected to the bus assembly **102**, a VRAM (Video Random-Access Memory) **105** connected to the bus assembly **102** for storing video images to be displayed, and an input/output port **106** connected to the bus assembly **102**. To the input/output port **106**, there are connected a floppy disk interface **108** connected to a floppy disk

drive **107**, an IC card interface **110** connected to a card slot **109**, a pointing device interface **111** connected to an input/output terminal **112** which is coupled to the pointing device **300** shown in FIG. **3**, a keyboard interface **113** connected to an input/output terminal **114** which is coupled to the keyboard **250** shown in FIG. **3**, an image display accelerator **115** for controlling the display of images instead of the CPU **101**, the image display accelerator **115** being connected to an output terminal **116** which is coupled to the display unit **50** shown in FIG. **3**, a video capture unit **117** for capturing video images, the video capture unit **117** being connected to an input terminal **118** which is coupled to the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** shown in FIG. **3**, a communication interface **119** connected to an input/output terminal **120** which is coupled to the data converter **400** shown in FIG. **3**, a SCSI (small Computer Systems Interface) **121** connected to an input/output terminal **122** which is coupled to the disk drive **350** shown in FIG. **3**, and an audio input/output circuit **123** connected to an input terminal **125** which is coupled to the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** shown in FIG. **3**. A loudspeaker **124** is connected to the audio input/output circuit **123**.

The communication interface **119** may comprise an RS-232C interface or an RS-422 interface, for example. The image display accelerator **115** is capable of displaying images with 1280×1024 dots in 16770 thousand colors on the display unit **50** shown in FIG. **3**.

When the computer **100** is turned on, the CPU **101** reads a basic input/output control system **126** (BIOS) which is stored in the ROM **103**, and then reads program data of an operating system from the disk drive **350** shown in FIG. **3**, and further reads program data of drivers.

When a camera setup system (described later on) is selected on a displayed image of the operating system, the CPU **101** reads program data of the camera setup system from the disk drive **350**. Blocks enclosed in a rectangular frame which is indicated by the dot-and-dash line represent functions of the CPU **101** which can be performed by the basic input/output control system, the operating system, the drivers, and the camera setup system which are resident in a main memory of the CPU **101**.

The basic input/output control system **126** serves to control input and output data, e.g., to receive and recognize input data from the keyboard **250**, to receive and recognize positional data from the pointing device **300**, and to send display data to the display unit **50**. The basic input/output control system **126** is normally stored as a conversion table in the ROM **103**. In this embodiment, however, the basic input/output control system **126** is resident in the main memory of the CPU **101**.

An IC card driver **127** allows the computer **100** to send data to and receive data from an IC card which is inserted in the card slot **109**. An accelerator driver **128** permits data to be transmitted between the computer **100** and the image display accelerator **115**. A video capture driver **130** permits data to be transmitted between the computer **100** and the video capture unit **117**. An audio driver **131** permits data to be transmitted between the computer **100** and the audio input/output circuit **123**.

An operating system **129** should preferably comprise an operating system capable of managing file data, controlling the disk drive **350**, and otherwise providing a graphical user interface. For example, the operating system **129** may comprise an operation system such as MS-WINDOW provided by Microsoft, SYSTEM 7.5 provided by Apple Computer, or OS/2 provided by IBM. Alternatively, an operating system with no graphical user interface may be realized by the above camera setup systems.

The other functions include an instruction analyzer **132**, a command analyzer **133**, a display controller **134**, a parameter controller **138**, a command generator **139**, a file manager **140**, and an arithmetic unit **141** which are performed by the camera setup system.

The instruction analyzer **132** is capable of analyzing instructions based on input data from the pointing device interface **111** and the keyboard interface **113**.

The command analyzer **132** is capable of analyzing commands in input data from the interface **119**.

The display controller **134** is capable of changing data stored in the VRAM **105** according to instructions analyzed by the instruction analyzer **132**.

The parameter controller **138** is capable of changing parameter data according to instructions analyzed by the instruction analyzer **132**.

The command generator **139** is capable of transmitting parameter data or data indicative of changes through the interface **119** and the input/output terminal **120** to the controllers **1200-1**, . . . , **1200-*n*** or the cameras **1000**, and also of issuing commands.

The file manager **140** is capable of holding and managing files of parameter data for the controllers **1200-1**, . . . , **1200-*n*** and the cameras **1000**.

The arithmetic unit **141** is capable of carrying out arithmetic operations for changing parameter data and display data according to instructions analyzed by the instruction analyzer **132**.

Operation of the computer **100** shown in FIG. **4** will be described in detail later on with reference to FIGS. **6**A, **6**B through **23**A–**23**E.

E. Control Operation According to a Main Routine of the Computer **100** Shown in FIG. **4** (see FIG. **5**)

FIG. **5** shows a control sequence according to a main routine of the computer **100** shown in FIG. **4**. The control sequence is started when the computer **100** is turned on.

In a step **S101**, an initializing program stored in the ROM **103** is read, and causes the CPU **101** to check a connected device. Then, control proceeds to a step **S102**.

In the step **S102**, the CPU **101** initializes the RAM **104** and the VRAM **105**. Thereafter, control proceeds to a step **S103**.

In the step **S103**, the basic input/output control system **126** starts to operate. Then, control proceeds to a step **S104**.

In the step **S104**, the basic input/output control system **126** reads the program data of the operating system **129** from the disk drive **350**, thereby starting the operating system **129**. Then, control proceeds to a step **S105**.

In the step **S105**, the operating system **129** reads the program data of the IC card driver **127**, the accelerator driver **28**, the video capture unit **130**, and the audio driver **131** from the disk drive **350**, and starts the IC card driver **127**, the accelerator driver **128**, the video capture unit **130**, and the audio driver **131**. Then, control proceeds to a step **S106**.

In the step **S106**, the operating system **129** confirms the camera setup system. Then, control proceeds to a step **S107**. Specifically, the operating system **129** confirms the camera setup system by reading information relative to the program data registered in the operating system **126** from files which are owned by the operating system **126**. For example, such information includes information indicating that the camera setup system is registered as a starting program and information as to icons of the camera setup system.

In the step **S107**, the operating system **129** writes image data of the operation system **129** in the VRAM **105**. The

image data of the operating system **129** written in the VRAM **105** are supplied through the image display accelerator **115** and the output terminal **116** to the display unit **50**. Thereafter, control proceeds to a step S**108**.

If the camera setup system is registered with respect to the operating system **129**, an icon indicative of the camera setup system is also displayed.

In the step S**108**, the operating system **129** decides whether the camera setup system is selected or not. If the camera setup system is selected (YES), then control proceeds to a step S**150**. If the camera setup system is not selected (NOT), then control jumps to a step S**109**.

The camera setup system is selected when the pointer image of the pointing device **300** is superposed on the icon of the camera setup system in the image of the operating system **129** displayed on the display unit **50** and also when the pointing device **300** is double-clicked by the operator. The pointing device **300** is double-clicked when a button on the pointing device **300** is pressed successively twice by the operator.

In the step S**150**, the processing operation of the camera setup system is executed. Then, control goes to the step S**109**.

In the step S**109**, the operating system **129** decides whether a setup program of the camera setup system is finished or not. If the setup program is finished (YES), then control proceeds to a step S**110**. If the setup program is not finished (NO), then control returns to the step S**150**.

In the step S**110**, the operating system **129** decides whether its operation is finished or not. If the operation of the operating system **129** is finished (YES), then control proceeds to a step S**111**. If the operation of the operating system **129** is not finished (NOT), then control goes back to the step S**107**.

In the step S**111**, the operating system **129** is finished by making itself non-resident in the main memory of the CPU **101**.

F. Initial Images Produces by the Operating System **129** in the Computer **100** Shown in FIG. **4** (see FIGS. **6**A and **6**B)

FIG. **6**A shows a window image Wa in an uppermost layer produced by the operating system **129**, and FIG. **6**B shows the manner in which the camera setup system is started.

In FIG. **6**A, the window image Wa is composed of a button image CB for displaying a pull-down menu of the system, a button image IB for iconizing the window image Wa, a button image EB for enlarging the window image Wa, a menu bar MBa for entering various instructions into the operating system **129**, and various icon images including an icon ICa of the camera setup system.

The menu bar MBa has a plurality of menu images representing menus "ICON", "OPTION", "WINDOW", and "HELP". When one of the menu images is selected, it displays a pull-down menu comprising related commands. To Select one of the menu images, the operator may press a certain key on the keyboard **250** shown in FIG. **3**, and then press a cursor key on the keyboard **250**. Alternatively, the operator may move the pointing device **300** to bring a pointer Po to a desired one of the words, and then click the word. The operator then selects and clicks a desired one of the commands displayed on the pull-down menu which is displayed as a result of the selection of one of the menu images.

The alphabetic letters in lower case, which are contained in the window image Wa, indicate the levels of layers. The alphabetic letter "a" indicates the highest level of layer, and the alphabetic letters "b", "c", "d", . . . indicate the progressively lower levels of layers. The window image Wa contains the button images CB, IB, EB at all times.

In the window image Wa shown in FIG. **6**A, the pointer Po is moved by the pointing device **300** to a position over the icon ICa marked with "CAMERA SETUP", and thereafter the button on the pointing device **300** is clicked once. Then, as shown in FIG. **6**B, a window image Wb in a next lower layer is displayed on the display unit **50**.

In the window usage Wb shown in FIG. **6**B, the pointer Po is moved by the pointing device **300** to a position over an icon ICb marked with "CAMERA SETUP", and thereafter the button on the pointing device **300** is double-clicked, thereby executing the camera setup system.

G. Connection Configuration Window Which is Displayed at First When the Camera Setup System Shown in FIG. **3** Starts to Operate (see FIG. **7**)

FIG. **7** shows a connection configuration window which is displayed at first when the camera setup system shown in FIG. **3** starts to operate.

A window image Wc shown in FIG. **7** is displayed when a file of connection configuration information is read which was generated when the camera setup system started the last time. The window image Wc contains icon images Ca**1**~Ca**6** of cameras, icon images Cu**1**~Cu**6** of CCUs connected respectively to the icon images Ca**1**~Ca**6**, an icon image Cn**1** of a CNU (Camera Network Unit) which is connected to the icon images Cu**1**~Cu**6**, an icon image Vc**1** of a VCS (Video Camera Selector) connected to the icon image Cn**1**, and a menu bar MBc which contains menus "FILE", "EDIT", "SETUP", and "HELP".

The window image Wc indicates that a camera system composed of six cameras, six CCUs connected respectively to the six cameras, a CNU connected to the six CCUs, and a VCS connected to the CNU is to be set up. As described later on, the connected configuration has been confirmed by the camera setup system when the camera setup system has been started. An object with respect to which parameters are to be established is one of the icon images Ca**1**~Ca**6** of cameras and the icon images Cu**1**~Cu**6** of CCUs.

In order to establish parameters with respect to a desired camera or CCU, the pointer Po is controlled by the pointing device **300** to move to a position over one of the icon images Ca**1**~Ca**6** of cameras and the icon images Cu**1**~Cu**6** of CCUs, and thereafter the button of the pointing device **300** is clicked once. When the button of the pointing device **300** is clicked once, the selected one of the icon images Ca**1**~Ca**6** of cameras and the icon images Cu**1**~Cu**6** of CCUs is colored or displayed in a certain display state, indicating that it is selected. In FIG. **7**, the icon image Ca**4** of a camera is selected.

The CNU corresponds to the system controller **1100** shown in FIG. **3**. The VCS serves to selectively output six video signals that are supplied through the CNU.

H. Parameter Icon Window of the Camera Setup System (see FIG. **8**)

FIG. **8** shows a window image Wd which is displayed when one of the icon images Ca**1**~Ca**6** of cameras in the connection configuration window Wc shown in FIG. **7** is selected by clicking once the button of the pointing device **300** and thereafter the button of the pointing device **300** is clicked once, or when the button of the pointing device **300** is double-clicked while the pointer Po is placed over one of the icon images Ca**1**~Ca**6** of cameras in the connection configuration window Wc.

The image window Wd contains camera parameters that can be set up as icon images. A process of setting up a desired one of the parameters can be started when the pointer Po is placed over the desired parameter by the pointing device **300** and thereafter the button of the pointing device **300** is double-clicked.

The parameters represented by the respective icon images will be described below.

Shutter

This is a parameter for adjusting the shutter speed of an electronic shutter. There are available two adjustment modes including a shutter mode of stepwise switching operation and an adjustment mode for adjusting a vertical resolution.

Filter

This is a parameter for adjusting an ND filter or a CC filter to a suitable filter in order to obtain a suitable depth of field through the color temperature or brightness of illumination.

Bars/Test

This is a parameter for establishing the output of a test signal or the output of color bars from the camera.

Automatic Setup

This is a parameter for controlling the automatic adjustment of white balance, black balance, white shading, black shading, master black level, gamma level, and knee level.

Iris

This is a parameter for adjusting the iris position (aperture) of the lens.

M Black (Master Black)

This is a parameter for adjusting the black level of a video output signal.

M Gain (Black Gain)

This is a parameter for adjusting the master gain of a video output signal depending on the illuminance of the subject to be imaged by the camera.

Knee SAT (Knee Saturation)

This is a parameter for controlling the compression of the level of only a luminance in a video signal.

M V MOD (Master V Modulation)

This is a parameter for adjusting the vertical modulating shading through simultaneous adjustment of primary color signals.

Knee

This is a parameter for controlling the compression of the level of a high-luminance portion of an input signal at the time the level of the input signal in the camera exceeds a certain value.

White Clip

This is a parameter for adjusting the limitation on the peak of a white level of the video signal.

Detail Level

This is a parameter for adjusting the corrective quantity for a corrective signal to emphasize the edge of the video signal.

H/V, H/L Ratios

These are parameters for adjusting the proportions of horizontal and vertical detail levels and adjusting the burst frequency of detail.

γ Mix Ratio

This is a parameter for adjusting the mixing ratio of corrective signals to emphasize the edge of the video signal before and after gamma correction.

R/G/B Mix Ratio

This is a parameter for adjusting the mixing ratio of signals from which to generate the corrective signal to emphasize the edge of the video signal.

Slim Detail

This is a parameter for adjusting the thickness of the edge with the corrective signal to emphasize the edge of the video signal.

Slant Detail

This is a parameter for adjusting the edge in an oblique direction with the corrective signal to emphasize the edge of the video signal.

H Limiter

This is a parameter for adjusting a level at which a limiter works for suppressing the white and black levels of the video signal, with respect to the corrective signal to emphasize the edge in a horizontal direction.

V Limiter

This is a parameter for adjusting a level at which a limiter works for suppressing the white and black levels of the video signal, with respect to the corrective signal to emphasize the edge in a vertical direction.

Knee Apt (Knee Aperture)

This is a parameter for adjusting the corrective quantity for the corrective signal to emphasize the edge of the video signal whose level is higher than a level for controlling the compression of the level of the high-luminance portion of the input signal at the time the level of the input signal exceeds a certain value.

Level Dep (Level Depend)

This is a parameter for adjusting the level of the corrective signal to emphasize the edge with respect to signals greater than a knee point.

Crispening

This is a parameter for adjusting the level of the corrective signal to emphasize the edge in order to remove the edge of a noise potion of the video signal.

Detail Area

This is a parameter for adjusting the area and its gain on the display screen which is corrected by the corrective signal to emphasize the edge.

Skin Tone

This is a parameter for adjusting the level of the corrective signal to emphasize the edge of the subject having a particular hue and saturation, of the video signal.

Black

This is a parameter for adjusting the black levels of the primary color signals in order to determine a black balance in each channel of the primary color signals.

White

This is a parameter for adjusting the white levels of the primary color signals in order to determine a white balance in each channel of the primary color signals.

Black Set

This is an adjusting parameter for making constant the black level which is a reference for each channel of the primary color signals.

Flare

This is a parameter for adjusting a flare balance of each channel of the primary color signals.

B SH H (Black Shading H)

This is a parameter for adjusting a horizontal black shading for each channel of the primary color signals.

B SH V (Black Shading V)

This is a parameter for adjusting a vertical black shading for each channel of the primary color signals.

W SH H (White Shading H)

This is a parameter for adjusting a horizontal white shading for each channel of the primary color signals.

W SH V (White Shading V)

This is a parameter for adjusting a vertical white shading for each channel of the primary color signals.

V MOD SH (V Modulation Shading)

This is a parameter for adjusting a vertical modulation shading for each channel of the primary color signals.

Matrix

This is an adjusting parameter for correcting fundamental colors of primary color signals to obtain an optimum color tone.

Gamma

This is a parameter for adjusting the gamma correction to correct nonlinear characteristics which is exhibited by a television cathode-ray tube when electric signals supplied thereto are converted into light.

Black Gamma

This is a parameter for adjusting the black gamma to improve gradation characteristics in the vicinity of the black level.

Transmit

This is a parameter for selecting a transmission method between the camera and the CCU.

Mic/Line

This is a parameter for selecting an input method for inputting an audio signal to the camera through a microphone or a line.

Matrix Mix

This is a parameter for establishing a mixing signal and a mixing ratio with respect to an external audio signal to be inputted to the camera.

Matrix Output

This is a parameter for selecting a program signal in the camera and adjusting the output level of the external audio signal.

Incom

This is a parameter for establishing an external audio signal to be inputted to the camera.

Tracker

This is a parameter for establishing an external audio signal to be inputted to the camera.

Ext Comm (External Command)

This is a parameter for establishing an ON or OFF response to an external command which is supplied to the camera.

I. Main Pull-Down Menus of the Camera Setup System (see FIGS. **9**A through **9**F)

FIGS. **9**A through **9**F show main pull-down menus which can be displayed when the pointer Po is placed over menus "FILE", "EDIT", "SETUP", "HELP" on the menu bars MBc, MBd in the window image Wc shown in FIG. **7** and the window image Wd shown in FIG. **8** and then the button of the pointing device **300** is clicked.

FIG. **9**A shows a pull-down menu which is displayed when the menu "FILE" is selected. When the menu "FILE" is selected, commands that can be selected from the menu "FILE" are as follows:

Upload

This is a command for reading all parameter data from the camera or the CCU that is connected.

Download

This is a command for setting all parameter data in the camera or the CCU that is connected.

Load

This is a command for reading all parameter data stored as a file from a floppy disk in the floppy disk drive **107** shown in FIG. **4**, the disk drive **350** shown in FIG. **3**, or an IC card in the card slot **109** shown in FIG. **4**.

Save

This is a command for saving parameter data as a file in a floppy disk in the floppy disk drive **107** shown in FIG. **4**, the disk drive **350** shown in FIG. **3**, or an IC card in the card slot **109** shown in FIG. **4**.

Save As

This is a command for saving a file which has been read as a file under a different name.

Page Setup

This is a command for establishing various page information for files.

Print

This is a command for printing file data with a printer.

Exit

This is a command for leaving the selection node on this pull-down menu.

Each of the above commands on the pull-down menu shown in FIG. **9** can be selected by placing the pointer Po over the command while the button of the pointing device **300** is being pressed and thereafter releasing the button of the pointing device **300**. This selecting method is used to select a command, an item, or a parameter on all the pull-down menus.

FIG. **9**B shows a pull-down menu which is displayed when the menu "Edit" is selected. When the menu "Edit" is selected, commands that can be selected from the menu "Edit" are as follows:

Undo

This is a command for undoing a process which has been carried out by a command.

Cut

This is a command for deleting image data in a specified area.

Copy

This is a command for duplicating specified data or image data.

Paste

This is a command for inserting specified data or image data into a desired position.

FIG. **9**C shows a pull-down menu which is displayed when the menu "SETUP" is selected. When the menu "SETUP" is selected, commands that can be selected from the menu "SETUP" are as follows:

User Defined **1**~**4**

These are commands for calling control commands which the user has set for use in the window and carrying out processes according to the called control commands.

Operation Status:

Video Level:

Color:

Detail:

Audio:

The above five commands have pull-down menus in a lower layer.

Memory Access

This is a command for accessing a memory in the camera or the CCU.

File Edit

This is a command for editing file data of read parameter data.

FIG. **9**D shows a pull-down menu which is displayed when the command "Memory Access" shown in FIG. **9**C is selected. When the command "Memory Access" is selected, commands that can be selected are as follows:

CCU

This command has a pull-down menu shown in FIG. **9**D.

FIG. **9**E shows a pull-down menu which is displayed when the command "CHU" shown in FIG. **9**D is selected.

FIG. **9**F shows a pull-down menu which is displayed when the menu "HELP" shown in FIG. **8** is selected. The menu "HELP" serves to display various items of assistive information with respect to the camera setup system.

J. Pull-Down Menus for a CHU of the Camera Setup System (see FIGS. **10**A through **10**C and FIGS. **11**A and **11**B)

FIGS. **10**A through **10**C and FIGS. **11**A and **11**B show pull-down menus which are displayed when a camera is selected in the window image Wc shown in FIG. **7** and thereafter the respective commands "Operation Status",

"Video Level", "Color", "Audio", and "Detail" are selected from the pull-down menu displayed at the time the menu "SETUP" shown in FIG. **9**C is selected. When the parameters on these pull-down menus are selected, they initiate the same processes as when the icon images shown in FIG. **8** are selected. Therefore, the above description of the icon images shown in FIG. **8** should be referred to for details of the parameters on the pull-down menus shown in FIGS. **10**A through **10**C and FIGS. **11**A and **11**B.

K. Pull-Down Menus for a CCU of the Camera Setup System (see FIGS. **12**A through **12**D)

FIGS. **12**A through **12**D show pull-down menus which are displayed when a CCU is selected in the window image Wc shown in FIG. **7** and thereafter the respective commands "Operation Status", "Video Level", "Color", and "Audio" are selected from the pull-down menu displayed at the time the menu "SETUP" shown in FIG. **9**C is selected. When some of the parameters on these pull-down menus are selected, they initiate the same processes as when some of the icon images shown in FIG. **8** are selected.

FIG. **12**A shows a pull-down menu that is displayed when the command "Operation Status" is selected. Parameters that can be selected when the command "Operation Status" is selected are as follows:

Cam Power

This is a parameter for establishing ON and OFF settings for the power supply of the camera.

Bars

This is a parameter for setting the output of color bars from the CCU.

H/SC Phase

This is a parameter for adjusting the phase of a horizontal synchronizing signal and a subcarrier signal.

SeqV Reset (Sequential V Reset)

This is a parameter for adjusting the resetting timing in a sequential output mode for outputting signals to a waveform monitor and a picture monitor.

Skin Gate

This is a parameter for controlling the display of an effective area for skin details displayed on a video monitor.

Prompt

This is a parameter for setting prompts.

Return

This is a parameter for setting a return signal.

Pix Monitor

This is a parameter for setting an output signal to be supplied to a picture monitor.

WF Monitor (Waveform Monitor)

This is a parameter for setting an output signal to be supplied to a waveform monitor.

FIG. **12**B shows a pull-down menu that is displayed when the command "Video Level" is selected. Parameters that can be selected when the command "Video Level" is selected are as follows:

ENC Out (Encoder Out)

This is a parameter for adjusting a composite signal outputted from the CCU.

Camera Out

This is a parameter for adjusting the level of an input signal from the camera.

Component Out

This is a parameter for adjusting a component signal outputted from the CCU.

VBS Level

This is a parameter for adjusting a VBS signal on an option board of a color corrector.

Y Comb

This is a parameter for adjusting a comb filter to reduce cross color of the VBS signal.

FIG. **12**C shows a pull-down menu that is displayed when the command "Color" is selected. Parameters that can be selected when the command "Color" is selected are as follows:

Color Switch

This is a parameter for establishing ON and OFF settings of colors.

Contrast/Saturation

This is a parameter for adjusting the color level of a signal outputted from the CCU and the linearity of a luminance component thereof.

Notch

This is a parameter for establishing a process for removing a signal of a certain frequency from the video signal.

EDTV

This is a parameter for adjusting an item relative to EDTV.

Mono Color

This is a parameter for adjusting a hue with respect to the function of mono color for mixing a chroma signal of a single hue in a luminance signal outputted from the CCU.

Color Correct

This is a parameter for adjusting correcting conditions with respect to a color corrector capable of correcting a particular hue.

Auto Color Matching

FIG. **12**D shows a pull-down menu that is displayed when the command "Audio Level" is selected. Parameters that can be selected when the command "Audio Level" is selected are as follows:

Transmit

This is a parameter for selecting a transmission method between the camera and the CCU.

Mic/Incom

This is a parameter for establishing settings with respect to a microphone and an external audio input signal.

Matrix Mix

This is a parameter for establishing a mixing signal and a mixing ratio with respect to an external audio signal to be inputted to the camera.

Ext Comm (External Command)

This is a parameter for establishing ON and OFF settings with respect to communication of commands with an external source.

L. Basics of a Parameter Setting Window of the Camera Setup System (see FIG. **13**)

FIG. **13** illustrates basics of a parameter setting window We which is displayed as a parameter setting window for setting the parameters of a camera or a CCU which are described above.

The parameter setting window We shown in FIG. **13** is displayed by placing the pointer Po over one of the icon images shown in FIG. **8** and double-clicking the button of the pointing device **300** or placing the pointer Po over one of the commands on the pull-down menus shown in FIGS. **10**A~**10**C through **12**A~**12**D while the button of the pointing device **300** is being pressed and thereafter releasing the button of the pointing device **300**. The monitor image **52** shown in FIG. **3** is omitted from illustration in FIG. **13**.

For illustrative purpose, it is assumed that settings are to be established with respect to an audio signal in the parameter setting window We. The parameter setting window We has an area Ar**1** containing a title image Ti and a button image BU. The title image Ti represents a title "SOLO", indicating that the selected audio signal is outputted singly.

The button BU switches between "ON" and "OFF" each time the button of the pointing device **300** is clicked after the pointer Po is placed on the button BU. That is, various data are established with respect to the button BU, and switched each time the button of the pointing device **300** is clicked. In the illustrated example, the button BU is set to "ON", and hence the title "SOLO" represented by the title image Ti is "ON", i.e., effective.

The parameter setting window we has an area Ar**2** containing a title image Ti and switch images SW represented by numerical values "1"~"5". The title image Ti represents a title "OUTPUT", indicating an "output terminal". The numerical values "1"~"5" indicate the numbers of output terminals for an audio signal. One of the switch images SW is selected by placing the pointer Po over that switch image SW and thereafter clicking the button of the pointing device **300**. At this time, one of the numerical values "1"~"5" which is indicated by the selected switch image SW, i.e., the corresponding number of the output terminal, is selected.

The parameter setting window We has an area Ar**3** containing a slide lever image SL and a numeral image displayed in an area Ar indicated by the broken lines. The slide lever usage SL comprises a lever image Ma and a reference point image P**0** which is displayed at a central position if a value to be set is an absolute value and displayed at a position before being changed if a value to be set is a relative value. The area Ar**3** also displays a numeral image indicating a negative maximum value and a numeral image indicating a positive maximum value, respectively on the opposite ends of the slide lever image SL.

The lever image Ma is moved with the pointing device **300** when the pointing device **300** is moved while the pointer Po is being placed over the lover image Ma and the button of the pointing device **300** is being pressed. The area Ar displays a numerical value depending on the distance which the pointing device **300** is moved.

The parameter setting window we has an area Ar**4** which displays therein a graph corresponding to a parameter being presently set as shown or a waveform image Li when the pointer Po is placed over a button image WBU below the area Ar**4** and thereafter the button of the pointing device **300** is clicked. When the pointer Po is placed over the button image WBU and thereafter the button of the pointing device **300** is clicked again, the waveform image Li displayed in the area Ar**4** disappears.

It should be noted that when the pointing device **300** is moved up and down while the button of the pointing device **300** is pressed with the pointer Po placed over a circular point P indicated by the broken line on the waveform image Li, the waveform image Li is also moved up and down as indicated by the solid-line arrow, and that when the waveform image Li is thus moved up and down, the value of the parameter data held in the computer varies, the lever Ma of the slide lever image SL moves, and the numeral image displayed in the area Ar varies. This process is controlled by the instruction analyzer **132**, the display controller **134**, and the parameter controller **138** shown in FIG. **4**.

The operator can thus control the parameters of the cameras and the CCUs with tho camera setup system which has a graphical user interface as shown in FIG. **13**.

Displayed examples of the parameter setting image We which correspond to the respective parameters will be described later on with reference to FIGS. **30** through **87**. In those displayed examples of the parameter setting image We, only the parameters differ, but the basic method of using the button BU, the switch images SW, the numeral image in the area Ar, the slide lever image SL, the waveform image Li, and the button image WBU, and the basis processing carried out when these images are controlled by the pointing device **300** remain the same. Therefore, those basic method and processing which have been described above with respect to FIG. **13** will not be repeated in the description of displayed examples of the parameter setting image We shown in FIGS. **30** through **87**.

M. A Main Processing Sequence of the Camera Setup System (see FIGS. **14** through **16**)

FIGS. **14** through **16** shows a main processing sequence of the camera setup system in the step S**150** shown in FIG. **5**.

In a step S**151** shown in FIG. **14**, the parameter controller **138** shown in FIG. **4** initializes the RAM **103**, etc. Also in the step S**151**, the file manager **140** reads the image data of the connection configuration window shown in FIG. **7** from the disk drive **350** shown in FIG. **3**. The display controller **134** writes the image data of the connection configuration window in the VRAM **105**. The image data of the connection configuration window written in the VRAM **105** are supplied through the image display accelerator **115** and the output terminal **116** to the display unit **50**, which displays the connection configuration window on its display panel. Then, control proceeds to a step S**152**.

In the step S**152**, when the operator selects one or the icon images Ca**1**~Ca**6** of cameras or the icon images Cu**1**~Cu**6** of CCUs in the displayed connection configuration window, the command generator **152** issues a command for requesting the transmission of device type ID data to one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-***n* shown in FIG. **4**. Then, control proceeds to a step S**153**.

In the step S**153**, the command generator **152** decides whether it has acquired the device type ID data or not. If it has acquired the device type ID data (YES), then control proceeds to a step S**155**. If it has not acquired the device type ID data (NO), then control goes to a step S**154**.

In the step S**154**, the display controller **134** writes in the VRAM **105** alarm image data for prompting the operator to confirm whether one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-***n*, which the operator has selected, is connected or not. The alarm image data written in the VRAM **105** are displayed as an alarm image on the display unit **50**. The command generator **139** transmits a command for requesting the transmission of device type ID data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-***n*. Thereafter, control returns to the step S**153**.

In the step S**155**, the file manager **402** confirms the acquired device type ID data by specifying a device type setting file corresponding to the acquired device type ID data. Then, control proceeds to a step S**156**.

In the step S**156**, the file manager **402** reads the device type setting file corresponding to the acquired device type ID which is confirmed in the step S**155** from the disk drive **350**. Thereafter, control returns to the step S**157**.

In the step S**157**, the file manager **402** decides whether it has properly read file data from the device type setting file or not. If it has properly read the file data (YES), then control proceeds to a step S**159**. If it has not properly read the file data (NO), then control goes to a step S**158**.

In the step S**158**, the display controller **134** writes in the VRAM **105** alarm image data indicating that the file manager **402** has failed to read the file data. The alarm image data written in the VRAM **105** are displayed as an alarm image on the display unit **50**. Then, control goes back to the step S**156**.

In the step S**159**, the parameter controller **138** establishes setting items based on the device type setting file data read

by the file manager **140**, and the display controller **134** writes window image data in the VRAM **105** based on the device type setting file data. The window image data written in the VRAM **105** are displayed as a window image on the display unit **50**. Then, control proceeds to a step **S160**.

In the step **S160**, the command generator **139** issues a command for confirming a connection to the data converter **400**. The command generator **139** decides whether the data converter **400** is connected or not based on whether it has received a response to the command or not. If the data converter **400** is connected (YES), then control proceeds to a step **S161** shown in FIG. **15**. If the data converter **400** is not connected (NO), then control jumps to a step **S162** shown in FIG. **15**.

In the step **S161**, the command generator **139** issues a command for requesting the transmission of setup data indicating a present setup status to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control goes to a step **S163**.

In the step **S163**, the command generator **139** decides whether it has acquired the setup data or not. If it has acquired the setup data (YES), then control proceeds to a step **S164**. If it has not acquired the setup data (NO), then control goes back to the step **S162**.

In the step **S164**, the file manager **140** stores the transmitted present setup data as a file in the RAM **103**. Thereafter, control proceeds to a step **S165**.

In the step **S165**, the file manager **140** verifies the contents of the setup data stored in the RAM **103**. Then, control proceeds to a step **S166**.

In the step **S166**, the file manager **140** decides, as a result of the verification process in the step **S165**, whether the contents of the transmitted setup data and the contents of the setup data stored in the RAM **103** agree with each other or not. If they agree with each other (YES), then control jumps to a step **S174** shown in FIG. **16**. If they do not agree with each other (NO), then control proceeds to a step **S167**.

In the step **S167**, the display controller **134** writes disagreement information image data indicative of the disagreed data contents in the VRAM **105**. The disagreement information image data written in the VRAM **105** are displayed as an image on the display unit **50**. Thereafter, control proceeds to a step **S168**.

In the step **S168**, the command analyzer **133** decides whether it has been instructed by the operator to set up the device according to the present setup data or not. If it has been instructed to set up the device (YES), then control goes to a step **S169**. If it has not been instructed to set up the device (NO), then control goes to a step **S170**.

In the step **S169**, the display controller **134** writes in the VRAM **105** image data indicative of the contents of setup items according to the present setup data. The image data written in the VRAM **105** are displayed as an image on the display unit **50**. Thereafter, control goes to the step **S174** shown in FIG. **16**.

In tho step **S170**, the display controller **134** writes in the VRAM **105** image data indicative of the contents of setup items according to the contents of a setting file. The image data written in the VRAM **105** are displayed as an image on the display unit **50**. Thereafter, control goes to a step **S171** shown in FIG. **16**. The setting file is a file stored in the disk drive **150**.

In the step **S171**, the command generator **140** transmits the setup data of the setting file to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. When the setup data are transmitted to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***, the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** establishes its own parameters to set up itself based on the transmitted setup data. Then, control proceeds to a step **S172**.

In the step **S172**, the command analyzer **133** analyzes a command from the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** to decide whether the transmission of the setup data has properly been finished or not. If the transmission of the setup data has properly been finished (YES), then control proceeds to the step **S174**. If the transmission of the setup data has not properly been finished (NO), then control goes to a step **S173**.

In the step **S173**, the command generator **173** retransmits the setup data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Thereafter, control goes back to the step **S171**.

In the step **S174**, the instruction analyzer **132** analyzes the position in the image where an instruction is entered through the pointing device **300** or the keyboard **250** by the operator. Based on the analyzed position, the command analyzer **133** analyzes a command entered by the operator, and decides whether the command indicates a file process or not. If the command indicates a file process (YES), then control goes to a step **S200**. If the command does not indicate a file process (NO), then control goes to a step **S175**.

The file process is executed in the step **S200**. Control then jumps from the step **S200** to a step **S178**.

In the step **S175**, the instruction analyzer **132** analyzes the position in the image where an instruction is entered through the pointing device **300** or the keyboard **250** by the operator. Based on the analyzed position, the command analyzer **133** analyzes a command entered by the operator, and decides whether the command indicates a setup process or not. If the command indicates a setup process (YES), then control goes to a step **S250**. If the command does not indicate a setup process (NO), then control goes to a step **S176**.

The setup process is executed in the step **S250**. Control then jumps from the step **S250** to the step **S178**.

In the step **5176**, the instruction analyzer **132** analyzes the position in the image where an instruction is entered through the pointing device **300** or the keyboard **250** by the operator. Based on the analyzed position, the command analyzer **133** analyzes a command entered by the operator, and decides whether the command indicates an edit process or not. If the command indicates an edit process (YES), then control goes to a step **S300**. If the command does not indicate an edit process (NO), then control goes to a step **S177**.

The edit process is executed in the step **S300**. Control then jumps from the step **S300** to the step **S178**.

In the step **S177**, the instruction analyzer **132** analyzes the position in the image where an instruction is entered through the pointing device **300** or the keyboard **250** by the operator. Based on the analyzed position, the command analyzer **133** analyzes a command entered by the operator, and decides whether the command indicates a help process or not. If the command indicates a help process (YES), then control goes to a step **S350**. If the command does not indicate a help process (NO), then control goes to the step **S178**.

The help process is executed in the step **S350**. Control then goes from the step **S350** to the step **S178**.

In the step **S178**, the instruction analyzer **132** analyzes the position in the image where an instruction is entered through the pointing device **300** or the keyboard **250** by the operator. Based on the analyzed position, the command analyzer **133** analyzed a command entered by the operator, and decides whether the command indicates an end of the camera setup system or not. If the command indicates an end of the

camera setup system (YES), then control comes to an end. If the command does not indicate an end of the camera setup system (NO), then control goes back to the step **S174**.

N. A Setup Process of the Camera Setup System (see FIGS. **17** and **18**)

FIGS. **17** and **18** shows the setup process in the main processing sequence shown in FIG. **16**.

In a step **S251** shown in FIG. **17**, the instruction analyzer **132** analyzes the position in the image where an instruction is entered through the pointing device **300** or the keyboard **250** by the operator. Based on the analyzed position, the command analyzer **133** analyzes a command entered by the operator, and decides whether the command indicates the designation of a setup item or not. If the command indicates the designation of a setup item (YES), then control proceeds to a step **S252**.

In the step **S252**, the parameter controller **138** selects a parameter corresponding to the setup item designated by the operator. Then, control proceeds to a step **S253**.

In the step **S253**, the file manager **140** reads image data of a parameter setting window corresponding to the parameter selected in the step **S252**, from the disk drive **350**. The display controller **134** writes the read image data of the parameter setting window in the VRAM **105**. The image data of the parameter setting window written in the VRAM **105** are displayed as an image on the display unit **50**. Then, control proceeds to a step **S254**.

In the step **S254**, the command analyzer **133** decides whether there is a waveform display or not. If there is a waveform display (YES), then control proceeds to a step **S255**. If there is not a waveform display (NO), then control jumps to a step **S258**.

In the step **S255**, the instruction analyzer **132** analyzes the position in which the button of the pointing device **300** is pressed. Based on the analyzed positioned, the instruction analyzer **132** decides whether a waveform display is indicated or not. If a waveform display is indicated (YES), then control proceeds to a step **S256**. If a waveform display is not indicated (NO), then control goes to a step **S257**.

In the step **S256**, the display controller **134** writes the image data of a waveform display window in the VRAM **105**. The image data of the waveform display window written in the VRAM **105** are displayed as an image on the display unit **50**. Thereafter, control proceeds to a step **S258**.

In the step **S257**, the display controller **134** writes the image data of a parameter setting window in the VRAM **105**. The image data of the parameter setting window written in the VRAM **105** are displayed as an image on the display unit **50**. The displayed image data of the waveform display window are now deleted from the display unit **50**. Then, control goes to the step **S258**.

In the step **S258**, the instruction analyzer **132** analyzes the position in the image in which the button of the pointing device **300** is clicked. Based on the analyzed positioned, the instruction analyzer **132** decides whether there is a change in the switch image or not. If there is a change in the switch image (YES), then control proceeds to a step **S259**. If there is not a change in the switch image (NO), then control goes to a step **S266** shown in FIG. **18**.

In the step **S259**, a change process with a switch is executed. Thereafter, control goes to the step **S266** shown in FIG. **18**.

In the step **S266**, the instruction analyzer **132** analyzes the position in the image in which the button of the pointing device **300** is pressed. Based on the analyzed positioned, the instruction analyzer **132** decides whether there is a change in the slide lever image or not. If there is a change in the slide lever image (YES), then control proceeds to a step **S267**. If there is not a change in the slide lever image (NO), then control goes to a step **S277**.

In the step **S267**, a change process with a slide lever is executed. Thereafter, control goes to the step **S277**.

In the step **S277**, the instruction analyzer **132** analyzes the position in the image in which the button of the pointing device **300** is clicked. Based on the analyzed positioned, the instruction analyzer **132** decides whether there is a change in the numerical value or not. If there is a change in the numerical value (YES), then control proceeds to a step **S278**. If there is not a change in the numerical value (NO), then control proceeds to a step **S288**.

In the step **S278**, a change process with a numerical value is executed. Thereafter, control goes to the step **S288**.

In the step **S288**, the instruction analyzer **132** analyzes the position in the image in which the button of the pointing device **300** is clicked. Based on the analyzed positioned, the instruction analyzer **132** decides whether the waveform display is ON or not. If the waveform display is ON (YES), then control proceeds to a step **S289**. If the waveform display is not ON (NO), then control proceeds to a step **S290**.

In the step **S289**, the instruction analyzer **132** analyzes the position in the image in which the button of the pointing device **300** is pressed. Based on the analyzed positioned, the instruction analyzer **132** decides whether there is a change in the waveform or not. If there is a change in the waveform (YES), then control proceeds to a step **S290**. If there is not a change in the waveform (NO), then control proceeds to a step **S299**.

In the step **S290**, a change process with a waveform is executed. Then, control goes to the step **S299**.

In the step **S299**, the instruction analyzer **132** analyzes the position in the image in which the button of the pointing device **300** is clicked. Based on the analyzed positioned, the command analyzer **133** decides whether the command entered by the operator indicates that the setup process is finished or not. It the command indicates that the setup process is finished (YES), then the setup process comes to an end. If the command does not indicate that the setup process is finished (NO), then control goes back to the step **S254**.

O. A Change Process With a Switch of the Camera Setup System (see FIG. **19**)

FIG. **19** shows a change process with a switch in the step **S259** of the setup process shown in FIG. **17**.

In a step **S260** shown in FIG. **19**, the display controller **134** writes switch image data after they are changed in the VRAM **105**. The switch image data written in the VRAM **105** are displayed as an image on the display unit **50**. Then, control proceeds to a step **S261**.

In the step **S261**, the parameter controller **138** changes the value of the corresponding parameter data. Then, control proceeds to a step **S262**.

In the step **S262**, the file manager **140** sets the changed parameter data as film data in the file stored in the RAM **104**, and saves the file data in the disk drive **350**. Thereafter, control goes to a step **S263**.

In the step **S263**, the command generator **139** transmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control proceeds to a step **S264**.

In the step **S264**, the command analyzer **133** analyzes a command from the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***, or a command from the data converter **400** to decide whether the transmission has prop-

erly been finished or not. If the transmission has properly been finished (YES), then control leaves the change process. Is the transmission has not properly been finished (NO), then control goes to a step **S265**.

In the step **S265**, the command generator **139** retransmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control goes back to the step **S263**.

P. A Change Process With a Slide Lever of the Camera Setup System (see FIG. **20**)

FIG. **20** shows a change process with a slide lever in the step **S267** of the setup process shown in FIG. **18**.

In a step **S268** shown in FIG. **20**, the instruction analyzer **132** detects the distance that the pointing device **300** has moved after the button of the pointing device **300** has been pressed until the button of the pointing device **300** is released. Based on the detected distance, the display controller **134** changes the image data of a slide lever stored in the VRAM **105**. Then, control proceeds to a step **S269**.

In the step **S269**, the display controller **134** changes the image data of a numerical value stored in the VRAM **105** based on the detected distance. Then, control proceeds to a step **S270**.

In the step **S270**, the parameter controller **138** changes parameter data based on the detected distance. Then, control proceeds to a step **S271**.

In the step **S271**, the display controller **134** decides whether the waveform display is ON or not. If the waveform display is ON (YES), then control proceeds to a step **S272**. If the waveform display is not ON (NO), then control proceeds to a step **S273**.

In the step **S272**, the display controller **134** changes a waveform image stored in the VRAM **105** based on the detected distance. Then, control goes to the step **S273**.

In the step **S273**, the file manager **140** sets the changed parameter data as file data in the file stored in the RAM **104**, and saves the file data in the disk drive **350**. Thereafter, control goes to a step **S274**.

In the step **S274**, the command generator **139** transmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control proceeds to a step **S275**.

In the step **S275**, the command analyzer **133** analyzes a command from the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***, or a command from the data converter **400** to decide whether the transmission has properly been finished or not. If the transmission has properly been finished (YES), then control leaves the change process. If the transmission has not properly been finished (NO), then control goes to a step **S276**.

In the step **S276**, the command generator **139** retransmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control goes back to the step **S274**.

Q. A Change Process With a Numerical Value of the Camera Setup System (see FIG. **21**)

FIG. **21** shows a change process with a numerical value in the step **S278** of the setup process shown in FIG. **18**.

In a step **S279** shown in FIG. **21**, the instruction analyzer **132** detects numerical data entered from the keyboard **250**. Based on the detected numerical data, the display controller **134** changes numerical image data stored in the VRAM **105**. Then, control proceeds to a step **S280**.

In the step **S280**, the display controller **134** changes the image data of a slide lever stored in the VRAM **105** based on the numerical data. Then, control proceeds to a step **S281**.

In the step **S281**, the parameter controller **138** changes parameter data based on the numerical data. Then, control proceeds to a step **S282**.

In the step **S282**, the display controller **134** decides whether the waveform display is ON or not. If the waveform display is ON (YES), then control proceeds to a step **S283**. If the waveform display is not ON (NO), then control proceeds to a step **S284**.

In the step **S283**, the display controller **134** changes a waveform image stored in the VRAM **105** based on the numerical data. Then, control goes to the step **S284**.

In the step **S284**, the file manager **140** sets the changed parameter data as file data in the file stored in the RAM **104**, and saves the file data in the disk drive **350**. Thereafter, control goes to a step **S285**.

In the step **S285**, the command generator **139** transmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control proceeds to a step **S286**.

In the step **S286**, the command analyzer **133** analyzes a command from the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***, or a command from the data converter **400** to decide whether the transmission has properly been finished or not. If the transmission has properly been finished (YES), then control leaves the change process. If the transmission has not properly been finished (NO), then control goes to a step **S287**.

In the step **S287**, the command generator **139** retransmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control goes back to the step **S285**.

R. A Change Process With a Waveform of the Camera Setup System (see FIG. **22**)

FIG. **22** shows a change process with a waveform in the step **S290** of the setup process shown in FIG. **18**.

In a step **S291** shown in FIG. **22**, the instruction analyzer **132** detects the distance that the pointing device **300** has moved after the button of the pointing device **300** has been pressed until the button of the pointing device **300** is released. Based on the detected distance, the display controller **134** changes the image data of a waveform stored in the VRAM **105**. Then, control proceeds to a step **S292**.

In the step **S292**, the display controller **134** changes the image data of a slide lever stored in the VRAM **105** based on the detected distance. Then, control proceeds to a step **S293**.

In the step **S293**, the display controller **134** changes the image data of a numerical value stored in the VRAM **105** based on the detected distance. Then, control proceeds to a step **S294**.

In the step **S294**, the parameter controller **138** charges parameter data based on the detected distance. Then, control proceeds to a step **S295**.

In the step **S295**, the file manager **140** sets the changed parameter data as file data in the file stored in the RAM **104**, and saves the file data in the disk drive **350**. Thereafter, control goes to a step **S296**.

In the step **S296**, the command generator **139** transmits the parameter data to the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***. Then, control proceeds to a step **S297**.

In the step **S297**, the command analyzer **133** analyzes a command from the selected one of the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***, or a command from the data converter **400** to decide whether the transmission has properly been finished or not. If the transmission has properly been finished (YES), then control leaves the change process. If the transmission has not properly been finished (NO), then control goes to a step **S298**.

In the step **S298**, the command generator **139** retransmits the parameter data to the selected one of the cameras **1000**

or the controllers **1200-1**, . . . , **1200-*n***. Then, control goes back to the step S**296**.

S. A Transmission Data Format and File Formats Used in the Camera Set Up System (see FIGS. **23**A through **23**E)

FIGS. **23**A through **23**E show a transmission data format and file formats used in the computer shown in FIG. **4**.

FIG. **23**A shows a transmission data format used at the time of setting parameters. As shown in FIG. **23**A, data which are transmitted comprise device type ID data indicative of a destination, a command indicative of a parameter change, parameter ID data indicative of a parameter to be changed, and parameter data.

FIG. **23**B shows a setup parameter file. As shown in FIG. **23**B, a setup parameter file comprises device type ID data, parameter ID data, and parameter data. The setup parameter file comprises all parameter data established with respect to cameras and CCUs.

FIG. **23**C shows an LSI port data file. As shown in FIG. **23**C, an LSI port data file comprises device type ID data, LSI ID data, data of the number of used bytes, and setting data. The setting data comprise LSI port data and I/O port data required for cameras and CCUs.

FIG. **23**D shows a screen display setting file. As shown in FIG. **23**D, a screen display setting file comprises device type ID data, parameter ID data, and parameter display data. The parameter display data are data indicative of which switch has what value when a switch number is selected for a desired setting.

FIG. **23**E shows an internal device data file. As shown in FIG. **23**E, an internal device data file comprises device type ID data and internal device data. The internal device data include gamma curve data, a scene file, a master setup file, various log files, and service information. The internal device data file is a file for allowing the computer **100** to save and load internal device information other than data handled by a setup parameter file owned by cameras and CCUs.

Although not shown, a device setting file is also used in addition to the above files. There are as many device setting files as the number of device types. A device setting file corresponding to the connected device type is loaded from the disk drive **350** into the computer **100** to allow the computer **100** to effect processes that match the connected device type.

The above five files can be stored in an ASCII test format, for example, in the disk drive **350** shown in FIG. **3** or an IC card or the like inserted in the card slot **109** shown in FIG. **4**. In addition, the contents of these files can be modified in a text format when the command "File Edit" is selected on the pull-down menu "SETUP" shown in FIG. **9**C.

T. A Data Converter in the Camera Setup System Shown in FIG. **3** (see FIG. **24**)

FIG. **24** shows the data converter **400** in the camera setup system shown in FIG. **3**.

Connections and Structure

As shown in FIG. **24**, the data converter **400** comprises a CPU **401**, a bus assembly **402** connected to the CPU **401** and comprising address, data, and control buses, a ROM **403** connected to the bus assembly **402** for storing program data and a protocol converting table, etc., a working RAM **404** connected to the bus assembly **402** for storing data loaded from the computer **100**, and interfaces **406**, **409**, **412** connected to the bus assembly **402**. Connectors **408**, **411**, **414** are connected respectively to the interfaces **406**, **409**, **412** through respective lines **407**, **410**, **413**.

The interface **406** may comprise an RS-232C interface or an RS-422 interface, for example. The interfaces **409**, **412** are provided in two types corresponding to the types of the cameras **1000** and the types of the controllers **1200-1**, . . . , **1200-*n***. Each of these interfaces **409**, **412** may comprise an RS-232C interface or an RS-422 interface, for example.

When the data converter **400** is turned on and command conversion data are loaded from the computer **100** into the data converter **400**, the CPU **401** performs various functions indicated as blocks in a frame surrounded by the dot-and-dash lines.

The functions performed by the CPU **401** will be described below.

A connection checker **415** serves to check connections between the data converter **400** and other devices. A communication controller **416** serves to control communications with other devices which are connected to the data converter **400**. A protocol checker **417** serves to check the communication protocol of data which are transmitted from other devices which are connected to the data converter **400**. A data analyzer **418** serves to decide whether data transmitted from the computer **100** are data for converting command data.

A command converter **419** serves to convert command data transmitted from the computer **100** into command data that can be recognized by the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n***, and also to convert command data supplied from the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** into command data that can be recognized by the computer **100**. A decision unit **420** serves to make various decisions.

Operation of the data converter **400** will be described below with reference to FIGS. **25** through **27**.

U. A Control Sequence of the Data Converter **400** Shown in FIG. **24** (see FIGS. **25** through **27**)

FIGS. **25** through **27** show a control sequence of the data converter **400** shown in FIG. **24**.

It is assumed that a communication protocol used for communications between the computer **100** and the data converter **400** is an ISR protocol provided for by SMPTE RP-273M, a communication protocol used for communications between the data converter **400** and the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** through the interface **409** is an RM protocol, and a communication protocol used for communications between the data converter **400** and the cameras **1000** or the controllers **1200-1**, . . . , **1200-*n*** through the interface **412** is an NCS (New Command System) protocol. The ISR protocol is used by an ISR (Interactive Status Reporting) system which is a centralized management system for broadcasting devices. It is also assumed that transmission of parameter data is carried out between the computer **100** and the data converter **400** and also between the data converter **400** and the cameras **1000**.

The protocols used are specifically described only for illustrative purpose. It is not intended to limit the present invention to any particular protocols and interfaces.

In a step S**401** shown in FIG. **25**, the connection checker **415** confirms cables for their connections. Then, control proceeds to a step S**402**.

In the step S**402**, the decision unit **420** decides whether there are input data from the computer **100** or not. If there are input data from the computer **100** (YES), then control proceeds to a step S**403**.

In the step S**403**, the protocol checker **417** checks the ISR protocol. Thereafter, control proceeds to a step S**404**.

In the step S**404**, the decision unit **420** decides whether the ISR protocol has properly been recognized or not as a result of the checking process. If the ISR protocol has properly been recognized (YES), then control proceeds to a

step **S406**. If the ISR protocol has not properly been recognized (NO), then control proceeds to a step **S405**.

In the step **S405**, the communication controller **416** transmits NAK data to the computer **100**. Then, control goes back to the step **S402**.

In the step **S406**, the communication controller **416** transmits ACK data to the computer **100**. Then, control goes to a step **S407**.

In the step **S407**, the decision unit **420** decides whether the data transmitted from the computer **100** are command conversion data or not. If the data transmitted from the computer **100** are command conversion data (YES), then control proceeds to a step **S408**. If the data transmitted from the computer **100** are not command conversion data (NO), then control goes to a step **S409**.

In the step **S408**, the command converter **419** sets command conversion data. Then, control goes back to the step **S402**.

In the step **S409**, the decision unit **420** decides whether a connected one of the cameras **1000** uses the NCR protocol or not. If the connected camera **1000** uses the NCR protocol (YES), then control goes to a step **S414** shown in FIG. **26**. If a connected camera **1000** does not use the NCR protocol (NO), then control goes to a step **S410**.

In the step **S410**, the command converter **419** converts the communication protocol from the ISR protocol into the RM protocol. Then, control proceeds to a step **S411**.

In the step **S411**, the communication controller **416** transmits data to the camera **1000**. Then, control jumps to a step **S412** shown in FIG. **26**.

In the step **S412**, the decision unit **420** decides whether there is a response from the camera **1000** or not. If there is a response from the camera **1000** (YES), then control proceeds to a step **S413**.

In the step **S413**, the command converter **419** converts the communication protocol from the RM protocol into the ISR protocol. Then, control jumps to a step **S425** shown in FIG. **27**.

In the step **S414**, the command converter **419** converts the communication protocol from the ISR protocol into the NCS protocol. Then, control proceeds to a step **S415**.

In the step **S415**, the communication controller **416** transmits data to the camera **1000**. Then, control proceeds to a step **S416**.

In the step **S416**, the communication controller **416** receives ACK data from the camera **1000**. Then, control proceeds to a step **S417**.

In the step **S417**, the decision unit **420** decides whether the data have properly been transmitted or not. If the data have properly been transmitted (YES), then control proceeds to a step **S419** shown in FIG. **27**. If the data have not properly been transmitted (NO), then control proceeds to a step **S418**.

In the step **S418**, the communication controller **416** retransmits the error data. Then, control goes back to the step **S415**.

In the step **S419**, the decision unit **420** decides whether there is a response from the camera **1000** or not. If there is a response from the camera **1000** (YES), then control proceeds to a step **S420**.

In the step **S420**, the protocol checker **417** checks the protocol. Thereafter, control proceeds to a step **S421**.

In the step **S421**, the decision unit **420** decides whether the NCS protocol has properly been recognized or not as a result of the checking process. If the NCS protocol has properly been recognized (YES), then control proceeds to a step **S423**. If the NCS protocol has not properly been recognized (NO), then control proceeds to a step **S422**.

In the step **S422**, the communication controller **416** transmits NAK data to the camera **1000**. Then, control goes back to the step **S419**.

In the step **S423**, the communication controller **416** transmits ACK data to the camera **1000**. Then, control proceeds to a step **S424**.

In the step **S424**, the command converter **419** converts the communication protocol from the NCS protocol into the ISR protocol. Then, control proceeds to the step **S425**.

In the step **S425**, the communication controller **416** transmits data to the computer **100**. Then, control proceeds to a step **S426**.

In the step **S426**, the communication controller **416** receives ACK data from the computer **100**. Then, control proceeds to a step **S427**.

In the step **S427**, the decision unit **420** decides whether the data has properly been transmitted or not. If the data have properly been transmitted (YES), then control goes back to the step **S402**. If the data have not properly been transmitted (NO), then control goes to a step **S428**.

In the step **S428**, the communication controller **416** retransmits the error data. Thereafter, control goes back to the step **S425**.

V. A Video System of a Camera **1000** Shown in FIG. **3** (see FIG. **28**)

FIG. **28** shows a video system of each of the cameras **1000** shown in FIG. **3**.

As shown in FIG. **28**, the video system of the camera **1000** comprises an objective lens **501**, a CC filter **502**, an ND filter **503**, CCDs **504**, **505**, **506** for detecting R, G, B signals, amplifiers **508**, **509**, **510**, adders **511**, **521**, **513** for adjusting black set and black shading, amplifiers **515**, **516**, **517**, trap filters **518**, **519**, **520**, gain-control amplifiers **521**, **522**, **523**, multipliers **525**, **526**, **527** for adjusting white shading, adders **529**, **530**, **531** for adjusting flare, pre-knee circuits **533**, **534**, **535** for controlling pre-knee, digital low-pass filters **537**, **538**, **539**, A/D converters **540**, **541**, **542**, 1H delay circuits **544**, **545**, **546**, **547**, **548**, **549**, a profile or edge correcting signal generator **550**, a digital low-pass filter **551**, a linear matrix circuit **552** for controlling a matrix, adders **553**, **554**, **555** for pedestal (black) control, black gamma correcting circuits **556**, **557**, **558** for black gamma control, knee correcting circuits **559**, **560**, **561** for knee control, gamma correcting circuits **562**, **563**, **564** for gamma control, adders **565**, **566**, **567** for edge correction, black/white clip circuits **568**, **569**, **570** for black/white clip control, digital low-pass filters **571**, **572**, **573**, rate converters **574**, **575**, **576** for converting sampling rates, an encoder **577** for producing an NTSC or PAL composite video signal, a D/A converter **547**, a controller **580**, a timing generator **507**, D/A converters **514**, **524**, **528**, **532**, **536**, and a snaring detector **543**.

An input/output terminal **581** is connected to the controllers **1200-1**, . . . , **1200-*n***. An output terminal **582** is connected to a display signal input terminal of the LCD unit **700** shown in FIG. **3**. An input terminal **583** is connected to a control data output terminal of the control key group **750**.

Operation for Setting Parameters

The controller **580** receives device type ID data, command data, parameter ID data, and parameter data which are supplied from the computer **100** through the input/output terminal **581**, the system controller **100**, and the controller **1200-1**. The controller **580** decides whether the transmitted data are destined for itself based on the device type ID data, recognizes what processing is to be made based on the contents of the command data, and effects a control process on a parameter indicated by the parameter ID data based on the parameter data.

The controller **580** supplies a CC filter control signal to the CC filter **502** to control the CC filter **502**, supplies an ND filter control signal to the ND filter **503** to control the ND filter **503**, and supplies a shutter control signal to the timing generator **507** to cause the timing generator **507** to supply CCD drive control signals to the CCDs **504**, **505**, **506** for shutter control.

The controller **580** also supplies a black set and black shading signal through the D/A converter **514** to adders **511**, **512**, **513**, supplies a gain control signal through the D/A converter **524** to the gain-control amplifiers **521**, **522**, **523**, supplies a white shading control signal through the D/A converter **528** to the multipliers **525**, **526**, **527**, supplies a flare control signal through the D/A converter **532** to the adders **529**, **530**, **531**, and supplies a pre-knee control signal through the D/A converted **536** to the pre-knee circuits **533**, **534**, **535**.

The controller **580** receives shading data, as control data, which are produced when the shading detector **543** detects output data from the A/D converters **540**, **541**, **542**.

The controller **580** supplies a detail control signal to the edge correcting signal generator **550**. The edge correcting signal generator **550** then supplies detail data to the adders **565**, **566**, **567**. The controller **580** supplies a matrix control signal to the linear matrix circuit **552**, supplies a pedestal (black) control signal to the adders **553**, **554**, **555**, supplies a black gamma control signal to the black gamma correcting circuits **556**, **557**, **558**, supplies a knee control signal to the knee correcting circuits **559**, **560**, **561**, supplies a gamma control signal to the gamma correcting circuits **562**, **563**, **564**, supplies a black/white clip control signal to the black/white clip circuits **568**, **569**, **570**.

W. An Audio System of a Camera **1000** Shown in FIG. **3** (see FIG. **29**)

FIG. **29** shows an audio system of each of the cameras **1000** shown in FIG. **3**.

As shown in FIG. **29**, the audio system has a processing system MIC/LINE for an audio signal inputted from the microphone **850** shown in FIG. **3** and a line, a first audio input signal processing system INCOM-**1** for a first audio signal inputted from the intercom of the camera **1000**, a second audio input signal processing system INCOM-**2** for a second audio signal inputted from the intercom of the camera **1000**, a third audio input signal processing system INCOM-**3** for a third audio signal inputted from the intercom of the camera **1000**, a first audio output signal processing system INCOM-**1** for a first audio signal outputted to the intercom of the camera **1000**, a second audio output signal processing system INCOM-**2** for a second audio signal outputted to the intercom of the camera **1000**, a third audio output signal processing system INCOM-**3** (Tracker) for a third audio signal outputted to the intercom of the camera **1000**, a first program audio output signal processing system PGM-**1** for a first program audio signal outputted to the intercom of the camera **1000**, a second program audio output signal processing system PGM-**2** for a second program audio signal outputted to the intercom of the camera **1000**, a third program audio output signal processing system PGM-**3** for a third program audio signal outputted to the intercom of the camera **1000**, a matrix circuit **612**, parallel-to-serial converters **613**, **625**, **627**, serial-to-parallel converters **626**, **628**, **614**, an encoder **606**, and a decoder **624**.

The processing system MIC/LINE comprises an amplifier **603** for amplifying an audio signal inputted from the microphone **850** or the like through an input terminal **601**, an amplifier **604** for amplifying an audio signal inputted from the microphone **850** or the like through an input terminal **602**, and an A/D converter **605** for converting amplified audio signals into digital audio signals.

The first audio input signal processing system INCOM-**1** comprises an amplifier **609** for amplifying a first audio signal supplied from the intercom of the camera **1000** through an input terminal **608**, an A/D converter **610** for converting an amplified audio signal from the amplifier **609** into a digital audio signal, and a serial-to-parallel converter **611** for converting the digital audio signal outputted from the A/D converter **610** into a parallel digital audio signal.

The second audio input signal processing system INCOM-**2** comprises an amplifier **616** for amplifying a second audio signal supplied from the intercom of the camera **1000** through an input terminal **615**, an A/D converter **617** for converting an amplified audio signal from the amplifier **616** into a digital audio signal, and a serial-to-parallel converter **618** for converting the digital audio signal outputted from the A/D converter **617** into a parallel digital audio signal.

The third audio input signal processing system INCOM-**3** comprises an amplifier **620** for amplifying a second audio signal supplied from the intercom of the camera **1000** through an input terminal **619**, an A/D converter **621** for converting an amplified audio signal from the amplifier **620** into a digital audio signal, and a serial-to-parallel converter **622** for converting the digital audio signal outputted from the A/D converter **621** into a parallel digital audio signal.

The first audio output signal processing system INCOM-**1** comprises a parallel-to-serial converter **629** for converting a parallel digital audio signal from the matrix circuit **612** into a serial digital audio signal, a D/A converter **630** for converting the digital audio signal outputted from the parallel-to-serial converter **629** into an analog audio signal, and an amplifier **631** for amplifying the analog audio signal outputted from the D/A converter **630** and outputting the amplified audio signal to the intercom of the camera **1000** through an output terminal **632**.

The second audio output signal processing system INCOM-**2** comprises a parallel-to-serial converter **635** for converting a parallel digital audio signal from the matrix circuit **612** into a serial digital audio signal, a D/A converter **636** for converting the digital audio signal outputted from the parallel-to-serial converter **635** into an analog audio signal, and an amplifier **637** for amplifying the analog audio signal outputted from the D/A converter **636** and outputting the amplified audio signal to the intercom of the camera **1000** through an output terminal **638**.

The third audio output signal processing system INCOM-**3** comprises a parallel-to-serial converter **641** for converting a parallel digital audio signal from the matrix circuit **612** into a serial digital audio signal, a D/A converter **642** for converting the digital audio signal outputted from the parallel-to-serial converter **641** into an analog audio signal, and an amplifier **643** for amplifying the analog audio signal outputted from the D/A converter **642** and outputting the amplified audio signal to the intercom of the camera **1000** through an output terminal **644**.

The first program audio output signal processing system PGM-**1** comprises the parallel-to-serial converter **629** for converting a parallel digital audio signal from the matrix circuit **612** into a serial digital audio signal, the D/A converter **630** for converting the digital audio signal outputted from the parallel-to-serial converter **629** into an analog audio signal, and an amplifier **633** for amplifying the analog audio signal outputted from the D/A converter **630** and outputting the amplified audio signal to the intercom of the camera **1000** through an output terminal **634**.

The second program audio output signal processing system PGM-**2** comprises the parallel-to-serial converter **635** for converting a parallel digital audio signal from the matrix circuit **612** into a serial digital audio signal, the D/A converter **636** for converting the digital audio signal outputted from the parallel-to-serial converter **635** into an analog audio signal, and an amplifier **639** for amplifying the analog audio signal outputted from the D/A converter **636** and outputting the amplified audio signal to the intercom of the camera **1000** through an output terminal **640**.

The third program audio output signal processing system PGM-**3** comprises the parallel-to-serial converter **641** for converting a parallel digital audio signal from the matrix circuit **612** into a serial digital audio signal, the D/A converter **642** for converting the digital audio signal outputted from the parallel-to-serial converter **641** into an analog audio signal, and an amplifier **645** for amplifying the analog audio signal outputted from the D/A converter **642** and outputting the amplified audio signal to the intercom of the camera **1000** through an output terminal **646**.

Based on a control signal from the controller **580** shown in FIG. **28**, the matrix circuit **612** mixes three audio signals inputted from the serial-to-parallel converters **611**, **618**, **622**, and mixes audio signals inputted from an input terminal **623** as AUX IN, converted from a video signal rate into an audio signal rate by the decoder **624**, and converted by the serial-to-parallel converters **626**, **628** into audio signals for the processing systems INCOM-**1**, INCOM-**2**, and audio signals for the processing systems PGM-**1**, PGM-**2**. Based on a control signal from the controller **580** shown in FIG. **28**, the encoder **606** converts an audio signal of the processing system MIC/LINE from the A/D converter **605**, and an audio signal outputted from the matrix circuit **612**, converted into a serial signal by the parallel-to-serial converter **613**, and converted into a parallel signal by the serial-to-parallel converter **614**, from an audio signal rate into a video signal rate, and outputs the signals from an output terminal **607** as AUX OUT.

The serial-to-parallel converters **611**, **618**, **622**, **626**, **628**, the matrix circuit **612**, and the parallel-to-serial converters **629**, **635**, **641**, **613** are integrated into one LSI circuit. The serial-to-parallel converter **614**, the parallel-to-serial converters **625**, **627**, the encoder **606**, and the decoder **624** are integrated into one LSI circuit.

X. Displayed Images for Establishing Parameters in the Camera Setup System (see FIGS. **30**A and **30**B through **87**)

FIGS. **30**A and **30**B through **87** show, by way of example, displayed images for establishing parameters in the camera setup system. Only those portions of the displayed images which are necessary for the description of the present invention will be described below. The buttons, switches, slide levers, titles, and areas for displaying numerical values have already been described above with reference to FIG. **3**, and major parameters have also been described above as to their meaning with reference to FIGS. **8** and **12**A through **12**D.

FIG. **30**A shows, by way of example, a displayed image for establishing shutter parameters.

FIG. **30**B shows, by way of example, a displayed image for establishing filter parameters.

In FIG. **30**B, numerical values given in broken-line frames serves to display values applied when switch numbers are selected. In this example, a switch number "**1**" and a switch "A" are selected.

FIG. **31**A shows, by way of example, a displayed image for establishing a test pattern and bars.

FIG. **31**B shows, by way of example, a displayed image for establishing an automatic setup process.

As shown in FIG. **31**B, in the automatic setup process, when a button indicates "START", a parameter indicated by its title is automatically set up. An area Ar**1** displays data indicative of a response from the camera, e.g., an image of letters "COMPLETED" when a test is normally finished.

FIG. **32**A shows, by way of example, a displayed image for establishing iris parameters.

Conversion equations for the F value of numerical data "F5.6" are as follows:

$$F=132.8\times(0.175^{\wedge}(i/(0.35\times 2^{\wedge}n))$$

i=16 bit data (open at 0000H and closed at FFFFH) where n is the bit accuracy (16 bits).

FIG. **32**B shows, by way of example, a displayed image for establishing master black parameters.

When the parameter "ABSOLUTE" is "ON", absolute data are handled, and when the parameter "ABSOLUTE" is "OFF", relative data are handled. The meaning of the absolute and relative data has already been described above.

When the parameter "ABSOLUTE" is "ON", the displayed slide lever and numerical value are changed to an absolute representation ranging from 0 to 100%.

FIG. **32**C shows, by way of example, a displayed image for establishing a master gain parameter.

In FIG. **32**C, a support gain for each device type is established as SW data based on the device type setting file.

FIG. **33** shows, by way of example, a displayed image for establishing knee saturation parameters.

FIG. **34** shows, by way of example, a displayed image for establishing knee and knee saturation parameters.

In FIG. **34**, when the parameter "WHITE CLIP" is "ON", a clip is applied, and when the parameter "WHITE CLIP" is "OFF", a clip is not applied.

Points P**1**, P**2**, P**3** on a waveform image move in the directions indicated by the arrows.

As shown in FIG. **34**, while the button of the pointing device **300** is being pressed, the pointer Po is superposed on the point P**1**, P**2**, or P**3** which is indicated by a broken-line circle in the waveform image. Thereafter, the pointing device **300** is moved to change a waveform L**1** as indicated by the solid-line arrows at the points P**1**, P**2**, P**3**. At the same time, the slide levers, etc. are also changed, and the numerical values in numerical value display areas on the right-hand side of the slide levers are also changed.

A white clip status with respect to a knee status, and a knee status with respect to a white clip status are reflected on the graphic representation.

FIG. **35** shows, by way of example, a displayed image for establishing knee and knee saturation parameters for servicing.

FIG. **36**A shows, by way of example, a displayed image for establishing master V modulation parameters.

FIG. **36**B shows, by way of example, a displayed image for establishing knee parameters.

In FIG. **36**B, when a button on the right-hand side of the parameter "WHITE CLIP" is turned on or off, the white clip is turned on or off at the knee item.

FIG. **37**A shows, by way of example, a displayed image for establishing white clip parameters.

In FIG. **37**A, the button "WAVEFORM>>" for outputting a waveform is not turned on as the button of the pointing device **300** is not clicked.

When the button "KNEE" is turned on or off, the knee can be turned on or off at the white clip item

FIG. **37**B Shows, by way of example, a displayed image for establishing white clip parameters, the displayed image including a displayed waveform.

In FIG. **37**B, the button "WAVEFORM >>" for outputting a waveform is turned on by clicking the button of the pointing device **300**. Therefore, a waveform image is displayed. KP represents a knee point, and WC OFF represents a white clip off. As shown in FIG. **37**B, the button "KNEE" is "OFF". When the button "KNEE" is "ON", a level in excess of the knee point is adjuster as shown by the broken lines in the waveform image as indicated by the arrow.

FIG. **38**A shows, by way of example, a displayed image for establishing detail level parameters.

FIG. **38**B shows, by way of example, a displayed image for establishing detail level parameters, the displayed image including a displayed waveform.

As shown in FIG. **38**B, the detail level can be adjusted by moving a point P with the pointing device **300** in the directions indicated by the solid-line arrow. However, the width of the waveform cannot be varied as indicated by the broken lines at the bottom of the waveform.

The distance between the two intermediate broken lines represents the detail level. When the numerical value is 0%, the detail level is 0%, and when the numerical value is 100%, the retail level is 100%.

FIG. **39**A shows, by way of example, a displayed image for establishing ratio parameters.

In FIG. **39**A, the parameter "H/V RATIO", which represents 100% as a whole, is divided into H and V areas by the slide lever, and each of the H and V areas indicates a percentage. For a relative representation of 99%, the entire parameter range extends from −99 to 0~99, with no H and V percentage representations, and the parameter is represented by a relative value as with other slide levers.

The parameter "H/L RATIO" may present a relative representation of ±99, and increases as it goes toward 100%.

FIG. **39**B shows, by way of example, a displayed image for establishing a gamma mix ratio parameter.

FIG. **40** shows, by way of example, a displayed image for establishing a gamma mix ratio parameter, the displayed image including a displayed waveform.

As shown in FIG. **40**, the letters "PRE", "POST" are displayed above the slide lever. The parameter "PRE" is "100%", i.e., the pre-to-post ratio of the gamma mix is 100% as a pre value. Therefore, the amount of detail remains the same when the video level is low or high as indicated by the elliptical broken lines.

The slide lever is displayed in a relative representation.

When the slide lever represents 0, the pre-to-post ratio of the gamma mix is 50%:50%.

When the slide lever represents −99, the pre-to-post ratio of the gamma mix is 100%:0%.

When the slide lever represents +99, the pre-to-post ratio of the gamma mix is 0%:100%.

FIG. **41** shows, by way of example, a displayed image for establishing a gamma mix ratio parameter, the displayed image including a displayed waveform.

Since the parameter "POST" is "100%", i.e., the pre-to-post ratio of the gamma mix is 100% as a post value. Therefore, the amount of detail is smaller when the video level is lower, and the amount of detail is greater when the video level is higher, as indicated by the elliptical broken lines.

FIG. **42** shows, by way of example, a displayed image for establishing R, G, B mix parameters.

As shown in FIG. **42**, the parameter "MIX RAIO" for "H-DTL" includes an area having a fixed value of 50% for G (green), and a remaining area divided into variable % values for R (red) and B (blue) by the slide lever.

The parameter "V-DTL MODE" for "V-DTL" has two buttons "MIX", "NAM". When the button "NAM" is selected, contrary to the selection in the illustrated example, the mix ratio has no bearing on this parameter, and the data cannot be changed.

In the parameter "MIX RATIO", two slide levers are displayed, dividing the entire bar into variable % values for R, G, B. The slide levers represent ratios R:B and RB:G. When the ratio R:B is changed, the lever of the ratio RB:G is not moved. When the lever of the ratio RB:G is moved, the lever of the ratio R:B is also moved therewith because the ratio R:B varies at the same ratio.

FIG. **43**A shows, by way of example, a displayed image for establishing a slim detail parameter.

FIG. **43**B shows, by way or example, a displayed image for establishing a slim detail parameter, the displayed image including a displayed waveform.

The width indicated by the solid-line arrow on the displayed waveform image is representative of the parameter "SLID RAIO". The detail width can be narrowed about the center of the detail waveform.

FIG. **43**C shows, by way of example, a displayed image for establishing a slant detail parameter.

In FIG. **43**C, when the numerical data displayed in a broken-line frame are 0%, no detail in an oblique direction is applied. When the numerical data are 100%, a fully adjusted detail in an oblique direction is applied. The slant detail parameter may be displayed in a relative representation of ±99.

FIG. **44**A shows, by way of example, a displayed image for establishing H limiter parameters.

FIG. **44**B shows, by way of example, a displayed image for establishing H limiter parameters, the displayed image including a displayed waveform.

In FIG. **44**B, a parameter setting image is displayed when a waveform display button is turned on by the pointing device **300**. As shown in FIG. **44**B, when the button of the pointing device **300** is pressed at a pointer **P1** or **P2** and then moved in the directions indicated by the arrow, the width W of a white level or the width B of a black level in a horizontal direction can be changed. At the same time, the displayed slide levers and numerical values are also changed.

The parameter "MASTER LIMIT LEVEL" may not be used depending on the type of a camera connected. In such a case, this parameter is not displayed or masked in its display by shading or the like, so that it cannot be accessed.

The slide lever may be displayed in a relative representation of ±99. When the slide lever moves toward +, it moves in a limiting direction, and when the slide lever moves toward −, it moves in an unlimiting direction.

When the limit level is 0%, no limit is applied, and the detail may be applied up to a maximum detail level.

When the limit level is 100%, a maximum limit is applied, and hence no detail is applied.

FIG. **45**A shows, by way of example, a displayed image for establishing V limiter parameters.

FIG. **45**B shows, by way of example, a displayed image for establishing V limiter parameters, the displayed image including a displayed waveform.

In FIG. **45**B, a parameter setting image is displayed when a waveform display button is turned on by the pointing device **300**. As shown in FIG. **45**B, when the button of the pointing device **300** is pressed at a pointer **P1** or **P2** and then moved in the directions indicated by the arrow, the width W of a white level or the width B of a black level in a vertical direction can be changed. At the same time, the displayed slide levers and numerical values are also changed.

FIG. **46** shows, by way of example, a displayed image for establishing knee aperture parameters.

FIG. **47** shows, by way of example, a displayed image for establishing knee aperture parameters, the displayed image including a displayed waveform.

As shown in FIG. **47**, when the button "KNEE" is "OFF", the displayed KP (knee point) disappears, and the displayed waveform image becomes a linear step-like waveform image. Detail levels for H, V, black, and white are applied at ×1.0. When the button "KNEE" is "ON" and the button "KNEE APERTURE" is "OFF", the knee is applied at a step higher than the knee point, but the detail level remains fixed at ×1.0.

Data may be established by moving the slide levers or changing the displayed numerical values. While the waveform image varies in unison with the slide levers, the settings cannot not be varied by moving the waveform image in this parameter setting image.

The detail level of ×1.0 is the same as a detail level lower than the knee point. The detail level of ×2.0 is twice a detail level lower than the knee point. The detail level of ×0 eliminates details above the knee point.

In broken-line elliptical areas in the displayed waveform image, the detail levels of black and white are adjusted with respect to details above the knee point.

The buttons "H", "V" ("V" is shown as selected) displayed below the waveform image serve to switch between H and V displayed waveform images.

FIG. **48** shows, by way of example, a displayed image for establishing knee aperture parameters, the displayed image including a displayed waveform.

FIG. **49**A shows, by way of example, a displayed image for establishing level depend parameters.

FIG. **49**B shows, by way of example, a displayed image for establishing level depend parameters, the displayed image including a displayed waveform.

In FIG. **49**B, when a point **P1** in the displayed waveform image is moved as indicated by the arrow, the gain is changed. When a point **P2** in the displayed waveform image is moved as indicated by the arrow, the parameter "AREA" is changed. At this time, a broken-line elliptical area of the waveform image moves therewith.

FIG. **50** shows, by way of example, a displayed image for establishing level depend parameters for servicing, the displayed image including a displayed waveform. The details of this displayed image are the same as those of FIGS. **49**A and **49**B except the parameter "TRANS". The parameter "TRANS" serves to change the width between area and trans points.

FIG. **51**A shows, by way of example, a displayed image for establishing crispening parameters.

FIG. **51**B shows, by way of example, a displayed image for establishing crispening parameters, the displayed image including a displayed waveform.

FIG. **52** shows, by way of example, a displayed image for establishing crispening parameters for servicing, the displayed image including a displayed waveform.

In FIG. **52**, the level is changed when a pointer **P1** in the displayed waveform image is moved as indicated by the arrow.

FIG. **53** shows, by way of example, a displayed image for establishing skin tone parameters.

The parameter "PHASE" can be changed in the range of 0 to 360 degrees.

FIG. **54** shows, by way of example, a displayed image for establishing skin tone parameters.

FIG. **55** shows, by way of example, a displayed image for establishing skin tone parameters, the displayed image including a displayed waveform.

Of the parameters "SKIN TONE **1**", "SKIN TONE **2**", those parameters for which the buttons are "ON" can be established.

FIG. **56** shows, by way of example, a displayed image for establishing skin tone parameters, the displayed image including a displayed waveform.

The parameter "WIDTH" represents a phase width.

FIG. **57**A shows, by way of example, a displayed image for establishing a detail area parameter, the displayed image including a displayed waveform.

FIG. **57**B shows, by way of example, a displayed image for establishing a detail area parameter, the displayed image including a displayed waveform.

FIG. **58**A shows, by way of example, a displayed image for establishing black parameters.

FIG. **58**B shows, by way of example, a displayed image for establishing black parameters, the displayed image including a displayed waveform.

FIG. **59** shows, by way of example, a displayed image for establishing white parameters.

FIG. **60** shows, by way of example, a displayed image for establishing white parameters, the displayed image including a displayed waveform.

In FIG. **60**, when the button "ABSOLUTE" is "ON", absolute data are handled, and when button "ABSOLUTE" is "OFF", relative data are handled.

When the button "ABSOLUTE" is "ON", the slide lever presents a representation ranging from 0 to 100%.

FIG. **61** shows, by way of example, a displayed image for establishing black set parameters.

FIG. **62** shows, by way of example, a displayed image for establishing flare parameters.

FIG. **63** shows, by way of example, a displayed image for establishing matrix parameters.

FIG. **64** shows, by way of example, a displayed image for establishing matrix parameters, the displayed image including a displayed waveform.

FIG. **65**A is illustrative of a matrix.

When the title "MATRIX" is "OFF" and the title "CONTROL" is "OFF", a point ("x" in a waveform image) according to default settings (with no corrective coefficient) determined by equations of luminance Y, color differences R-Y, B-Y is displayed.

When the title "MATRIX" is "OFF" and the title "CONTROL" is "ON", a point determined by adding a value ranging from "a" to "f" to default settings, determining R', G', B', and substituting the determined R', G', B' in Y, R-Y B-Y is displayed.

When the title "MATRIX" is "ON" and the title "CONTROL" is "OFF", a point determined by determining R', G', B' with a coefficient given as a hardware default setting and substituting the determined R', G', B' in Y, R-Y, B-Y is displayed.

When the title "MATRIX" is "ON" and the title "CONTROL" is "ON", a point determined by adding a value ranging from "a" to "f" to a coefficient given as a hardware default setting and substituting the determined R', G', B' in Y, R-Y, B-Y is displayed.

$$Y=0.587G+0.299R+0.114B$$

$$R-Y=-0.587G+0.701R-0.114B$$

$$B-Y=-0.587G-0.299R+0.886B$$

$$R'=R+a(G-R)+b(B-R)$$

$$G'=G+c(R-G)+d(B-G)$$

$$B'=B+e(R-B)+f(G-B)$$

a=value of(G−R)R

b=value of (B−R)R

c=value of (R−G)G
d=value of (B−G)G
e=value of (R−B)B
f=value of (G−B)B

A coefficient ranging from "a" to "f" is established, R', G', B, are determined, and the determined R', G', B' are substituted in Y, R-Y, B-Y, to thereby determine a point on vector.

Display points are displayed in six colors, given below, except gray and black, of the 8 colors of the color bar. R, G, B (R', G', B' if "a"~"f" are added) are substituted in the equations of Y, R-Y, B-Y to calculate values of R-Y, B-Y, and points are displayed on vector.

Yellow (Y), Cyan (CY), Green (G), Magenta (M), Red (R), and Blue (B).

For vector display, R-Y/1.14 and B-Y/2.03 are used as R-Y and B-Y, respectively.

FIG. **65**B illustrates a matrix as it is turned off.

FIG. **66**A shows, by way of example, a displayed image for establishing gamma parameters.

In FIG. **66**A, the switch "COURSE" is used to select a gamma curve. Adjustments made using the slide levers effect an addition to the selected gamma curve.

FIG. **66**B shows, by way of example, a displayed image for establishing gamma parameters, the displayed image including a displayed waveform.

In FIG. **66**B, the switch "COURSE" is used to select a gamma curve. When the button "GAMMA" is "OFF", the waveform image is displayed as a linear line. The point P moves perpendicularly to the curve.

FIG. **67**A shows, by way of example, a displayed image for establishing black gamma parameters.

FIG. **67**B shows, by way of example, a displayed image for establishing black gamma parameters, the displayed image including a displayed waveform.

FIG. **68** shows, by way of example, a displayed image for establishing knee, white clip, gamma, black gamma parameters, the displayed image including a displayed waveform.

The buttons M, R, G, B are used to select signals with respect to which settings are to be made.

When the parameter "MIX" is selected, the waveform image is displayed together with functions corresponding to titles displayed on the left-hand side.

FIG. **69** shows, by way of example, a displayed image for establishing knee, white clip, gamma, black gamma parameters, the displayed image including a displayed waveform. The displayed image shown in FIG. **69** is the same as the displayed image shown in FIG. **68**.

FIG. **70** shows, by way of example, a displayed image for establishing black shading H parameters.

The button "AUTO BLACK SHADING" is used in the same manner as with the automatic setup process.

FIG. **71** shows, by way of example, a displayed image for establishing black shading V parameters.

FIG. **72** shows, by way of example, a displayed image for establishing black shading H/V parameters, the displayed image including displayed waveforms.

The buttons "H", "V", "R", "G", "B" are used to select items with respect to which settings are to be made.

FIG. **73** shows, by way of example, a displayed image for establishing white shading H parameters.

The button "EXTENDER" is used to indicate whether information from the lens system is obtained or not, and not to establish settings.

FIG. **74** shows, by way of example, a displayed image for establishing white shading V parameters.

FIG. **75** shows, by way of example, a displayed image for establishing white shading H/V parameters, the displayed image including displayed waveforms.

The button "EXTENDER" is used to display a status only.

FIG. **76**A shows, by way of example, a displayed image for establishing V modulation shading parameters.

FIG. **76**B shows, by way of example, a displayed image for establishing V modulation shading parameters, the displayed image including displayed waveforms.

The buttons "M", "R", "G", "B" are used to switch between displayed waveforms.

FIG. **77**A shows, by way of example, a displayed image for establishing transmit parameters.

FIG. **77**B shows, by way of example, a displayed image for establishing mic/line parameters.

FIG. **78** shows, by way of example, a displayed image for establishing mic/line parameters.

When "LINE" is selected at the parameter "INPUT SELECT", the parameter "POWER SELECT" is masked as shown because is it not used.

FIG. **79** shows, by way of example, a displayed image for establishing incom parameters.

FIG. **80**A shows, by way of example, a displayed image for establishing tracker parameters.

FIG. **80**B shows, by way of example, a displayed image for establishing external command parameters.

FIG. **81** shows, by way of example, a displayed image for establishing NTSC matrix (mix) parameters, the displayed image including a displayed graph.

In FIG. **81**, the solid dots "●" represent mixed audio data and the blank dots "○" represent audio data that can be mixed but are not mixed at present. "INCOM-**1**", "INCOM-**2**", "INCOM**1**", "INCOM**2**", "TRACKER", "PGM" represent the same audio signals which are indicated by those reference characters used in the explanation of FIG. **29**. The displayed menu "Matrix" indicates the same processing as that of the matrix circuit shown in FIG. **29**. This matrix processing is controlled on the display screen of the computer **100** by the controller **580** shown in FIG. **28** based on the contents of settings made in parameter setting images shown in FIGS. **82** through **87**.

The buttons "A"~"E" correspond to the alphabetic letters in parentheses at items displayed in the area "OUTPUT AUDIO", and are used to set mix levels. When an output system is selected, the buttons "A"~"E" select a mixing ratio with respect to the output system.

Switches "0" displayed in a lower area of the displayed image are selected for points where no audio signals are to be mixed. If the audio signal "PGM" is mixed with respect to the audio signals "PGM-**1**", "PGM-**2**", and "PGM-**3**", then the audio signal "PGM" is not mixed with respect to the audio signals "INCOM-**1**", "INCOM-**2**", and "TRACKER".

FIG. **82** shows, by way of example, a displayed image for establishing NTSC matrix (mix) parameters, the displayed image including a displayed graph.

In FIG. **82**, if one of the audio signals PGM is mixed, then the other audio signal PGM is not mixed in the displayed waveform image.

The switches "A:PGM SELECT", "B:PGM SELECT", "C:PGM SELECT" are used to select the type of audio signals PGM to be mixed.

The slide levers displayed below the above switches are used to set respective output levels of the signals.

FIG. **83** shows, by way of example, a displayed image for establishing PAL matrix (mix) parameters, the displayed image including a displayed graph.

FIG. **84** shows, by way of example, a displayed image for establishing PAL matrix (mix) parameters, the displayed image including a displayed graph.

FIG. **85** shows, by way of example, a displayed image for establishing PAL matrix (mix) parameters, the displayed image including a displayed graph.

FIGS. **86**A through **86**E show, by way of example, displayed images for processing memory accesses.

The displayed images represent items necessary to directly establish data with respect to LSI ports and memories of the cameras and CCUs, and extract data for checking. These items are present as an application separate from the application for setting parameters.

The data that can be established include data for LSI ports, data for I/O ports, data for servicing EEPROMs, data for gamma tables, and data for indicated memories.

FIG. **87** shows, by way of example, a displayed image for establishing LSI ports.

The established data are changed by rewriting addresses (numerical values on the left-hand side) directly with data. The data of those addresses which are associated with up/down buttons can continuously be varied between "00" and "FF" by the up/down buttons. The window image shown in FIG. **87** is present with respect to each of the LSI circuits.

According the present invention, as described above, since a camera or a CCU is set up using a graphical user interface, it can be set up efficiently, accurately, and reliably by the operator in an environment which enables the operator to control various setting operations easily.

In the above embodiment, the parameters are supplied from the computer **100** to the cameras and the CCUs. However, as can be seen from the displayed images shown in FIGS. **30**A, **30**B through **87** and the above embodiment, the parameter data may not be supplied directly to the cameras and the CCUs, but only parameter changes effected in parameter setting windows or the computer **100**, i.e., only relative data, may be supplied to the cameras and the CCUs in view of responses of the cameras and the CCUs and changes in displayed images.

As described above, the display state of a parameter changing switch is changed depending on input information, the display state of a setting state display image is changed depending on input information, and a parameter is changed. The changed parameter or the parameter change is transmitted to the controlled device to set up the controlled device. Therefore, the controlled device can be set up highly efficiently, accurately, and reliably.

Furthermore, the display state of a parameter changing switch, the display state of a setting state display image, and the value of a parameter, which are displayed on the display unit, are changed depending on input information supplied from the input unit. The changed parameter or the parameter change is transmitted to the controlled device to set up the controlled device. Therefore, the controlled device can be set up highly efficiently, accurately, and reliably.

Having described a preferred embodiment of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to that precise embodiment and that various changes and modifications could be effected by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended claims.

What is claimed is:

1. A method of setting up an electronic device by transmitting parameters indicated by a controller to said electronic device positioned separate from said controller and not utilized to set said parameters to set up said electronic device, comprising the steps of:

(a) displaying on a display associated with said controller a parameter setting image depicting a plurality of parameters that can be established with respect to said electronic device;

(b) deciding whether input information has been entered into said controller while the parameter setting image is being displayed on said display associated with said controller;

(c) changing a portion of the parameter setting image displayed on said display associated with said controller which corresponds to input information if such input information is entered;

(d) establishing parameter data according to the input information; and

(e) transmitting the established parameter data or a change in the parameter data to said electronic device positioned separate from said controller and not utilized to set said parameter data to change a parameter in said electronic device.

2. A method according to claim **1**, wherein said parameter setting image includes a parameter changing switch image or a setting state display image which moves or changes in the parameter setting image depending on the input information, and wherein said step (c) comprises the step of changing the display state of said parameter changing switch image depending on the input information, and/or the step of changing the setting state display image depending on the input information.

3. A method according to claim **2**, wherein said step (d) comprises the step of saving the established parameter data as a file, and said step (e) comprises the step of transmitting all the parameter data saved as the file to the controlled device to change the parameter in the controlled device.

4. A method according to claim **2**, wherein said step (e) comprises the step of adding at least control device identification data indicative of the controlled device, control data indicative of a change in the parameter data, and parameter identification data indicative of the parameter, to the parameter data transmitted to the controlled device.

5. A method according to claim **4**, further comprising the steps of:

receiving the data transmitted from said controller in the controlled device;

converting a communication protocol of the received data in the controlled device;

recognizing the parameter to be changed with the parameter identification data in the data whose communication protocol has been converted, in the controlled device; and

changing the parameter in the controlled device based on the recognized parameter and the parameter data.

6. A method according to claim **2**, wherein a data converter for converting a transmission format is disposed between the controller and the controlled device, further comprising the steps of:

receiving the data transmitted from the controller in the data converter;

converting a communication protocol of the received data in the data converter; and

transmitting the data whose communication protocol has been converted, from the data converter to the controlled device.

7. A method according to claim **2**, wherein the controlled device comprises a video camera having signal processing capabilities or a camera system comprising a camera device and a control unit.

8. A method of setting up an electronic device by transmitting parameters indicated by a controller to said electronic device positioned separate from said controller and not used to set parameters to set up said electronic device, comprising the steps of:

(a) displaying on a display associated with said controller a parameter setting image depicting a plurality of

parameters that can be established with respect to said electronic device, said parameter setting image including a parameter changing switch image and/or a setting state display image whose display state changes depending on input information;

(b) deciding whether input information has been entered into said controller while the parameter setting image is being displayed on said display associated with said controller;

(c) changing the display state of said parameter changing switch image and/or said setting state display image displayed on said display associated with said controller which corresponds to input information if such input information is entered;

(d) establishing parameter data according to the input information;

(e) transmitting the established parameter data or a change in the parameter data from said controller to said electronic device positioned separate from said controller and not utilized to set said parameter data to change a parameter in said electronic device; and

(f) changing the parameter in said electronic device positioned separate from said controller based on the parameter data or the change in the parameter data transmitted from said controller.

9. A method according to claim **8**, wherein said step (d) comprises the step of saving the established parameter data as a file, and said step (e) comprises the step of transmitting all the parameter data saved as the file to the controlled device to change the parameter in the controlled device.

10. A method according to claim **8**, wherein said step (e) comprises the step of adding at least control device identification data indicative of the controlled device, control data indicative of a change in the parameter data, and parameter identification data indicative of the parameter, to the parameter data transmitted to the controlled device.

11. A method according to claim **8**, further comprising the steps of:

receiving the data transmitted from said controller in the controlled device;

converting a communication protocol of the received data in the controlled device;

recognizing the parameter to be changed with the parameter identification data in the data whose communication protocol has been converted, in the controlled device; and

changing the parameter in the controlled device based on the recognized parameter and the parameter data.

12. A method according to claim **8**, further comprising the step of:

(g) converting a transmission format between the controller and the controlled device;

and wherein said step (g) comprises the steps of:

receiving the data transmitted from the controller;

converting a communication protocol of the received data; and

transmitting the data whose communication protocol has been converted, to the controlled device.

13. A method according to claim **8**, wherein the controlled device comprises a video camera having signal processing capabilities or a camera system comprising a camera device and a control unit.

14. An apparatus for setting up an electronic device, comprising:

storage means for storing parameter setting image data for establishing one or more parameters with respect to said electronic device not utilized to establish said one or more parameters, said parameter setting image including parameter changing switch image data and setting state display image data;

display means for displaying a parameter setting image based on and depicting the parameter setting image data read from said storage means;

input means for entering input information indicating changes in display states of a parameter changing switch image data and a setting state display image which are displayed by said display means and a parameter to be established; and

control means positioned separate from said electronic device for changing the display states of the parameter changing switch image data and the setting state display image which are displayed by said display means and the parameter to be established, based on the input information entered by said input means, and transmitting changed parameter data or a change in the parameter to said electronic device positioned separate from said control means and not utilized to establish said parameter data.

15. An apparatus according to claim **14**, wherein said control means comprises:

position recognizing means for recognizing the position of a pointer in the parameter setting image displayed by said display means, based on the input information entered by said input means; and

parameter generating means for generating parameter data based on the input information entered by said input means.

16. An apparatus according to claim **15**, wherein said control means comprises:

means for saving the established parameter or parameters as a file, and transmitting all the parameter data saved as the file to the controlled device.

17. An apparatus according to claim **16**, wherein said control means comprises:

means for adding at least control device identification data indicative of the controlled device, control data indicative of a change in the parameter data, and parameter identification data indicative of the parameter, to the parameter data transmitted to the controlled device.

18. An apparatus according to claim **17**, wherein said controlled device comprises:

means for receiving the data transmitted from said control means, converting a communication protocol of the received data, recognizing the parameter to be changed with the parameter identification data in the data whose communication protocol has been converted, and changing the parameter based on the recognized parameter and the parameter data.

19. An apparatus according to claim **16**, further comprising:

a data converter disposed between the controller and the controlled device, for converting a communication protocol of the parameter data transmitted from said control means, and transmitting the data whose communication protocol has been converted, to the controlled device.

20. An apparatus according to claim **14**, wherein said controlled device comprises a video camera having signal processing capabilities or a camera system comprising a camera device and a control unit.

21. An apparatus according to claim **20**, wherein said control means comprises display means for displaying a

video signal supplied from said a video camera or said camera device or said control unit.

22. An apparatus for setting up an electronic device, comprising:

storage means for storing parameter setting image data for establishing one or more parameters with respect to a controlled device, said parameter setting image including parameter changing switch image data and setting state display image data;

display means for displaying a parameter setting image based on and depicting the parameter setting image data read from said storage means;

input means for entering input information indicating chances in display states of a parameter changing switch image data and a setting state display image which are displayed by said display means and a parameter to be established; and

control means positioned separate from said controlled device for changing the display states of the parameter changing switch image data and the setting state display image which are displayed by said display means and the parameter to be established, based on the input information entered by said input means, and transmitting changed parameter data or a change in the parameter to the controlled device positioned separate from said control means;

said display means displaying a plurality of components, including at least a plurality of available input devices, or controlled devices, a plurality of associated camera control units, a camera network unit controller, a video camera selector, and interconnections therebetween; and

said input means is also adapted for designating one of said displayed plurality of available input devices, or controlled devices,

wherein designation of said one input device or controlled device electrically connects said designated input device or controlled device to said network in accordance with said interconnections, thereby allowing said changed parameter data to be transmitted to said designated input device or controlled device.

23. The apparatus of claim **22**, wherein said interconnections indicate potential data transfer paths between various of the displayed components.

24. The apparatus of claim **22**, wherein at least one of said plurality of input devices is a video recorder.

25. The apparatus of claim **22**, wherein said designated input device is indicated on said display means.

26. The apparatus of claim **22**, further comprising parameter setting means for setting various parameters in accordance with said designated input device.

27. The apparatus of claim **26**, further comprising control means for transmitting said various parameter settings or changes to said various parameter settings to said designated device.

* * * * *

EXHIBIT D

US006009233A

United States Patent [19]

Tsujimura et al.

[11] **Patent Number: 6,009,233**

[45] **Date of Patent: *Dec. 28, 1999**

[54] **APPARATUS AND METHOD FOR RECORDING AND REPRODUCING A VIDEO SIGNAL WITH CAMERA SETTING DATA**

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[73] Assignee: **Sony Corporation**, Tokyo, Japan

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/697,456**

[22] Filed: **Aug. 23, 1996**

[30] **Foreign Application Priority Data**

Aug. 31, 1995 [JP] Japan 7-224406

[51] **Int. Cl.**[6] **H04N 5/91**; H04N 5/928

[52] **U.S. Cl.** **386/95**; 386/107

[58] **Field of Search** 386/95, 107, 117, 386/118, 46–38; 348/207, 208, 213, 222, 232, 262

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,736,849	6/1973	Thompson	386/118
3,843,956	10/1974	Kauneckas	386/107
5,270,831	12/1993	Parulski et al. .	
5,386,117	1/1995	Piety et al.	250/330
5,477,264	12/1995	Sarbadhikari et al.	348/222
5,627,616	5/1997	Sergeant et al.	354/81

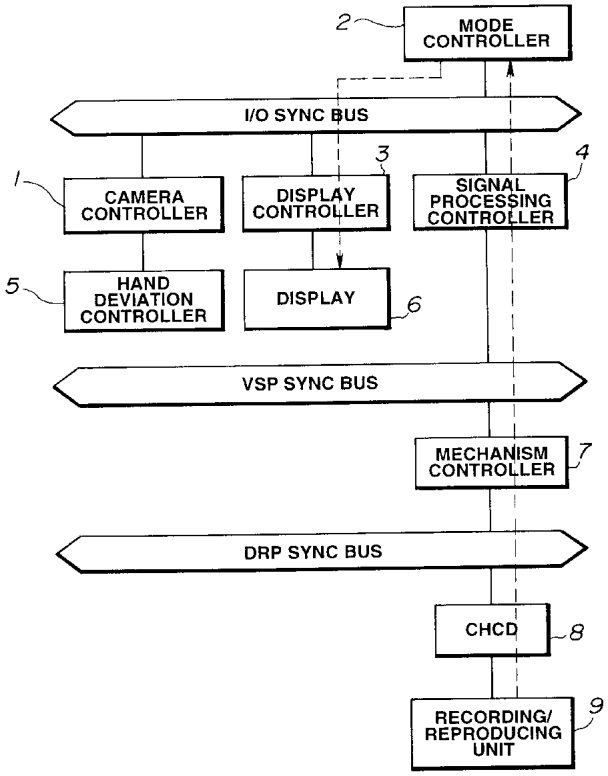
Primary Examiner—Robert Chevalier

Attorney, Agent, or Firm—Frommer, Lawrence & Haug, LLP.; William S. Frommer

[57] **ABSTRACT**

A camera having a digital video tape recorder integrated therein establishes various camera settings in preparation of imaging a video image, images the video image so as to produce a video signal, generates camera setting data which identifies the various camera settings (e.g., iris setting, shutter speed, white balance mode and focusing mode) that were established for imaging the video image, and records the video signal in a first location of a track on a record medium, e.g., a magnetic tape, and records the camera setting data in a second location of the track on the record medium. When the video signal and camera setting data are reproduced from the record medium, display data is generated from the reproduced camera setting data and is output along with the video signal so as to allow a user to modify (i.e., process) the video signal using the stored camera setting data.

33 Claims, 34 Drawing Sheets



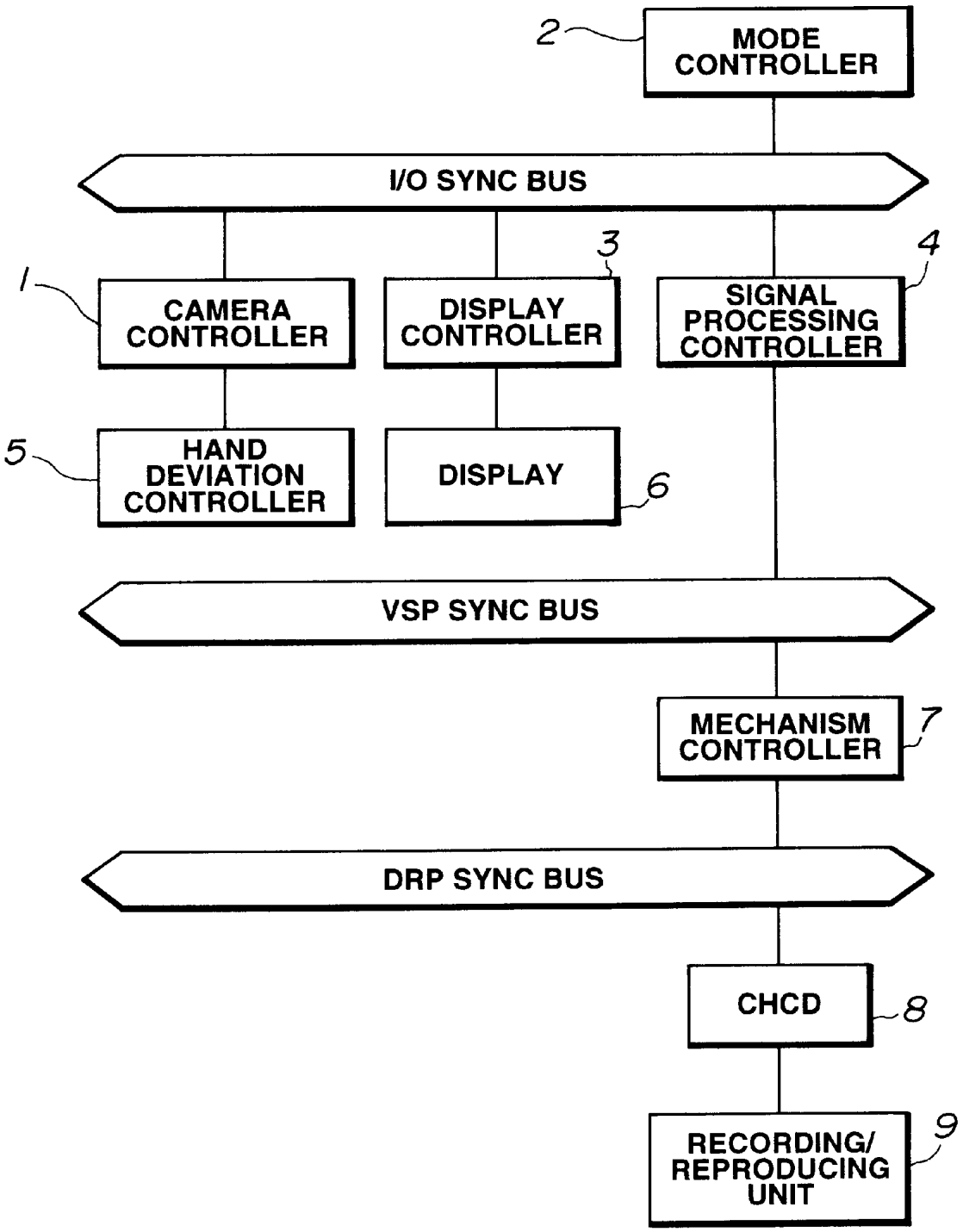

2
MODE CONTROLLER
I/O SYNC BUS
1
CAMERA CONTROLLER
3
DISPLAY CONTROLLER
4
SIGNAL PROCESSING CONTROLLER
5
HAND DEVIATION CONTROLLER
DISPLAY
6
VSP SYNC BUS
MECHANISM CONTROLLER
7
DRP SYNC BUS
CHCD
8
RECORDING/ REPRODUCING UNIT
9

FIG.1

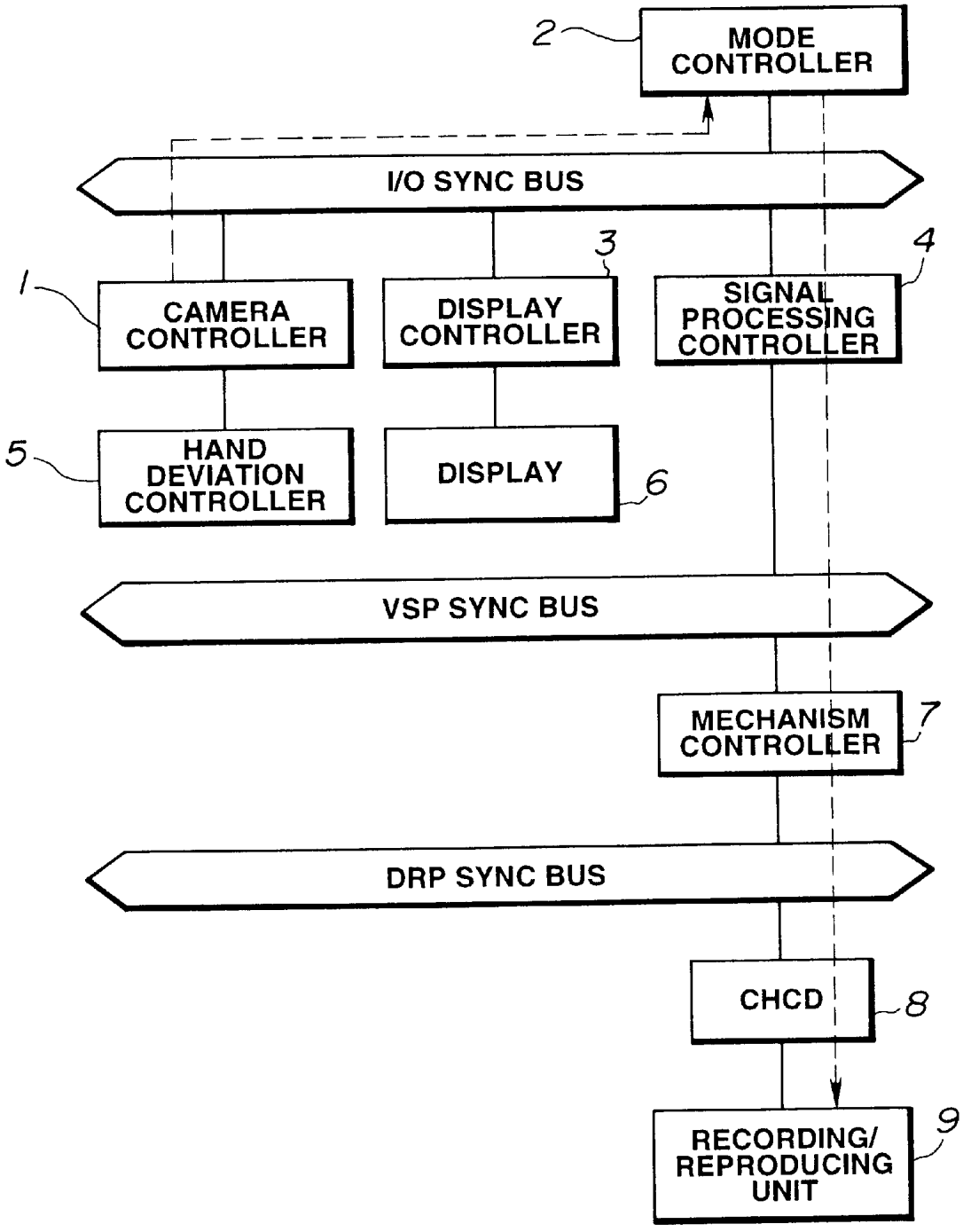

2
MODE CONTROLLER
I/O SYNC BUS
1
CAMERA CONTROLLER
3
DISPLAY CONTROLLER
4
SIGNAL PROCESSING CONTROLLER
5
HAND DEVIATION CONTROLLER
DISPLAY
6
VSP SYNC BUS
MECHANISM CONTROLLER
7
DRP SYNC BUS
CHCD
8
RECORDING/ REPRODUCING UNIT
9

FIG.2

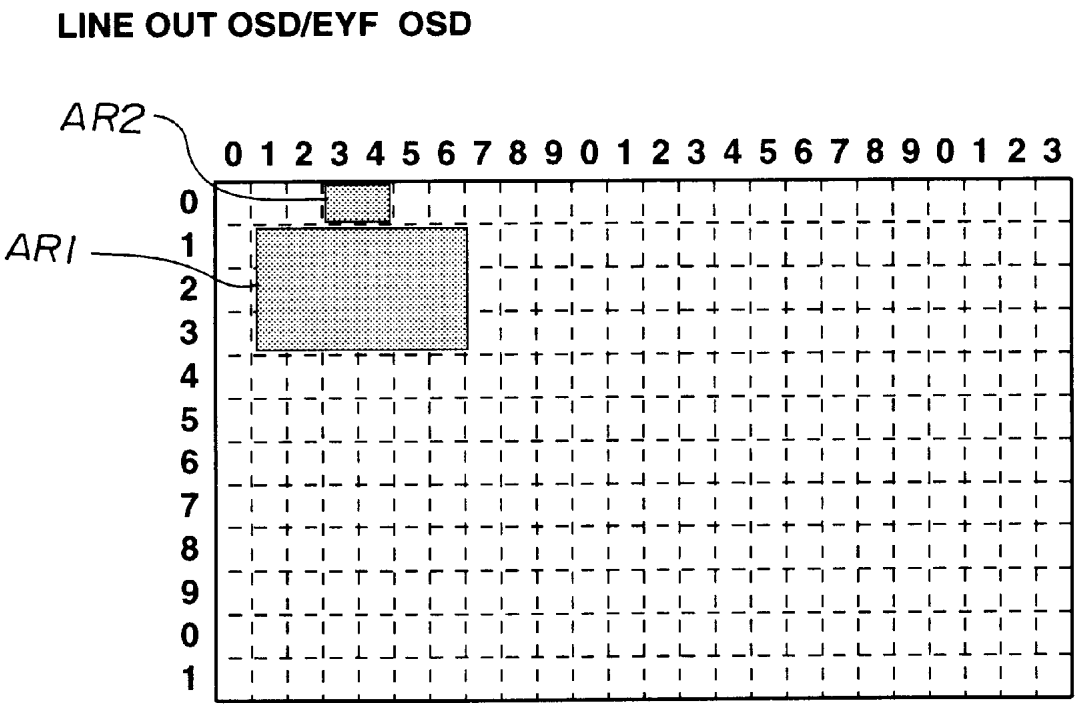

LINE OUT OSD/EYF OSD
AR2
AR1
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3
0
1
2
3
4
5
6
7
8
9
0
1

FIG.3

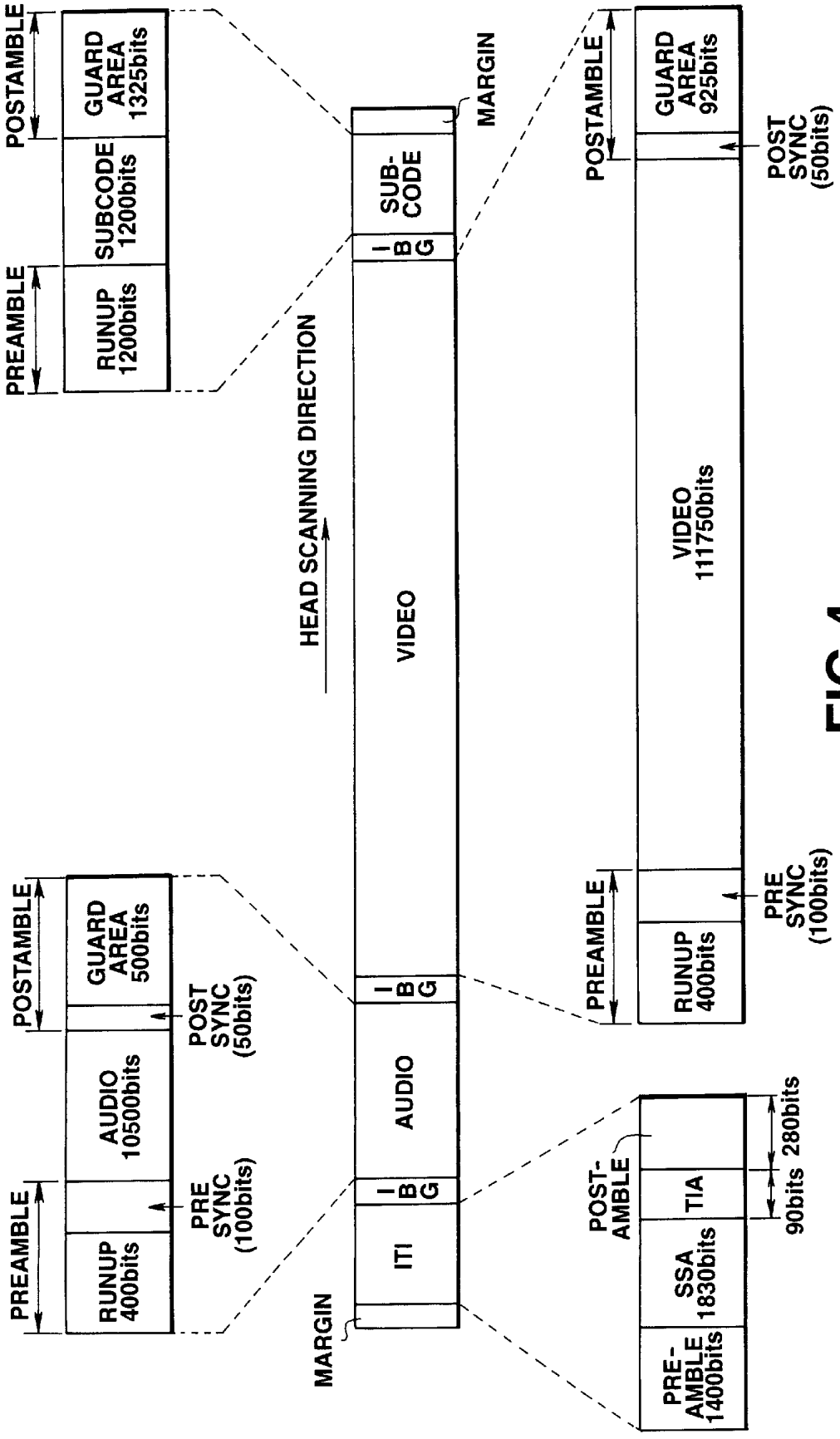

POSTAMBLE
GUARD AREA 1325bits
SUBCODE 1200bits
PREAMBLE
RUNUP 1200bits
MARGIN
SUB-CODE
I B G
HEAD SCANNING DIRECTION
VIDEO
POSTAMBLE
GUARD AREA 925bits
POST SYNC (50bits)
VIDEO 111750bits
PREAMBLE
RUNUP 400bits
PRE SYNC (100bits)
POSTAMBLE
GUARD AREA 500bits
POST SYNC (50bits)
AUDIO 10500bits
PREAMBLE
RUNUP 400bits
PRE SYNC (100bits)
I B G
AUDIO
I B G
ITI
MARGIN
POST-AMBLE
TIA
90bits
280bits
SSA 1830bits
PRE-AMBLE 1400bits

FIG.4

FIG.5A

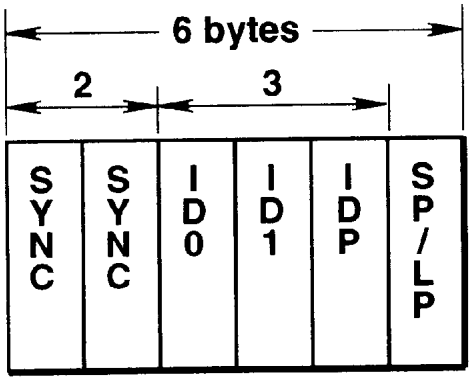
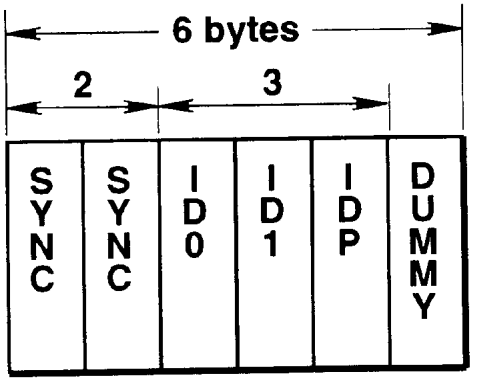

PRE SYNC BLOCK
6 bytes
2
3
SYNC
SYNC
ID0
ID1
IDP
SP/LP

FIG.5B


POST SYNC BLOCK
6 bytes
2
3
SYNC
SYNC
ID0
ID1
IDP
DUMMY

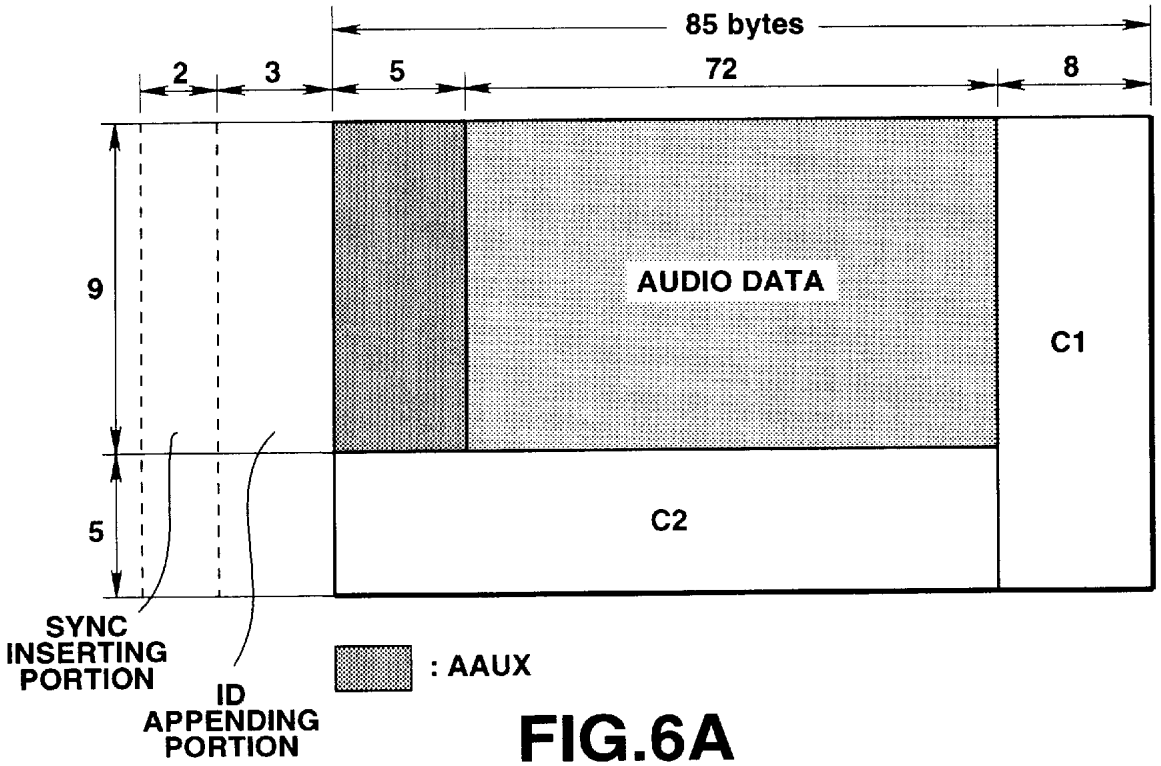

85 bytes
2
3
5
72
8
9
5
AUDIO DATA
C1
C2
SYNC INSERTING PORTION
ID APPENDING PORTION
: AAUX

FIG.6A

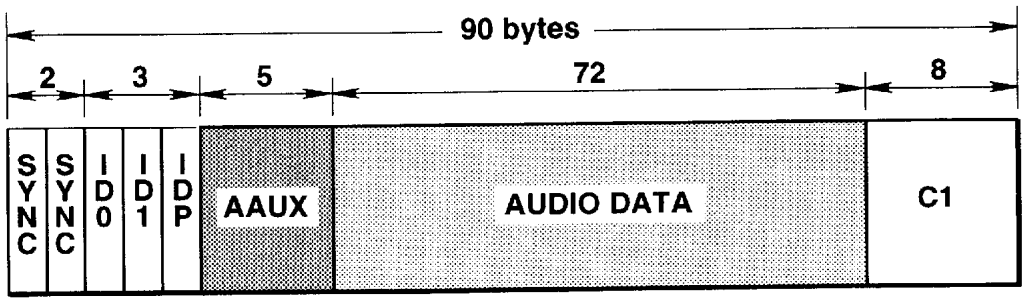

90 bytes
2
3
5
72
8
SYNC
SYNC
ID0
ID1
IDP
AAUX
AUDIO DATA
C1

FIG.6B

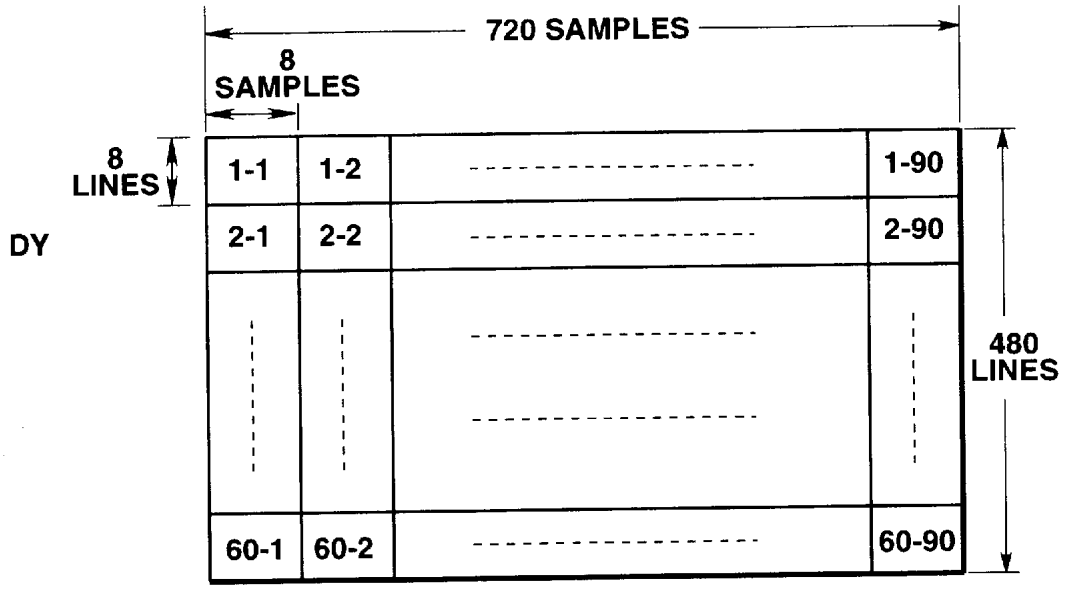

720 SAMPLES
8 SAMPLES
8 LINES
DY
1-1
1-2
1-90
2-1
2-2
2-90
480 LINES
60-1
60-2
60-90

FIG.7A

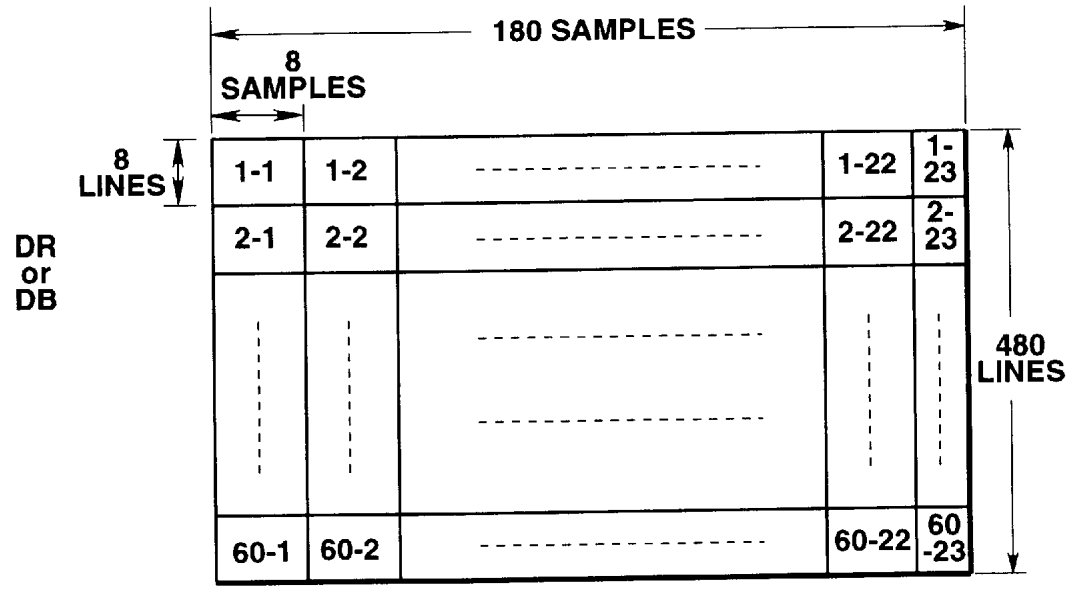

180 SAMPLES
8 SAMPLES
8 LINES
DR or DB
1-1
1-2
1-22
1-23
2-1
2-2
2-22
2-23
480 LINES
60-1
60-2
60-22
60-23

FIG.7B

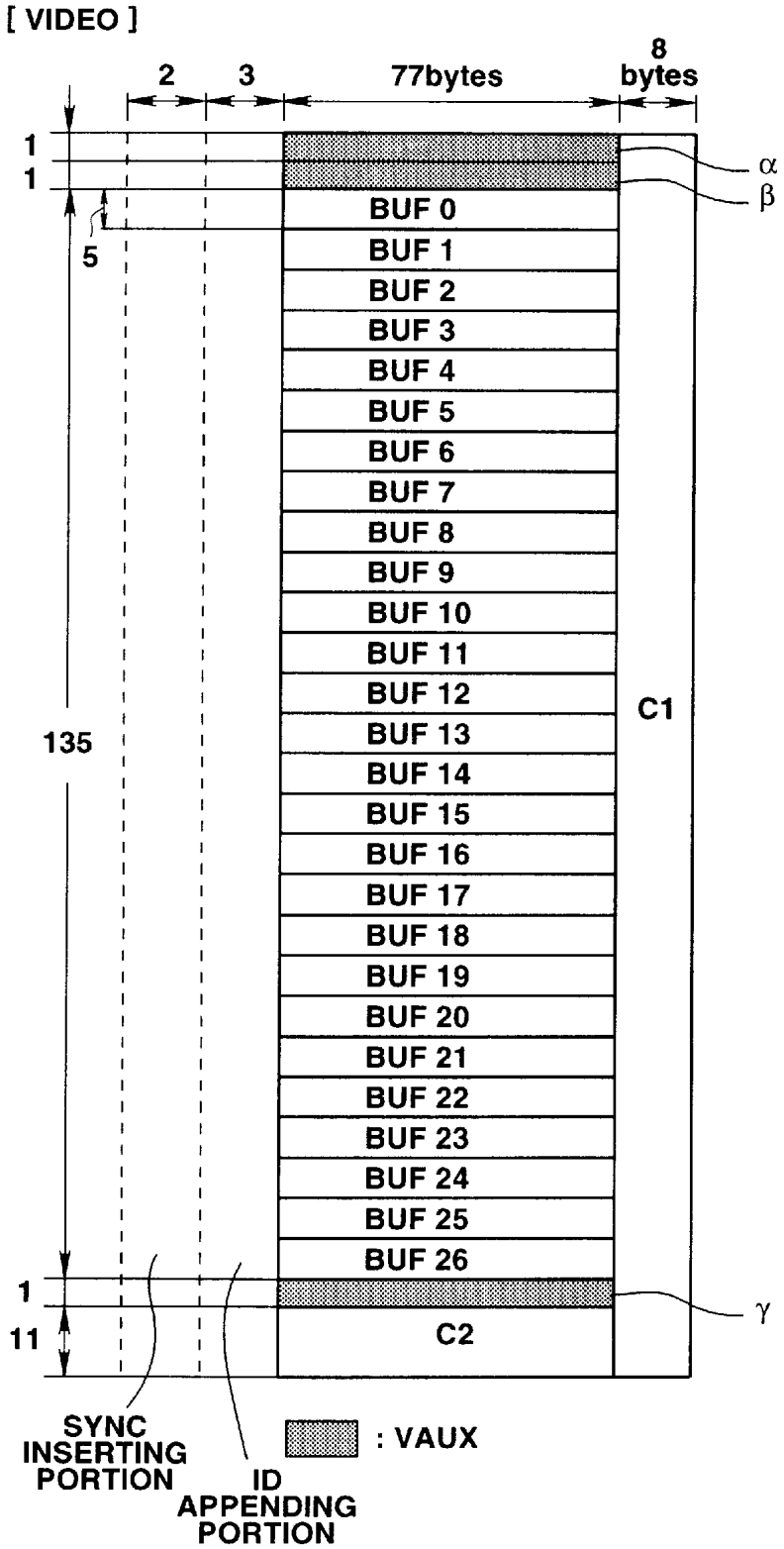

[VIDEO]
2
3
77bytes
8 bytes
1
1
5
135
1
11
α
β
γ
BUF 0
BUF 1
BUF 2
BUF 3
BUF 4
BUF 5
BUF 6
BUF 7
BUF 8
BUF 9
BUF 10
BUF 11
BUF 12
BUF 13
BUF 14
BUF 15
BUF 16
BUF 17
BUF 18
BUF 19
BUF 20
BUF 21
BUF 22
BUF 23
BUF 24
BUF 25
BUF 26
C1
C2
SYNC INSERTING PORTION
ID APPENDING PORTION
: VAUX

FIG.8

FIG.9A

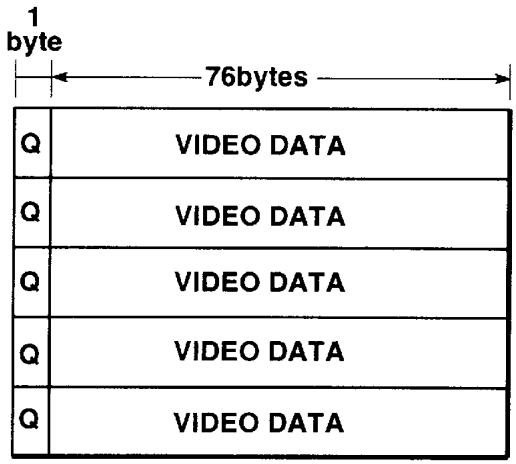


FIG.9B

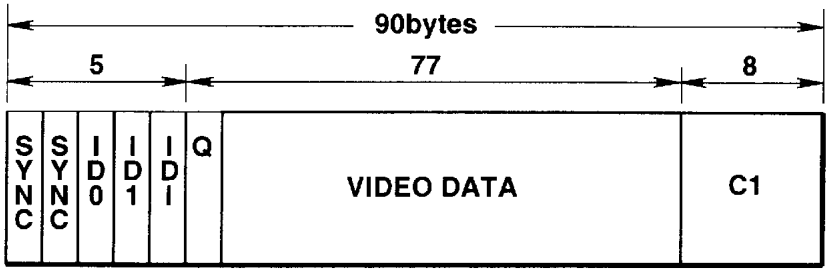
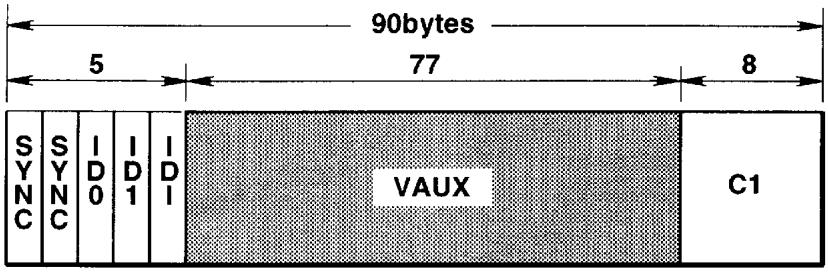


FIG.9C



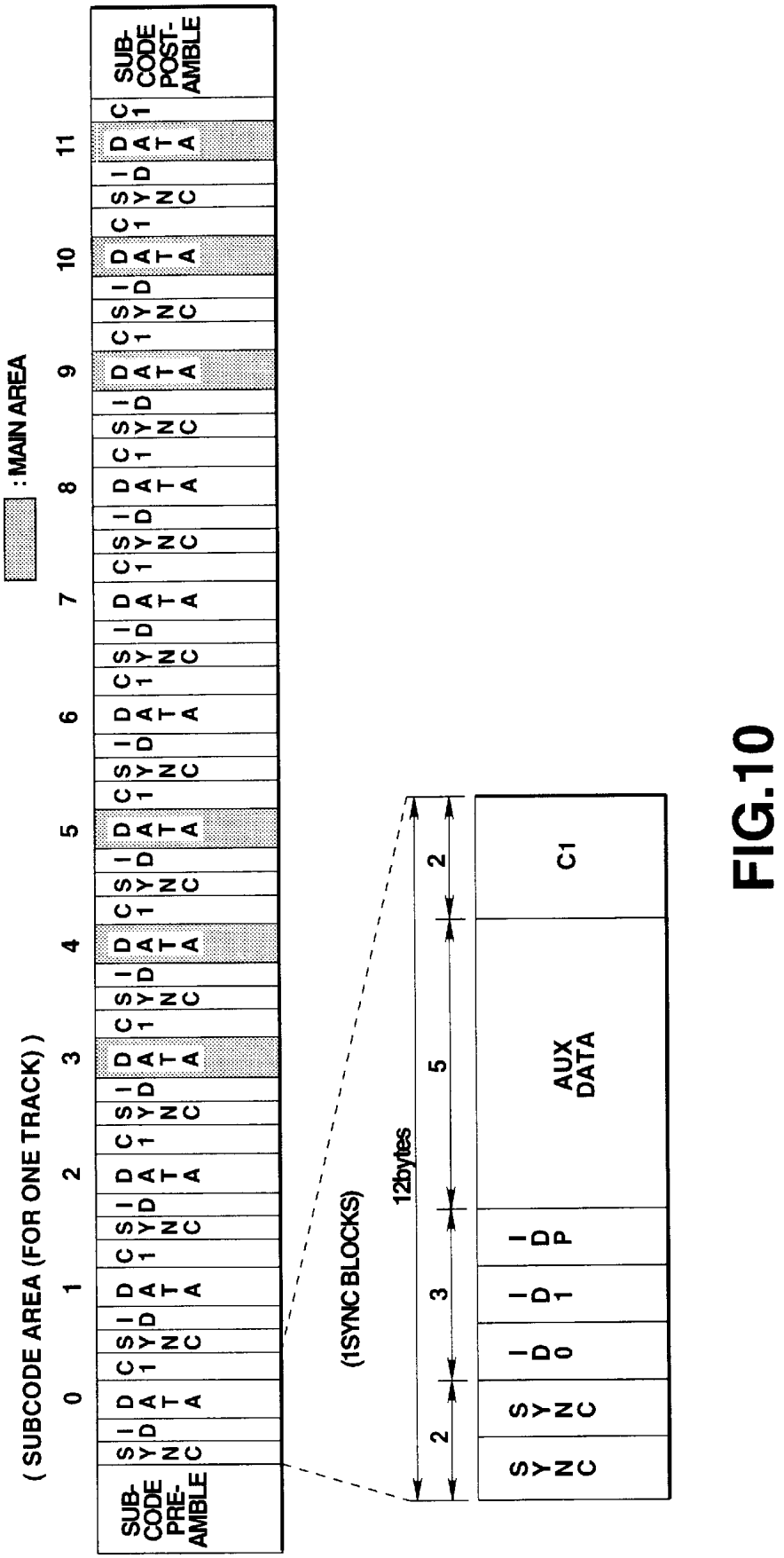

: MAIN AREA
(SUBCODE AREA (FOR ONE TRACK))
0
1
2
3
4
5
6
7
8
9
10
11
SUB-CODE PRE-AMBLE
SUB-CODE POST-AMBLE
(1SYNC BLOCKS)
12bytes
2
5
3
2
SYNC
ID0
ID1
IDP
AUX DATA
C1

FIG.10

AAUX+AUDIO SYNC,
VIDEO SYNC.

	ID 0	ID 1
MSB	SEQ 3	SYNC 7
	SEQ 2	SYNC 6
	SEQ 1	SYNC 5
	SEQ 0	SYNC 4
	TRACK 3	SYNC 3
	TRACK 2	SYNC 2
	TRACK 1	SYNC 1
LSB	TRACK 0	SYNC 0

FIG.11A

PRE SYNC,
POST SYNC,
C2 PARITY SYNC.

	ID 0	ID 1
MSB	AP1/AP2 2	SYNC 7
	AP1/AP2 1	SYNC 6
	AP1/AP2 0	SYNC 5
	SEQ 0	SYNC 4
	TRACK 3	SYNC 3
	TRACK 2	SYNC 2
	TRACK 1	SYNC 1
LSB	TRACK 0	SYNC 0

FIG.11B

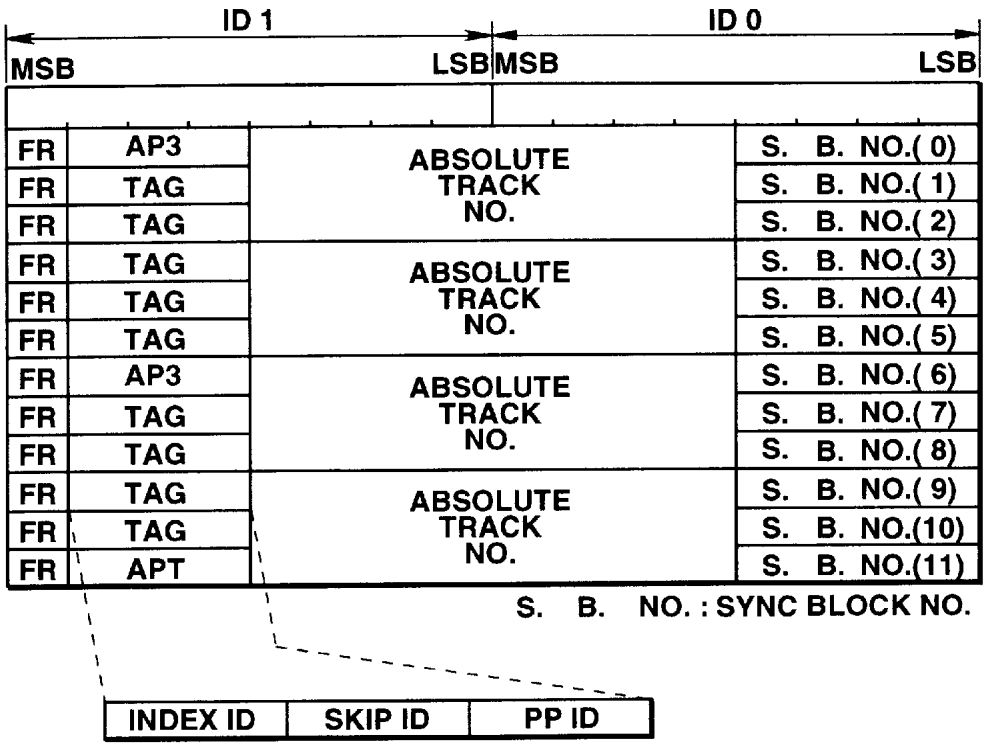


FIG.12

WORD NAME		MSB LSB
PC0	(ITEM)	
PC1	(DATA)	
PC2		
PC3		
PC4		

FIG.13

MSB UPPER	LSB LOWER	
0 0 0 0	x x x x	CONTROL
0 0 0 1	x x x x	TITLE
0 0 1 0	x x x x	CHAPTER
0 0 1 1	x x x x	PART
0 1 0 0	x x x x	PROGRAM
0 1 0 1	x x x x	AAUX
0 1 1 0	x x x x	VAUX
0 1 1 1	x x x x	CAMERA
1 0 0 0	x x x x	LINE
1 0 0 1 ~ 1 1 1 0	x x x x	RESERVED
1 1 1 1	a a a a	SOFT MODE
1 1 1 1	1 1 1 1	NO INFORMATION

a a a a : 0 0 0 0 ~ 1 1 1 0
x x x x : 0 0 0 0 ~ 1 1 1 1

FIG.14

FIG.15A

AAUX SOURCE

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	1	AF SIZE					
PC2	CH			PA	AUDIO MODE			
PC3	1	1	50/60	STYPE				
PC4	EF	TC	SMP			QU		

FIG.15B

AAUX SOURCE CONTROL

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	SCMS		COPY SOUR.	COPY GENE.		CP	CI	
PC2	REC ST.	REC E.	REC MODE	1	1	1	1	
PC3	DRF	SPEED						
PC4	1	GENRE CATEGORY						

REC ST. : RECORDING START FRAME
REC E. : RECORDING END FRAME

FIG.15C

AAUX REC DATE

	MSB							LSB
PC0	0	1	0	1	0	0	1	0
PC1	DS	TM	TIME ZONE					
PC2	1	1	DAY					
PC3	WEEK		MONTH					
PC4	YEAR							

FIG.15D

AAUX REC TIME

	MSB							LSB
PC0	0	1	0	1	0	0	1	1
PC1	S2	S1	TENS OF PR.	UNITS OF FRAMES				
PC2	S3	TENS OF SECONDS	UNITS OF SECONDS					
PC3	S4	TENS OF MINUTES	UNITS OF MINUTES					
PC4	S6	S5	TENS OF H.	UNITS OF HOURS				

FIG.15E

AAUX REC TIME BINARY GROUP

	MSB							LSB
PC0	0	1	0	1	0	1	0	0
PC1	2nd BINARY				1st BINARY			
PC2	4th BINARY				3rd BINARY			
PC3	6th BINARY				5th BINARY			
PC4	8th BINARY				7th BINARY			

FIG.16A

AAUX CLOSED CAPTION

	MSB							LSB
PC0	0	1	0	1	0	1	0	1
PC1	1	1	MAIN AUDIO LANG.			MAIN AUDIO TYPE		
PC2	1	1	2ND AUDIO LANG.			2ND AUDIO TYPE		
PC3	1	1	1	1	1	1	1	1
PC4	1	1	1	1	1	1	1	1

FIG.16B

VAUX SOURCE

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	TENS OF TV CHANNEL				UNITS OF TV CHANNEL			
PC2	B/W	EN	CLF		HUNDREDS OF TV CHANNEL			
PC3	SOURCE CODE		50/60	STYPE				
PC4	TUNER CATEGORY							

FIG.16C

VAUX SOURCE CONTROL

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	SCMS		COPY SOUR.		COPY GENE.		CP	CI
PC2	REC ST.	1	REC MODE		1	DISP		
PC3	FF	FS	FC	IL	ST	SC	BCSYS	
PC4	1	GENRE CATEGORY						

FIG.16D

VAUX REC DATE

	MSB							LSB
PC0	0	1	1	0	0	0	1	0
PC1	DS	TM	TIME ZONE					
PC2	1	1	DAY					
PC3	WEEK		MONTH					
PC4	YEAR							

FIG.16E

VAUX REC TIME

	MSB							LSB
PC0	0	1	1	0	0	0	1	1
PC1	S2	S1	TENS OF FR.		UNITS OF FRAMES			
PC2	S3	TENS OF SECONDS			UNITS OF SECONDS			
PC3	S4	TENS OF MINUTES			UNITS OF MINUTES			
PC4	S6	S5	TENS OF H.		UNITS OF HOURS			

FIG.17A

VAUX REC TIME BINARY GROUP

	MSB							LSB
PC0	0	1	1	0	0	1	0	0
PC1	2nd BINARY				1st BINARY			
PC2	4th BINARY				3rd BINARY			
PC3	6thBINARY				5th BINARY			
PC4	8th BINARY				7th BINARY			

FIG.17B

VAUX CLOSED CAPTION

	MSB							LSB
PC0	0	1	1	0	0	1	0	1
PC1	1st FIBLD LINE 21 UPPER BYTE							
PC2	1st FIBLD LINE 21 LOWER BYTE							
PC3	2nd FIBLD LINE 21 UPPER BYTE							
PC4	2nd FIBLD LINE 21 LOWER BYTE							

[AAUX PACK STRUCTURE]

TRACK NO. →	1	2	3	4	5	6	7	8	9	10
8	55		55		55		55		55	
7	54		54		54		54		54	
6	53		53		53		53		53	
5	52	55	52	55	52	55	52	55	52	55
4	51	54	51	54	51	54	51	54	51	54
3	50	53	50	53	50	53	50	53	50	53
2		52		52		52		52		52
1		51		51		51		51		51
0		50		50		50		50		50

PACK NO. ↑

50 ~ 55 : AAUX MAIN AREA

NUMBER OF REAL DATA IN OPTIONAL AREA : 120bytes

FIG.18

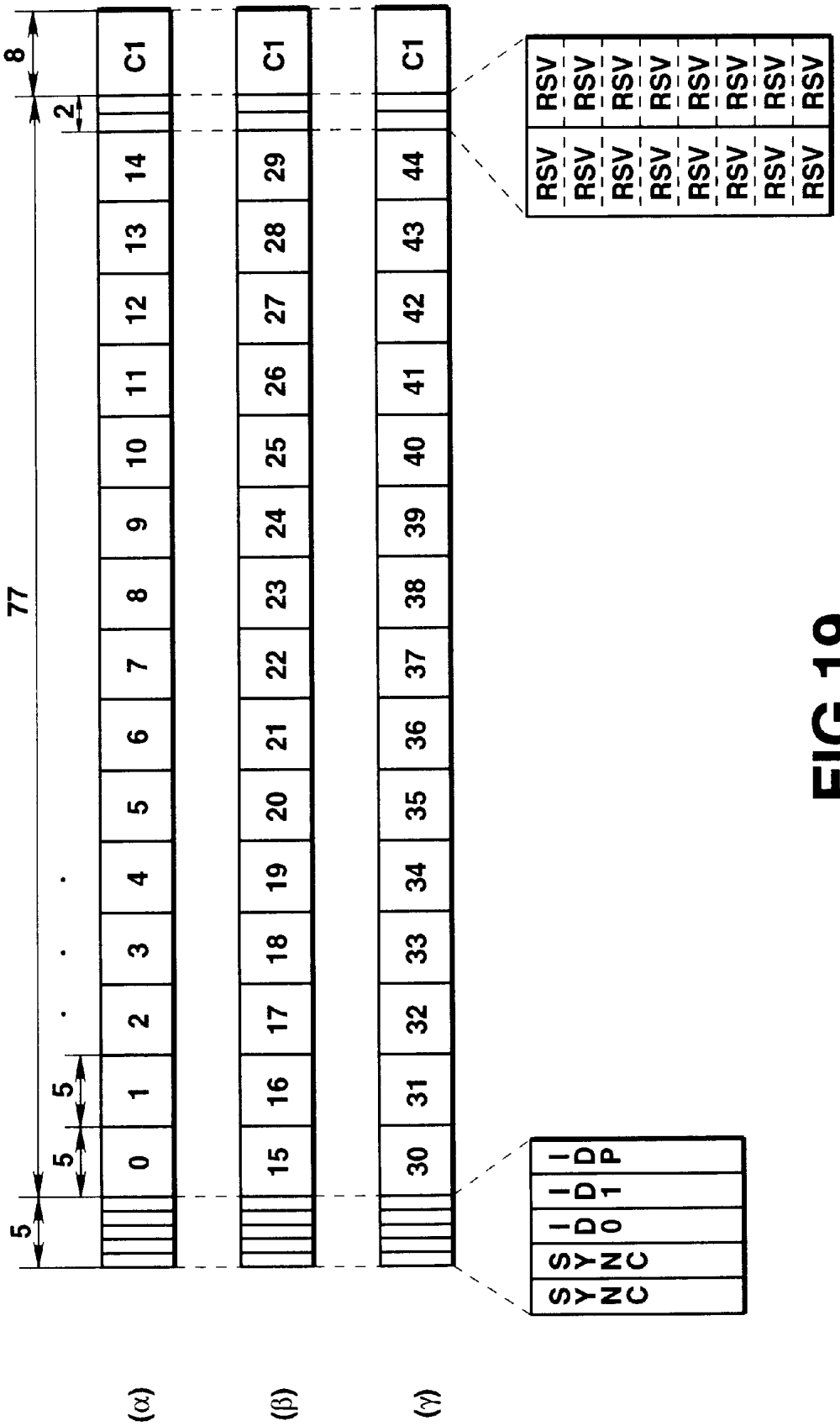

8
2
77
5
5
5
C1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
RSV
SYNC
SYS
IDD0
IDD1
IDDP
(α)
(β)
(γ)

FIG.19

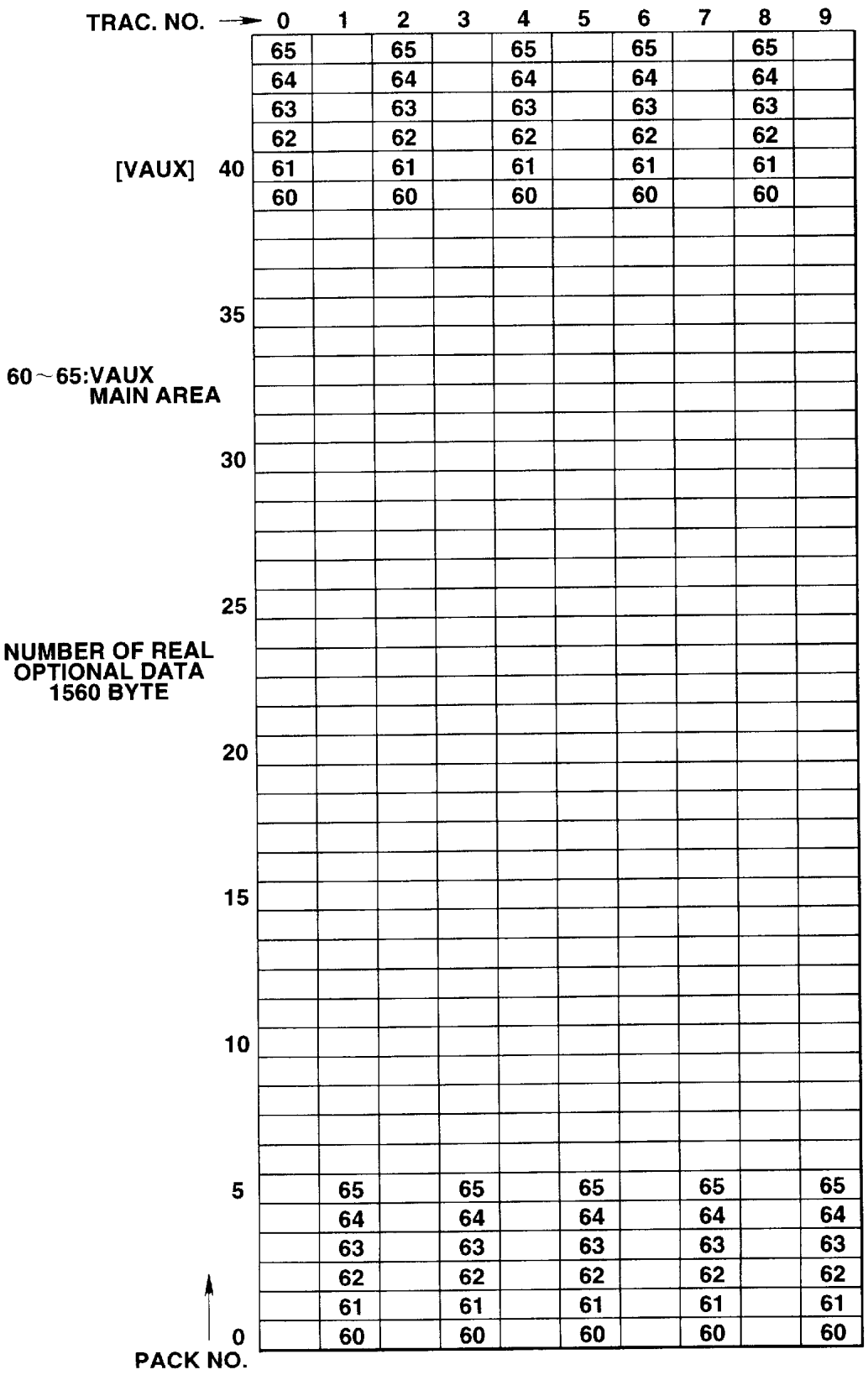

TRAC. NO.
0 1 2 3 4 5 6 7 8 9
[VAUX]
40
35
30
25
20
15
10
5
0
PACK NO.
60～65:VAUX MAIN AREA
NUMBER OF REAL OPTIONAL DATA 1560 BYTE
65
64
63
62
61
60

FIG.20

TRACK NO. →	0	1	2	3	4	5	6	7	8	9
11	C	C	C	C	C	E	E	E	E	E
10	B	B	B	B	B	D	D	D	D	D
9	A	A	A	A	A	A	A	A	A	A
8	f	c	f	c	f	m	i	m	i	m
7	e	b	e	b	e	k	h	k	h	k
6	d	a	d	a	d	j	g	j	g	j
5	C	C	C	C	C	E	E	E	E	E
4	B	B	B	B	B	D	D	D	D	D
3	A	A	A	A	A	A	A	A	A	A
2	c	f	c	f	c	i	m	i	m	i
1	b	e	b	e	b	h	k	h	k	h
0	a	d	a	d	a	g	j	g	j	g

SYNC BLOCK NO. ↑

FIG.21

TRACK NO. →	0	1	2	3	4	5	6	7	8	9	10	11
11	C	C	C	C	C	C	E	E	E	E	E	E
10	B	B	B	B	B	B	D	D	D	D	D	D
9	A	A	A	A	A	A	A	A	A	A	A	A
8	f	c	f	c	f	c	m	i	m	i	m	i
7	e	b	e	b	e	b	k	h	k	h	k	h
6	d	a	d	a	d	a	j	g	j	g	j	g
5	C	C	C	C	C	C	E	E	E	E	E	E
4	B	B	B	B	B	B	D	D	D	D	D	D
3	A	A	A	A	A	A	A	A	A	A	A	A
2	c	f	c	f	c	f	i	m	i	m	i	m
1	b	e	b	e	b	e	h	k	h	k	h	k
0	a	d	a	d	a	d	g	j	g	j	g	j

SYNC BLOCK NO. ↑

FIG.22

CONSUMER CAMERA 1

	MSB							LSB
PC 0	0	1	1	1	0	0	0	0
PC 1	1	1	IRIS					
PC 2	AE MODE				AGC			
PC 3	WB MODE			WHITE BALANCE				
PC 4	FCM	FOCUS						

FIG.23

CONSUMER CAMERA 2

	MSB							LSB
PC 0	0	1	1	1	0	0	0	1
PC 1	1	1	VPD	V PANNING SPEED				
PC 2	IS	HPD	H PANNING SPEED					
PC 3	FOCAL LENGTH							
PC 4	ZEN	UNITS OF E-ZOOM			1/10 OF E-ZOOM			

FIG.24

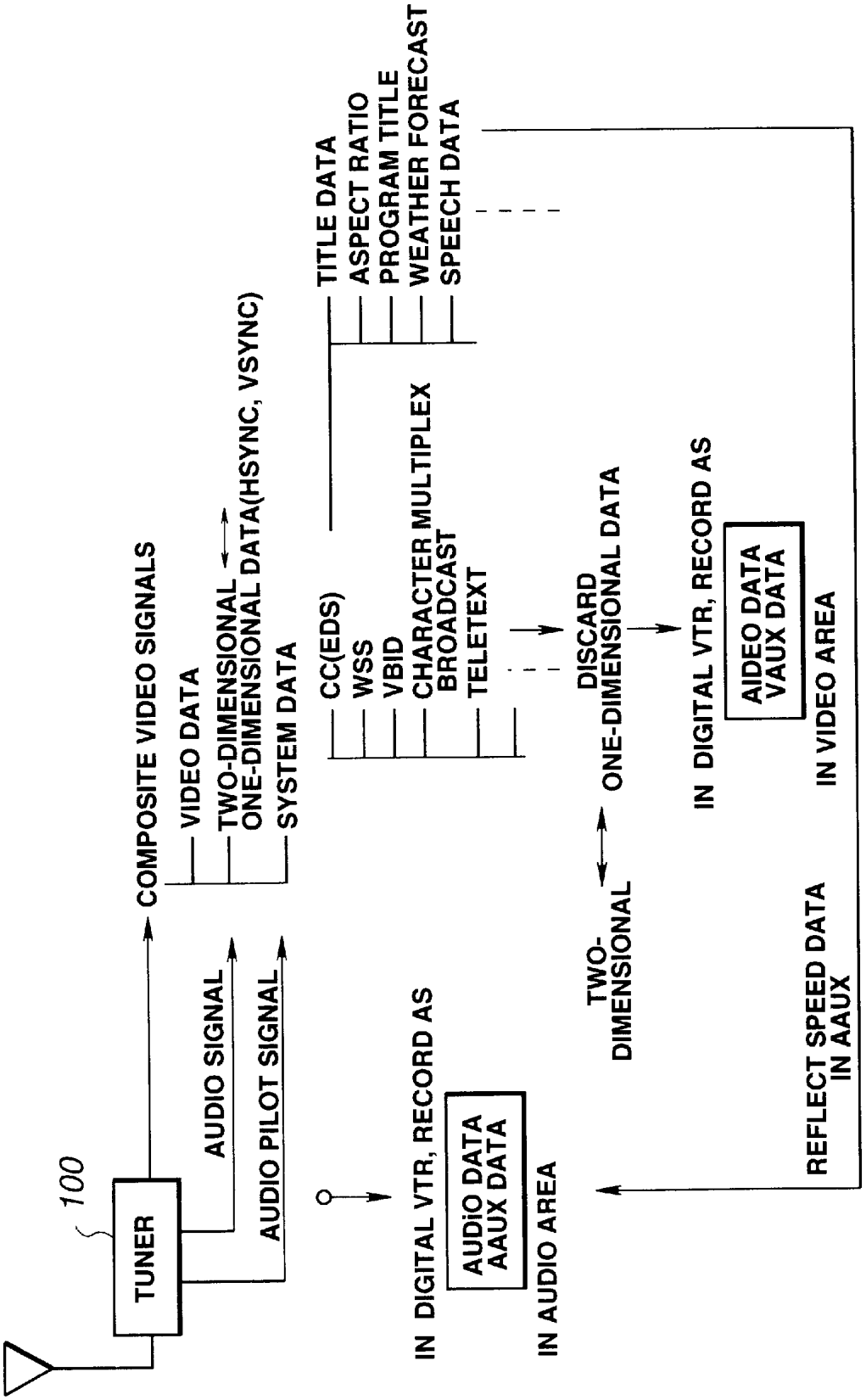

100
TUNER
COMPOSITE VIDEO SIGNALS
VIDEO DATA
TWO-DIMENSIONAL
ONE-DIMENSIONAL DATA(HSYNC, VSYNC)
SYSTEM DATA
AUDIO SIGNAL
AUDIO PILOT SIGNAL
TITLE DATA
ASPECT RATIO
PROGRAM TITLE
WEATHER FORECAST
SPEECH DATA
CC(EDS)
WSS
VBID
CHARACTER MULTIPLEX BROADCAST
TELETEXT
DISCARD
ONE-DIMENSIONAL DATA
TWO-DIMENSIONAL
IN DIGITAL VTR, RECORD AS
AUDIO DATA
AAUX DATA
IN AUDIO AREA
IN DIGITAL VTR, RECORD AS
AIDEO DATA
VAUX DATA
IN VIDEO AREA
REFLECT SPEED DATA IN AAUX

FIG.25

	ASPECT RATIO	COPY GUARD	TITLE	SEPARATE PROGRAM	OTHERS	CLOCKS	NUMBER OF bits / FRAME
CC	○		○	○		503kHz	32bits
EDS	○			○	○	503kHz	
VBID	○	○			○	Fsc/4	20bits
WSS	○				○	833kHz	14bits
CHARACTER MULTIPLEXED SIGNAL			○	○		5.7272MHz	4480bits
TELETEXT			○	○		6.9375MHz	11008bits
MACROVISION SIGNAL		○				OPTIONAL	ANALOG
INTER-STATION CONTROL SIGNAL					○	OPTIONAL	ANALOG
BUSINESS-USE SIGNAL					○	NOT CLEAR	NOT CLEAR

FIG.26

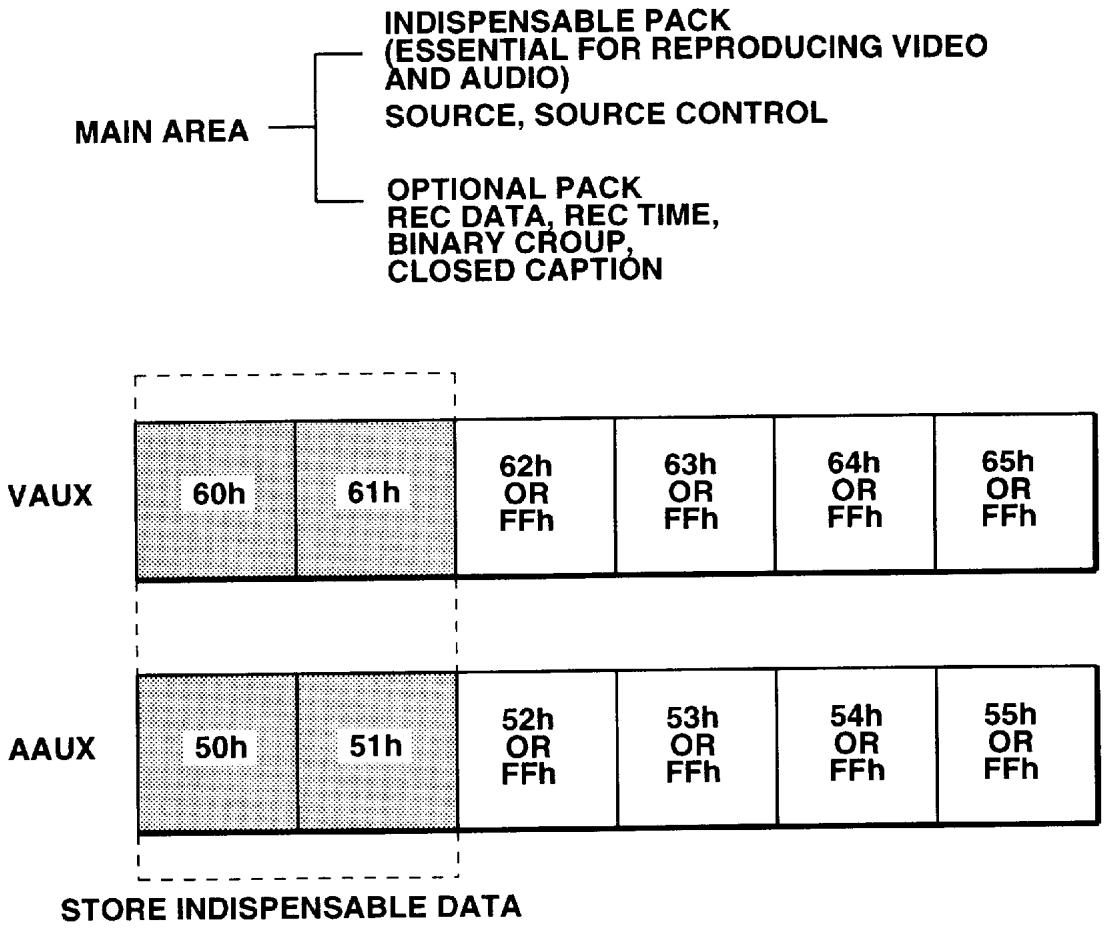

MAIN AREA
INDISPENSABLE PACK
(ESSENTIAL FOR REPRODUCING VIDEO AND AUDIO)
SOURCE, SOURCE CONTROL
OPTIONAL PACK
REC DATA, REC TIME, BINARY CROUP, CLOSED CAPTION
VAUX
60h
61h
62h OR FFh
63h OR FFh
64h OR FFh
65h OR FFh
AAUX
50h
51h
52h OR FFh
53h OR FFh
54h OR FFh
55h OR FFh
STORE INDISPENSABLE DATA

FIG.27

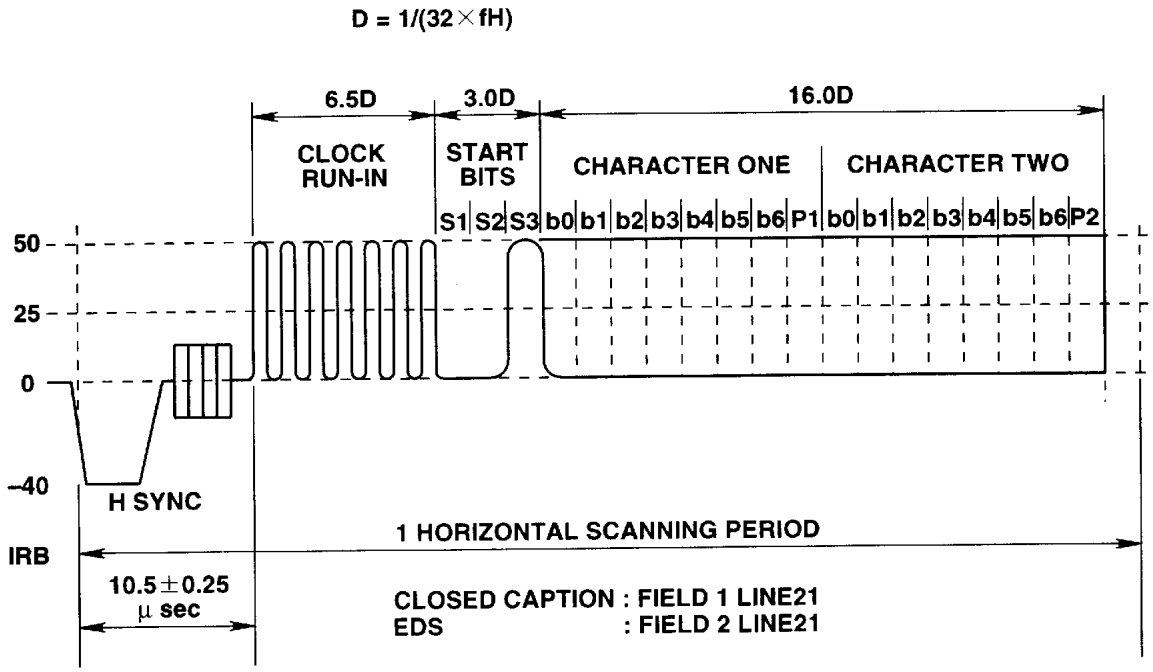

D = 1/(32×fH)
6.5D
3.0D
16.0D
CLOCK RUN-IN
START BITS
CHARACTER ONE
CHARACTER TWO
S1 S2 S3 b0 b1 b2 b3 b4 b5 b6 P1 b0 b1 b2 b3 b4 b5 b6 P2
50
25
0
-40
IRB
H SYNC
1 HORIZONTAL SCANNING PERIOD
10.5±0.25 μ sec
CLOSED CAPTION : FIELD 1 LINE21
EDS : FIELD 2 LINE21

FIG.28

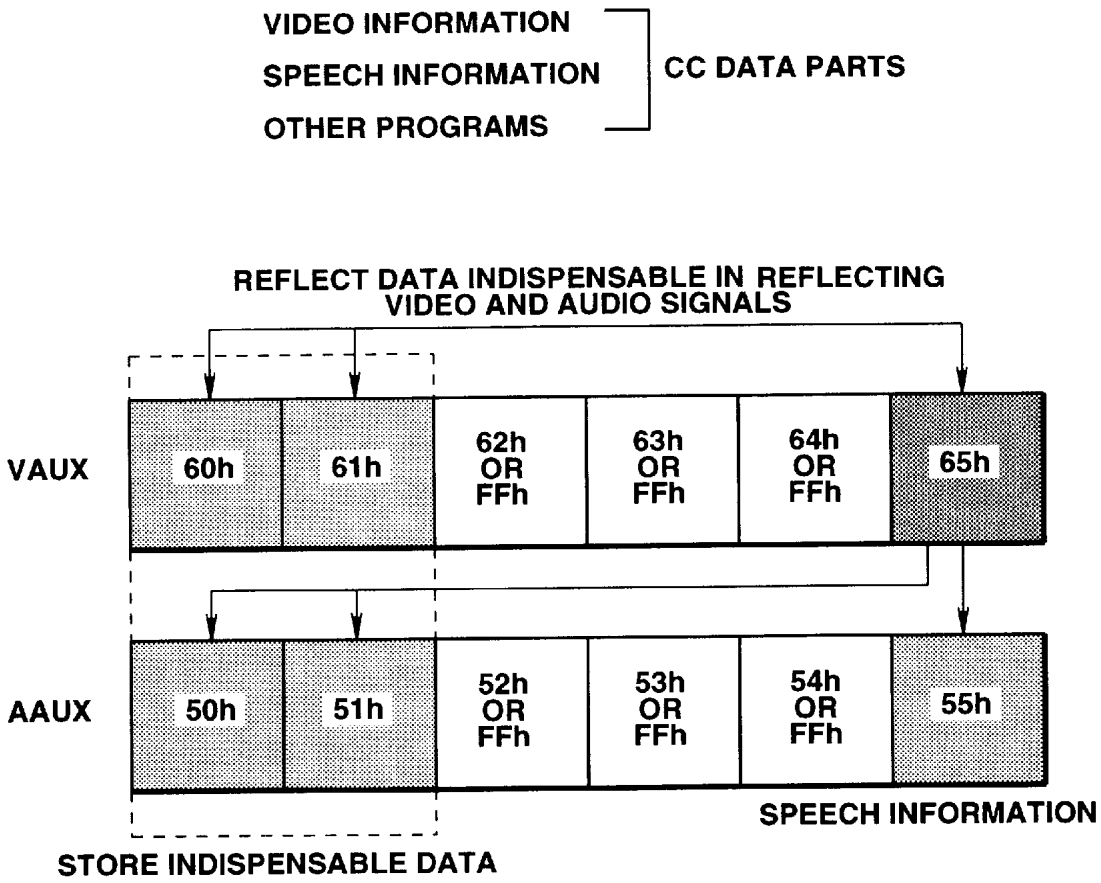

VIDEO INFORMATION
SPEECH INFORMATION
OTHER PROGRAMS
CC DATA PARTS
REFLECT DATA INDISPENSABLE IN REFLECTING VIDEO AND AUDIO SIGNALS
VAUX
60h
61h
62h OR FFh
63h OR FFh
64h OR FFh
65h
AAUX
50h
51h
52h OR FFh
53h OR FFh
54h OR FFh
55h
SPEECH INFORMATION
STORE INDISPENSABLE DATA

FIG.29

AUDIO TYPE OF CC PACK		AUDIO MODE OF SOURCE PACK	
MAIN	2ND	CH 1	CH 2
001	000	0010	1110
	001	0010	0010
	010	0010	1110
	011	0010	1110
	100	0010	1110
	101	0010	1110
	110	0010	1110
	111	0010	1111

0010 : MONO
1110 : BEYOND DISCRIMINATION
1111 : NO INFORMATION
CH 1 : FORMER 5 TRACKS
CH 2 : LATTER 5 TRACKS

FIG.30

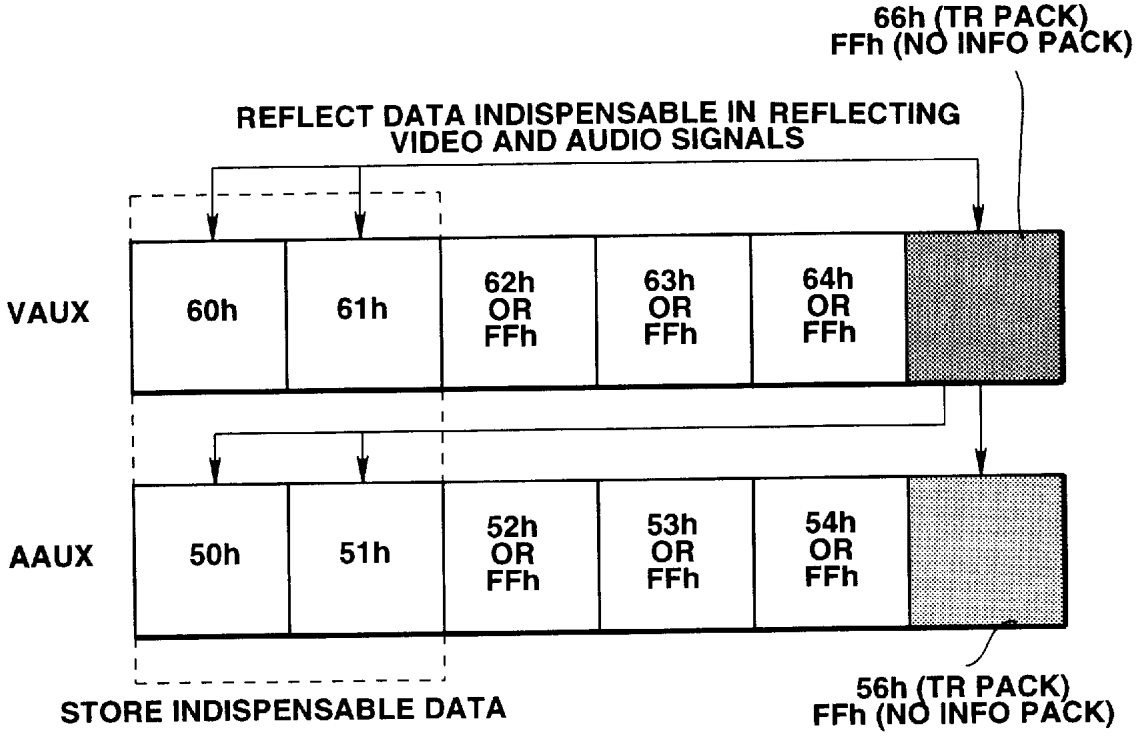

66h (TR PACK)
FFh (NO INFO PACK)
REFLECT DATA INDISPENSABLE IN REFLECTING VIDEO AND AUDIO SIGNALS
VAUX
60h
61h
62h OR FFh
63h OR FFh
64h OR FFh
AAUX
50h
51h
52h OR FFh
53h OR FFh
54h OR FFh
STORE INDISPENSABLE DATA
56h (TR PACK)
FFh (NO INFO PACK)

FIG.31

VTR NOT ADAPTABLE TO TR PACK	WRITE CC PACK IF THERE IS ANY
VTR ADAPTABLE TO TR PACK	WRITE CC PACK AND TR PACK (WRITE CC PACK AT ANY RATE IN TWO LAST TRACKS OF EACH VIDEO FRAME)

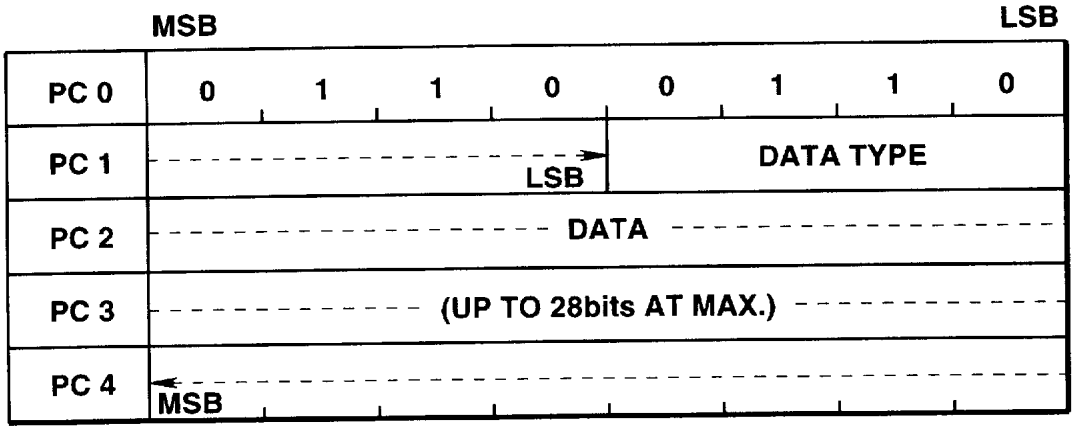
RECORD TIME

FIG.32A

VTR NOT ADAPTABLE TO TR PACK	IF THERE IS CC PACK, SEND IT IN SUPERPOSITION ON PRE-SET LINE
VTR ADAPTABLE TO TR PACK	IF THERE ARE CC AND TR PACKS, SECOND THEM IN SUPERPOSITION ON PRE-SET LINE
FOR BOTH TR PACK ADAPTABLE AND NON-ADAPTABLE VTRS, OTHER COMPOSITE VIDEO SIGNAL ANCILLARY INFORMATION FROM 60h, 61h, 50h AND 51h PACKS	

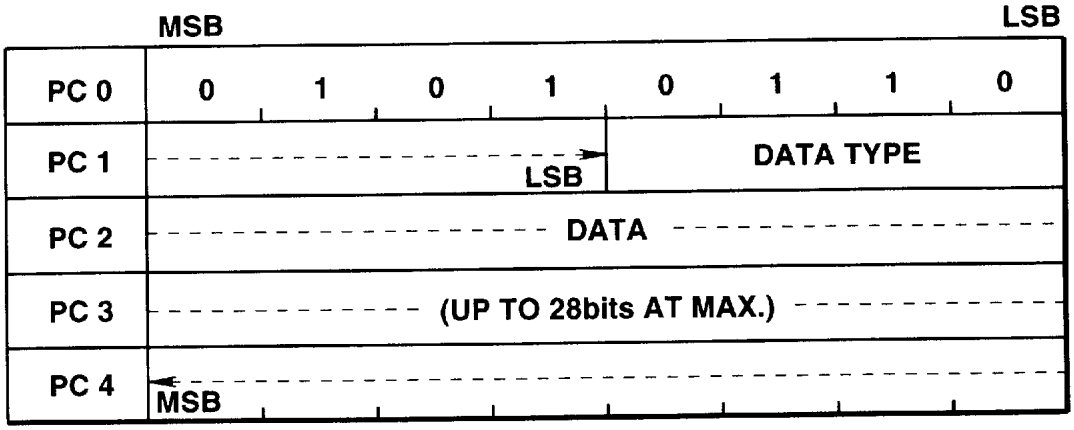
PLAYBACK TIME

FIG.32B



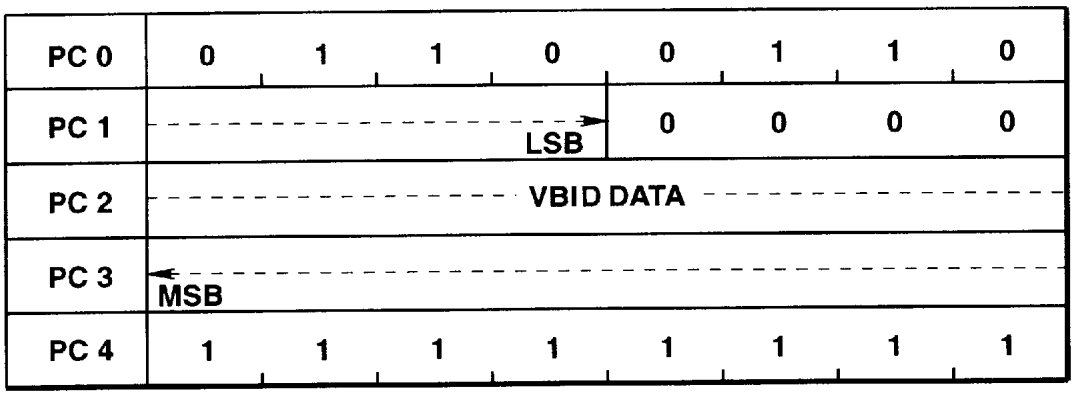
DATA TYPE :
0 0 0 0 = VBID
0 0 0 1 = WSS
0 0 1 0 = EDTV2
0 0 1 1 = X FIELD1
0 1 0 0 = X FIELD2
OTHERS = RESERVED

FIG.33



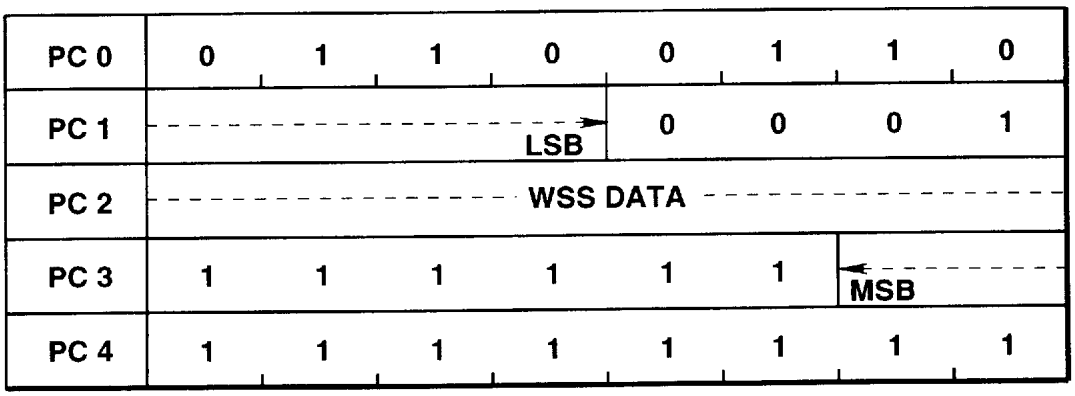
DATA TYPE :
0 0 0 0 = NOT ASSIGNED
0 0 0 1 = NOT ASSIGNED
0 0 1 0 = NOT ASSIGNED
0 0 1 1 = X FIELD1
0 1 0 0 = X FIELD2
OTHERS = RESERVED

FIG.35



WITH VBID DATA(20bits) RECORDED

FIG.34A



WITH WSS DATA(14bits) RECORDED

FIG.34B

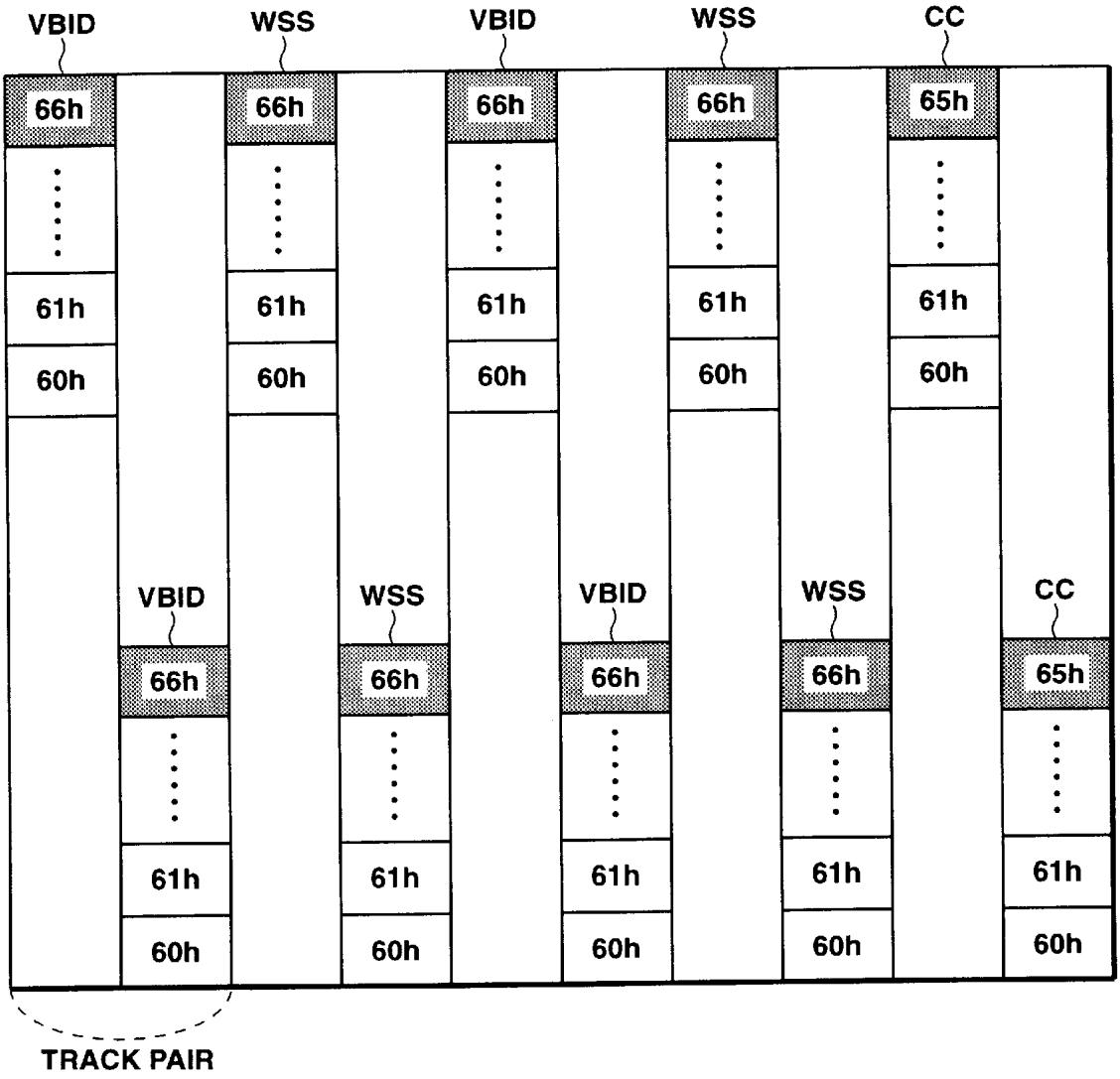

VBID
WSS
VBID
WSS
CC
66h
65h
61h
60h
VBID
WSS
VBID
WSS
CC
TRACK PAIR

FIG.36

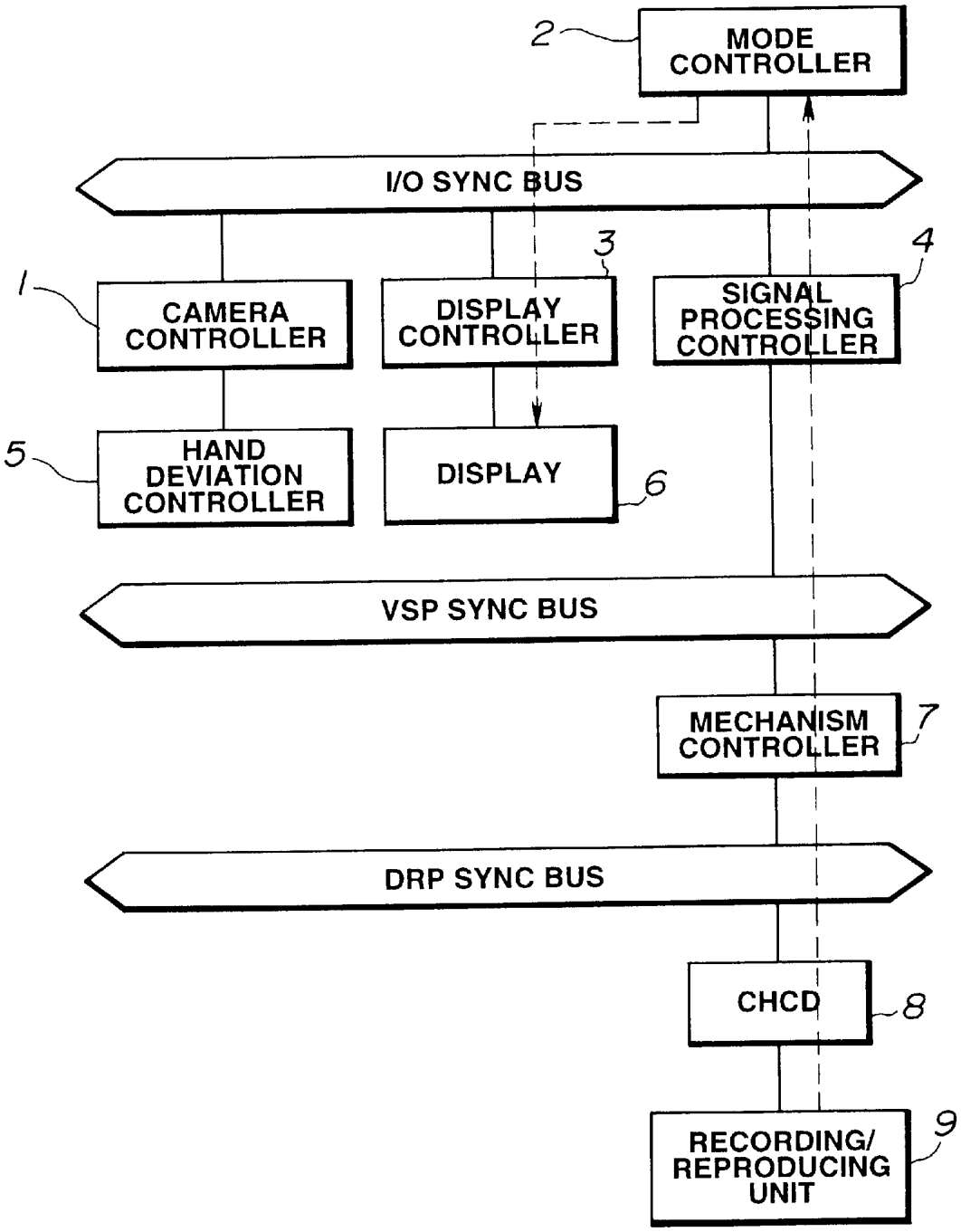

2
MODE CONTROLLER
I/O SYNC BUS
3
4
1
CAMERA CONTROLLER
DISPLAY CONTROLLER
SIGNAL PROCESSING CONTROLLER
5
HAND DEVIATION CONTROLLER
DISPLAY
6
VSP SYNC BUS
MECHANISM CONTROLLER
7
DRP SYNC BUS
CHCD
8
RECORDING/ REPRODUCING UNIT
9

FIG.37

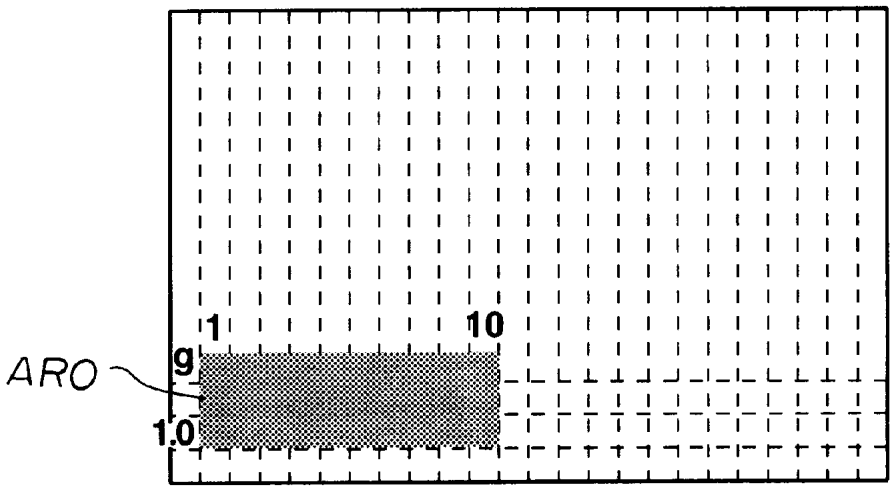

ARO
1
10
9
10

FIG.38

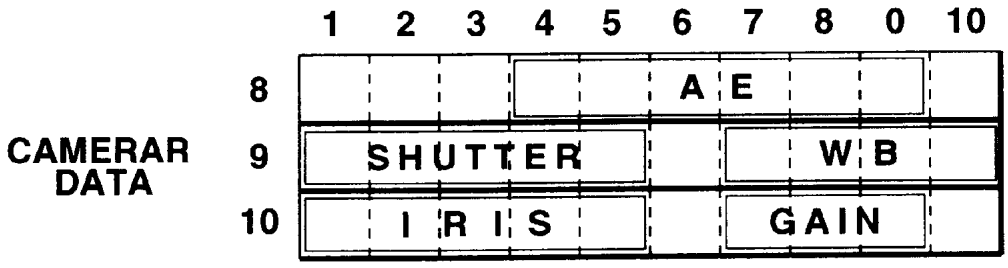

1 2 3 4 5 6 7 8 0 10
8
9
10
A E
SHUTTER
W B
I R I S
GAIN
CAMERAR DATA

FIG.39

FIG.40A

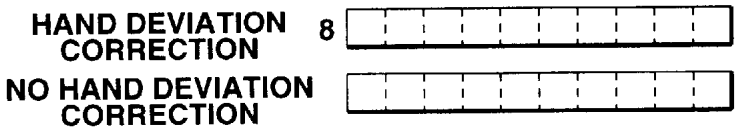


FIG.40B

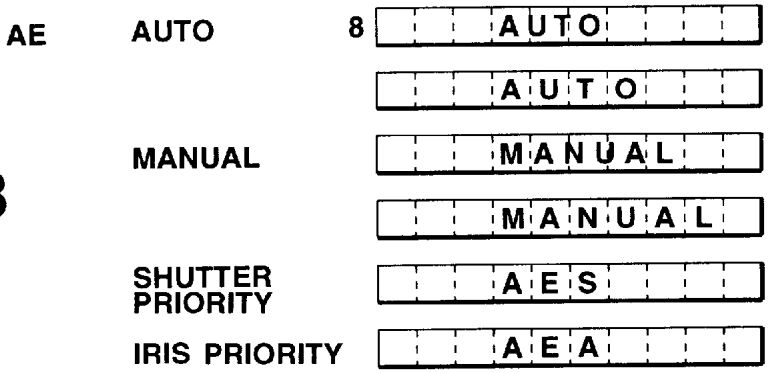


FIG.40C

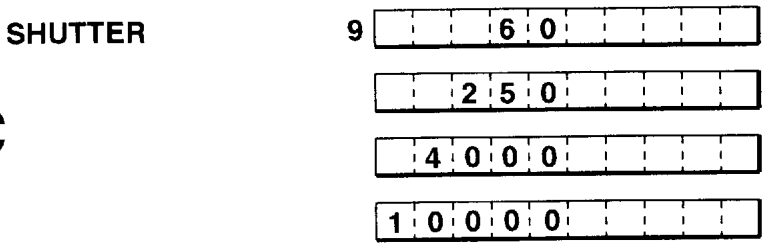


FIG.40D

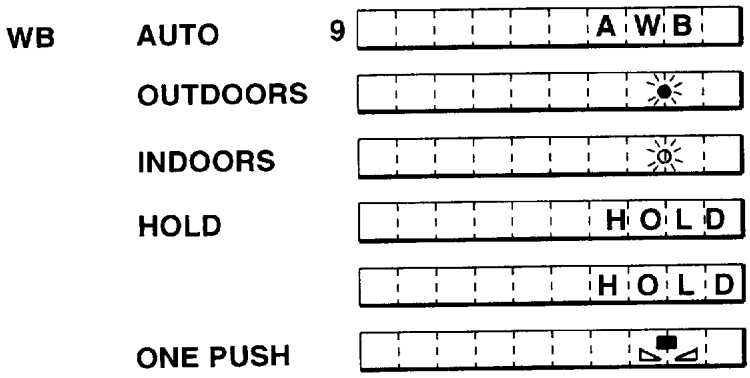
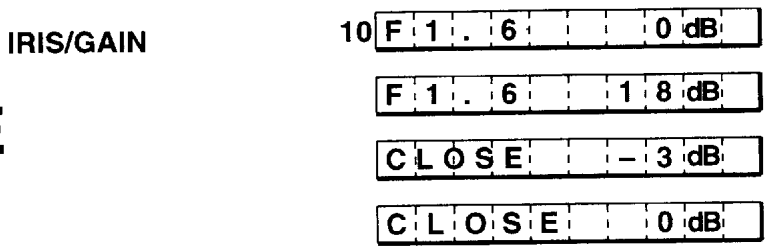


FIG.40E



APPARATUS AND METHOD FOR RECORDING AND REPRODUCING A VIDEO SIGNAL WITH CAMERA SETTING DATA

BACKGROUND OF THE INVENTION

The present invention relates to apparatus and method for recording and reproducing a video signal with camera setting data and, more particularly, to a camera having a video tape recorder integrated therein which is operable to record and reproduce a video signal along with camera setting data which identifies the various settings of the camera during imaging of a video image.

As is known, a combination camera/video tape recorder, known as a camcorder, images a video image to produce a video signal and records the video signal on a magnetic tape. Like ordinary still cameras, various settings of the camcorder are manually or automatically adjusted prior to and during the imaging of the video image so that the highest quality of picture can be obtained. The camera settings that are adjusted generally include the iris setting, the shutter speed, and the gain and white balance.

Cameras with video tape recorders integrated therein are known to insert certain information signals, for example, closed caption, VBID and EDTV2 type signals, in the vertical blanking intervals of a video signal prior to recording the video signal on a magnetic tape.

One difficulty encountered in typical recording/reproducing devices is their general inability to record, reproduce and subsequently process video signals by utilizing the various settings of the camera that generated those video signals.

OBJECTS OF THE INVENTION

Therefore, it is an object of the present invention to provide apparatus and method for recording and reproducing a video signal with camera setting data which overcome the shortcomings of the above described devices.

Another object of the present invention is to provide apparatus and method for recording and reproducing a video signal with camera setting data which enables the recorded video signals to be processed in accordance with the stored camera setting data so as to produce high quality video images.

A further object of the present invention is to provide a recording and reproducing technique which allows for the automatic or manual processing and/or correction of recorded video signals by utilizing the stored camera setting data.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, apparatus and method operate to establish various camera settings of an imaging device, e.g., a camera, in preparation of imaging a video image, image the video image so as to produce a video signal, generate camera setting data which identifies the various camera settings that were established for imaging the video image, and record the video signal in a first location of a track on a record medium, e.g., a magnetic tape, and the camera setting data in a second location of the track on the record medium.

As one aspect of the present invention, date and time data which represents a date and time at which the video image is imaged is generated, and the date and time data is recorded along with the video signal and camera setting data on the record medium.

As another aspect of the present invention, the video signal is recorded in a video data area of each track and the camera setting data is recorded as data packs having a common pack structure in a video auxiliary area of each track.

As yet a further aspect of the present invention, the camera setting data identifies the iris setting, shutter speed, white balance mode and focusing mode of the camera during imaging of the video image.

As yet another aspect of the present invention, the camera setting data identifies a vertical panning speed, a horizontal panning speed, manual control (hand deviation data), and distance data of the camera during panning imaging of the video image.

In accordance with another embodiment of the present invention, apparatus and method operate to reproduce from a record medium a video signal that represents a video image imaged by a camera and camera setting data that identifies various states of the camera during imaging of the video image, generate display data from the reproduced camera setting data, and output the reproduced video signal and the generated display data.

As one aspect of this embodiment, the display data is displayed to a user, and the video signal is modified in accordance with user instructions and the displayed display data.

BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description, given by way of example and not intended to limit the present invention solely thereto, will best be appreciated in conjunction with the accompanying drawings, wherein like reference numerals denote like references and parts, in which:

FIG. **1** is a block diagram of apparatus for recording a video signal with camera setting data in accordance with the present invention;

FIG. **2** is another block diagram of apparatus for recording a video signal with camera setting data which illustrates a signal flow of the camera setting data during a recording operation of the apparatus of the present invention;

FIG. **3** is a schematic illustration of a camera display in accordance with the present invention;

FIG. **4** illustrates the data structure of a track recorded on a record medium in accordance with the present invention;

FIGS. **5**A and **5**B schematically illustrate the data structure of a pre-sync block and a post-sync block, respectively;

FIGS. **6**A and **6**B schematically illustrate the data structure of the audio area of a track;

FIGS. **7**A and **7**B schematically illustrate the data structure of the video signal;

FIG. **8** shows the data structure of a video frame having error correction data added thereto;

FIGS. **9**A to **9**C schematically illustrate the data structure of the video area of a track;

FIG. **10** illustrates the data structure of the subcode area of a track;

FIGS. **11**A and **11**B show the data structure of the ID data in the audio and video auxiliary areas;

FIG. **12** illustrates the data structure of the ID data in the subcode area;

FIG. **13** shows the data structure of a pack of data;

FIG. **14** is a chart of the "large item" data as identified in a data pack;

FIGS. **15**A to **15**E illustrate the data structure of various audio auxiliary data packs;

FIG. **16**A illustrates an audio auxiliary closed caption data pack, and FIGS. **16**B to **16**E illustrate the data structure of various video auxiliary data packs;

FIGS. **17**A and **17**B illustrate the data structure of two more video auxiliary data packs;

FIG. **18** identifies the audio auxiliary packs stored in successive tracks on a record medium;

FIG. **19** illustrates the data structure of the video auxiliary area of a track;

FIG. **20** identifies the particular video auxiliary data packs stored in successive tracks;

FIG. **21** schematically illustrates the data structure of a subcode area recorded in accordance with a 525/50 video system;

FIG. **22** schematically illustrates the data structure of a subcode area recorded in accordance with a 625/50 video system;

FIG. **23** illustrates the data structure of a "consumer camera **1**" data pack;

FIG. **24** illustrates the data structure of a "consumer camera **2**" data pack;

FIG. **25** is useful for explaining the operation of a television tuner;

FIG. **26** is a chart which identifies the type of signals that are inserted into the various composite video signals;

FIG. **27** is useful for explaining the video and audio auxiliary areas;

FIG. **28** is a waveform diagram of a closed caption signal;

FIG. **29** is useful for explaining the insertion of a closed caption data pack in the video and audio auxiliary areas;

FIG. **30** is a chart which identifies the relationship between the data of the closed caption data pack and the audio mode data of the audio auxiliary source data pack;

FIG. **31** is useful for explaining the insertion of a transparent (TR) data pack in the VAUX and AAUX areas;

FIGS. **32**A and **32**B are useful for explaining the apparatus of the present invention operating in the recording and reproducing modes;

FIG. **33** illustrates the data structure of the video auxiliary TR data pack;

FIGS. **34**A and **34**B illustrate the data structure of VBID data and WSS data stored in the video auxiliary TR pack;

FIG. **35** illustrates the data structure of the audio auxiliary TR pack;

FIG. **36** schematically illustrates the data structure of tracks having CC, VBID and WSS data therein;

FIG. **37** is a block diagram of the apparatus of the present invention showing the flow of camera setting data during a reproducing operation;

FIG. **38** schematically illustrates an on-screen display during a reproducing operation of the apparatus of the present invention;

FIG. **39** schematically illustrates the display of the various camera control settings; and

FIGS. **40**A to **40**E schematically illustrate the various displays of the camera control data in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, and particularly to FIG. **1** thereof, apparatus for recording and reproducing a video signal with camera setting data (hereinafter, either "video tape recorder" or "camera") is shown as comprising a camera controller **1**, a mode controller **2**, a display controller **3**, a signal processing controller **4**, a hand deviation controller **5**, a display **6**, a mechanism controller **7**, a channel coder **8**, a recording/reproducing unit **9**, as well as an I/O sync bus, a VSP sync bus and a DRP sync bus. Although not shown, the apparatus of the present invention further includes an imaging unit (i.e., a camera) which images a video image to produce a video signal. The video tape recorder of FIG. **1**, also identified herein as the camera data control system, records camera setting data that is generated in controller **1** on a record medium in the manner to be discussed.

Camera controller **1**, in response to control signals from hand deviation controller **5**, sets the various camera settings, including the AE mode, the shutter speed, the white balance, the iris/gain setting, etc., and transmits via the I/O sync bus, the camera settings to mode controller **2**, such as shown in FIG. **2**. Hand deviation controller **5** receives user input instructions to manually set the desired camera settings. Mode controller **2** converts the camera setting information into camera setting data (to be discussed) and supplies the camera setting data via the I/O sync bus to signal processing controller **4** which supplies the data via the VSP sync bus to mechanism controller **7** and then to channel coder **8** before being recorded on the record medium (e.g., a magnetic tape). During a recording operation of the video tape recorder of the present invention, display controller **3** controls display **6** to display those camera settings that are manually adjusted but to not display those settings which have been automatically adjusted. FIG. **3** is a schematic illustration of display **6** and which shows the manually adjusted settings in either display area AR**1** or display area AR**2**. For example, if the camera is operating in a mode in which the iris is manually set, the particular mode of operation in which the iris is manually adjusted is indicated in the viewfinder (i.e., display **6**) as well as the actual manually set value of the iris. As another example, if the amount of white balance is manually adjusted, the manually adjusted value also is displayed in, for example, display area AR**2** of display **6**. Further, if the shutter speed is manually adjusted, the shutter speed value is displayed in area AR**1** as well as on a separate LCD panel of the camera.

Referring next to FIG. **4**, the data structure of a track recorded on a magnetic tape in accordance with the present invention is shown. The track format is comprised of a margin, followed by an ITI area, an audio area, a video area, a subcode area, and another margin area. Inter-block gaps (IBG) are provided between the ITI, audio, video and subcode areas. The ITI area is comprised of a 1400 bit preamble, followed by an 1830 bit start-sync block (SSA) area, a 90 bit track information (TIA) area and a 280 bit postamble area. The preamble of the ITI area allows for PLL run-in during a playback operation, the postamble establishes the end of the ITI area, and the SSA and TIA areas each is comprised of 30 bit blocks of data in which a 10 bit preset sync pattern (ITI-sync) is recorded at the beginning of each block thereof. The 20 bits following the 10 bit preset sync pattern of each block in the SSA area identify the number of the respective sync block, and the 20 bits following the preset sync pattern in the TIA area includes various recording format information, including a 3 bit APT data, an SP/LP flag which indicates the type of recording mode, and a PF flag which indicates the reference frame of the server system during the recording operation. The APT data defines the data structure of the track and is generally

"000" in consumer type digital video tape recorders. A relatively large number of sync blocks, each having a relatively small amount of code therein, are recorded at predetermined fixed intervals on each track of the magnetic tape and, thus, post-recording of data in the sync blocks is easily carried out.

The audio area of a track, as shown in FIG. **4**, is comprised of a 400 bit run-up area for PLL engagement purposes, a 100 pre-sync area which allows for the detection of an audio sync block, and a post-amble area that includes therein a 50 bit post sync which identifies the end of the audio area followed by a 500 bit guard area for protecting the audio data during a post-recording operation. The pre-sync block and post-sync block, as shown in FIGS. **5**A and **5**B, respectively, each is comprised of 2 bytes of sync data, followed by 3 bytes of identification data (ID**0**, ID**1** and IDP). The 6th byte of the pre-sync block includes an SP/LP flag, which is redundant to the flag stored in the ITI area, and is utilized in the event the ITI area cannot be reproduced. The 6th byte of the post-sync block is not used.

The audio data stored in the audio area of each track is located between the pre-sync and post-sync blocks shown in FIG. **4** and has a data structure as shown in FIG. **6**A. The "data" portion of the audio area is comprised of an audio auxiliary (AAUX) area in which 5 byte packs of AAUX data are stored, and an audio data area in which sound information are stored. The audio area is comprised of 14 blocks in which the first 9 blocks include AAUX data, audio data, and horizontal parity C**1**, and the succeeding 5 blocks each is comprised of vertical parity data C**2** and horizontal parity data C**1**. The 14 blocks each also include at the beginning thereof 2 bytes of sync data followed by 3 bytes of identification data. FIG. **6**B illustrates the data structure of each of the first 9 blocks shown in FIG. **6**A.

Referring again to FIG. **4**, the video area of a track has a data structure that is similar to the audio area and, as shown, is comprised of a run-up area, a pre-sync area, a video data area, a post-sync area, and a guard area. A composite video signal is separated into its respective Y, R-Y and B-Y components, and converted to digital data. In a 525/60 video system, 720 samples in the horizontal direction and 480 lines in the vertical direction of the Y signal are extracted for each frame, and 180 samples in the horizontal direction and 480 lines in the vertical direction of the R-Y and B-Y signals are extracted for each frame. The extracted data is divided into blocks of data, such as shown in FIGS. **7**A and **7**B. FIG. **7**A illustrates the Y(DY) signals in the block structure and FIG. **7**B illustrates the R-Y(DR) and B-Y(DB) signals in the block structure, in which pairs of vertically adjacent blocks are grouped together to form each block since the "right hand" side blocks have only 4 horizontal samples each. The block structure shown in FIGS. **7**A and **7**B is comprised of 8100 blocks per frame and a block that is comprised of 8 horizontal samples and 8 vertical lines is identified herein as a DCT block.

The blocks are shuffled and transformed in a manner well known in the art, and the transformed blocks are quantized and variable length encoded in which the quantization step is established in terms of 30 DCT blocks as a single unit so that the total amount of resultant encoded data does not exceed a predetermined value. The encoded data corresponding to 30 DCT blocks is identified herein as a buffering unit. FIG. **8** illustrates the data structure of the video area of a track in which buffering units 0 to 26 each is comprised of 5 video blocks, as shown in FIG. **9**A. Each block in the buffering unit is comprised of 1 byte of Q data, which corresponds to a quantization parameter, followed by 76 bytes of video data. Referring back to FIG. **8**, the video area is comprised of a first block α having VAUX data stored therein, a second block β having VAUX data stored therein, 27 buffering units, a third block γ having VAUX data stored therein, and 11 blocks of data having vertical parity data C**2** stored therein. Each VAUX block, buffering unit, and block of C**2** data, is preceded by 2 bytes of sync data and 3 bytes of identification data, and is followed by 8 bytes of horizontal parity data C**1**. Thus, each "video data" block in the video area of a track is comprised of 90 bytes of data, as shown in FIG. **9**B, and each VAUX block (α, β and γ) in the video area of a track also is comprised of 90 bytes of data, as shown in FIG. **9**C.

It is seen in the above discussed framing format, that since 27 buffering units are stored in each track on the magnetic tape, and since each track includes therein 810 DCT blocks of video data and each frame corresponds approximately to 8100 DCT blocks of video data, one video frame is recorded in 10 tracks on the magnetic tape.

Referring next to FIG. **10** of the drawings, the data structure of the subcode area of a track is shown. The subcode area generally is provided for high speed searching of the video and/or audio data, and is comprised of a subcode preamble, followed by 12 sync blocks and a postamble. Unlike the video and audio areas of a track, the subcode area does not include a presync and postsync area. Each subcode sync block, as shown in expanded form in FIG. **10**, is comprised of two sync bytes, three identification bytes, a 5 byte auxiliary data area, and two bytes of horizontal parity C**1**.

Referring back to FIGS. **9**B and **9**C, the sync blocks of the audio, video and subcode areas are 24/25 modulated so that the amount of data of each of the video, audio and subcode areas have the amount of data shown in FIGS. **9**B and **9**C. As is known, 24/25 modulation converts 24-bit based data to 25 bits so that the pilot frequency components for tracking control are in accordance with the recorded codes.

The ID data following the 2 sync bytes shown in FIGS. **5**A, **5**B, **6**B, **9**B, **9**C and **10** have a data structure as shown in FIGS. **11**A and **11**B. As shown in both FIGS. **11**A and **11**B, byte ID**1** in all of the above discussed areas, identifies the sync block number of the block in which the identification data is located. The 4 least significant bits of identification byte ID**0** identify the track (i.e., track number) within each frame. Referring to FIG. **11**A, which illustrates the data structure of the identification data in AAUX, audio and video sync blocks, the four most significant bits of identification byte ID**0** identify a sequence number which is utilized for variable speed reproduction. The three most significant bits of identification byte ID**0**, shown in FIG. **11**B, identify the data structure of the area in which the presync, postsync and C**2** parity sync blocks are located. That is, identification data located in the audio area of a track identifies the data structure of the audio area (data AP**1**), and identification data in the video area of a track identifies the data structure of the video area (data AP**2**). Data AP**1** and AP**2** generally have the value "1000" for consumer type digital video tape recorders.

FIG. **12** illustrates the data structure of the identification data ID**0** and ID**1** in all of the sync blocks in the subcode area of a track. The most significant bit (FR) of byte ID**1** of each of the sync blocks identifies the particular field, i.e., odd or even field, to which the current track corresponds. In other words, flag FR indicates whether the track is one of the first 5 tracks of a frame or is one of the second 5 tracks of the frame. The next three most significant bits (AP**3**) of bit

ID1 in sync block 0 and sync block 6 identify the data structure of the subcode area, and the second through fourth most significant bits in ID1 of sync block 11 (APT) identify the data structure of the track. The three bits of byte ID1 identified at "tag" in sync blocks 1–5 and 7–10 are shown in expanded form in FIG. 12 and include an index ID which is used for indexing purposes, a skip ID which is used to skip various frames, for example, commercials, and a PP ID which is used to identify a frame as a still image. The 4 least significant bits of byte ID1 and the 4 most significant bits of byte ID0 are used to store the absolute track number and this number is stored four times in the subcode area of each track, as shown. The 4 least significant bits of byte ID0 of each sync block identifies the number of that sync block.

As previously discussed, the audio auxiliary (AAUX) data is stored in the audio area of a track, the video auxiliary (VAUX) data is stored in the video area of a track, and subcode auxiliary (AUX) data is stored in the subcode area of each track. These auxiliary data are stored in units of 5 bytes, called a 5 byte "pack" or simply a data pack, and have a data structure as shown in FIG. 13. The first byte PC0 of each data pack identifies the type of data stored in the pack and is called the "item" or "header" of the pack. Bytes PC1 to PC4 of each pack are the pack data as defined by the item (byte PC0). The item (PC0) is divided into the upper four bits, referred to as the "large item", and the lower four bits, referred to as the "small item". The large item identifies the "Group" to which the pack data pertains and the small item identifies specifically what information is contained within the pack data (PC1–PC4) within the specified Group.

FIG. 14 is a table showing the available Groups and, as shown, the large item can specify the Groups of control (0000) title (0001), chapter (0010), part (0011), program (0100), audio auxiliary data (AAUX) (0101), video auxiliary data (VAUX) (0110), camera (0111), line (1000) and soft mode (1111). Large items (1001) to (1110) are reserved for future use and large item (1111) identifies a pack having no information.

FIGS. 15A–15E and 16A illustrate the data structure of various audio auxiliary (AAUX) packs that are stored in the AAUX audio area. The pack "AAUX source" is shown in FIG. 15A and has an item value of 01010000 (PC0) and bytes PC1 to PC4 contain the information of locked mode flag (LF), audio frame size (AF size), audio channel mode (CH), field system (50/60), signal type (STYPE), emphasis flag (EF), time constant of emphasis (TC), sampling frequency (SMP) and quantization data (QU). Flag LF identifies whether or not the audio sampling frequency is locked to the picture signals, data AF size identifies the number of audio samples per frame, data CH identifies the number of audio channels, and PA and audio mode identify the type of audio mode, such as stereo or mono-audio.

FIG. 15B illustrates the data structure of the pack "AAUX source control", which has the item value (PC0) of "01010001". Bytes PC1 to PC4 of this pack identify the type of copy protection of the audio signal, whether the video tape is an original version, whether the original signal was an analog source signal, copy generation data, cipher type data (CP), a recording start frame flag (REC ST), a recording end frame flag (REC END), recording mode data (REC MODE) which indicates the type of recording (e.g. original recording, post recording, insert recording, etc.), a direction flag (DRF), a play back speed (SPEED), and a genre category.

FIG. 15C illustrates the data structure of the pack "AAUX REC DATE", and which has the item value of "01010010". Bytes PC1 to PC4 of this pack include a daylight savings time flag (DS), a thirty minute flag (TM) which indicates a time difference of at least thirty minutes, data which indicates the time difference, and data which indicates the day, week, month and year on which the particular video signal was recorded.

FIG. 15D illustrates the data structure of the pack "AAUX REC TIME", and which has the item value of "01010011". Bytes PC1 to PC4 of this pack identify the particular time at which the data was recorded. In the preferred embodiment, the time recorded is based on the SMPTE format.

FIG. 15E illustrates the data structure of the pack "AAUX REC TIME BINARY GROUP" and which has the item value of "01010100". Bytes PC1 and PC4 of this pack contain 8 binary groups of SMPTE time code.

FIG. 16A illustrates the data structure of the pack "AAUX CLOSED CAPTION" and which has the item value of "01010101". Bytes PC1 and PC2 identify the language of the primary "or main" language and its type, as well as a secondary (or second) audio language of the data included in the closed caption signals that are transmitted during the vertical blanking interval of a television signal. The three bits of the main and second audio languages are defined as follows:

000=unknown;
001=English;
010=Spanish;
011=French;
100=German;
101=Italian;
110=Other;
111=none.

The type of the main audio language (main audio type) is defined as follows:

000=unknown;
001=mono;
010=simulated stereo;
011=true stereo;
100=stereo;
101=data service;
110=other;
111=none.

The second audio types are defined as follows:

000=unknown;
001=mono;
010=descriptive video service;
011=non-program audio;
100=special effects;
101=data service;
110=other;
111=none.

When a closed caption pack is stored in the AAUX main area (to be discussed), additional data relating to main audio and second audio follow the above-discussed data. However, a "no information" pack is recorded in place of a closed caption pack, and data corresponding to the main speech and second speech follow the information "audio mode" in the AAUX source pack.

FIGS. 16B–16E, 17A and 17B illustrate the data structure of various VAUX packs that are stored in the video auxiliary area of the video area of a track. Referring first to FIG. 16B, the data structure of the pack "VAUX SOURCE" is shown.

The item value of this pack is "0110000" (PC0) and bytes PC1 to PC4 include data pertaining to the number of television channels (tens of TV channel and units of TV channel), a black and white (B/W) flag which identifies if the video signal is a monochromatic signal, a color frames enable (EN) flag with a color frames identification code (CLF), source code data which specifies the source of a video signal (e.g. camera, line, cable, tuner, soft tape, etc.), the type of video system (50/60 and STYPE), and tuner category data which identifies the type of tuning system (e.g. broadcast/satellite broadcast, etc.).

FIG. **16**C illustrates the data structure of the pack "VAUX SOURCE CONTROL" and which has an item value of "01100001". Bytes PC1 to PC4 of this pack include SCMS data, as well as other data which specify the type of copy protection (if any) of the video signal, whether the tape is original or a copy, the source of the video signal (e.g., analog or digital), copy generation data, cipher type data (CP), a recording start frame flag (REC ST), a recording end frame flag (REC END), the type of recording mode of the stored data (e.g. original recording, post recording, insert recording, etc.), the aspect ratio (BC SYS and DISP), a field flag (FF) indicating whether a field is to be outputted twice, a flag (FS) which specifies whether a first field or a second field is to be supplied during the period of the first field, a flag (FC) which specifies whether or not the data of the current frame is different from the data of a previous frame, a flag (IL) which specifies the type of scanning (e.g. interlaced or non-interlaced), a flag (ST) which specifies if the stored image is a still picture, and data which specifies whether the picture is recorded by a still camera, and the category of the genre.

FIG. **16**D illustrates the data structure of the pack "VAUX REC DATE" and which has the item value of "01100010". Bytes PC1 to PC4 of this pack identify the date on which the video signal is recorded. FIG. **16**E illustrates the data structure of the pack "VAUX REC TIME", has the item value of "01100011" and bytes PC1 to PC4 thereof identify the SMPTE time of the frame in which the pack data is included. FIG. **17**A illustrates the data structure of the pack "VAUX REC TIME BINARY GROUP", which has the item value of "01100100", and bytes PC1 to PC4 thereof include 8 binary groups of time code.

FIG. **17**B illustrates the data structure of the pack "VAUX CLOSED CAPTION". This pack has an item value of "01100101" and bytes PC1 to PC4 identify the closed caption signals that are transmitted during the vertical blanking period of the analog video signal.

As described above, the audio, video and subcode areas of the track store auxiliary data in the 5 byte pack structure. In the preferred embodiment of the present invention, the respective AAUX, VAUX and subcode AUX data each comprises a "main area" and an "optional area" and are described below.

Referring next to FIG. **18**, the AAUX pack structure of the audio area of 10 successive tracks are shown in which each track includes nine audio auxiliary packs (numbered **0–8**) and in which the audio area of each track has the data structure as shown in FIG. **6**A, previously discussed. Referring FIG. **18**, nine packs are recorded in each of ten tracks of a frame where pack number **0** corresponds to the pack in the first audio sync block and pack number **8** corresponds to the pack in the ninth audio sync block. Packs numbers **3–8** in odd numbered tracks contain the numbers **50**, **51** . . . **55**, respectively, and pack numbers **0–5** in even numbered tracks also contain the numbers **50**, **51** . . . **55**, respectively. In this area, i.e., those packs which contain a number, comprises the AAUX main area, while the other area, i.e., those packs that do not contain a number, comprises the AAUX optional area. The packs in the main AAUX area, as identified in FIG. **18**, identify the value of the item (by PC0), in hexadecimal notation, of the AAUX packs. For example, the AAUX source pack is stored as pack number **3** in tracks **1**, **3**, **5**, **7**, **9** and as pack number **0** in tracks **2**, **4**, **6**, **8** and **10**.

As previously discussed with reference to FIG. **8**, sync block α, β and γ each includes a 77 byte VAUX data area. FIG. **19** illustrates the data structure of sync blocks α, β and γ in which each of these blocks includes 15 five byte packs, followed by two unused bytes. As shown, a sync block α includes pack numbers **0–14**, sync block β includes pack numbers **15–20**, and sync block γ includes pack numbers **30–44**, for a total of 45 packs that are stored in the video area of a track.

FIG. **20** illustrates the pack structure of the VAUX area of the video area of 10 tracks (1 frame) and, as shown, pack numbers **39–45** in odd numbered tracks and pack numbers **0–5** in even numbered tracks comprise the VAUX main area. The other packs, i.e., those that do not contain a number, comprise the VAUX optional area. The packs in the VAUX main area containing numbers **60–65** correspond to the packs "VAUX SOURCE", "VAUX SOURCE CONTROL", "VAUX REC DATE", "VAUX REC TIME", "VAUX REC TIMES BINARY GROUP", and "VAUX CLOSED CAPTION", respectively, shown in FIGS. **16**B–**16**E, **17**A and **17**B.

As previously discussed with reference to FIG. **10**, the subcode area of each track includes 12 sync blocks in which each sync block includes therein five bytes of auxiliary (AUX) data. A five byte pack is stored as the five bytes of auxiliary data in each sync block and, thus, the subcode area of each track includes 12 sync packs. Referring next to FIG. **21**, the block structure of the subcode area of 10 tracks in a 525/50 system in which each frame is comprised of 10 tracks is shown. In FIG. **21**, sync blocks **3–5** and **9–11** are shaded and represent the main area of the subcode area, and the remaining sync blocks **0–2** and **6–8** represent the optional area. The upper case letters in the main area of this subcode area represent subcode auxiliary packs, such as those previously discussed, and the lower case letters in the optional area of the subcode area represent optional subcode auxiliary packs which may be stored in the optional subcode area. FIG. **22** is similar to FIG. **21** but illustrates the pack structure of the subcode area of 12 tracks of a 525/60 system in which each frame is comprised of 12 tracks on a magnetic tape.

Referring back to FIG. **14**, a pack having a large item value of "0111" indicates that the pack pertains to the Group "CAMERA". Several packs in the Group CAMERA include "CONSUMER CAMERA **1**", "CONSUMER CAMERA **2**", "LENS", "GAIN", "PEDESTAL", "GAMMA", "DETAIL", "CAMERA PRESET", "FLARE", "SHADING", "KNEE", and "SHADOW". FIG. **23** illustrates the data structure of the pack "CONSUMER CAMERA **1**". Bytes PC1 to PC4 of this pack include data pertaining to the iris information (IRIS), AE mode information, automatic gain mode information (AGC), white balance mode information (WB MODE), white balance information (WHITE BALANCE), focussing mode information (FCM) and focal point position information (FOCUS).

The iris information (IRIS) in the data pack "CONSUMER CAMERA **1**", wherein the iris position=$2^{IP/8}$, is defined as follows:

0 to 3 Ch=IP;

3Dh=not more than F1.0;

3Eh=close; and

3Fh=no information.

The AE mode information (AE MODE) is defined as follows:

0=full automatic;

1=gain priority mode;

2=shutter priority mode;

3=iris priority mode;

4=manual;

Fh=no information; and

Other values=reserved.

The automatic gain control information (AGC) is defined as follows:

0 to Dh=G; and

Fh=no information,

where the value of G=−3+G×3 dB.

The white balance mode data (WB MODE) is defined as follows:

0=automatic;

1=hold;

2=one push;

3=pre-set;

7=no information; and

other values=reserved.

The white balance data (WHITE BALANCE) is defined as follows:

0=candle;

1=incandescent lamp;

2=low color temperature florescent lamp;

3=high color temperature florescent lamp;

4=sunlight;

5=cloudy weather;

Fh=no information; and

other values=reserved.

The focusing mode information (FCM) is defined as follows:

0=automatic focusing; and

1=manual focusing.

The focal point information (FOCUS) is defined as follows:

0 to 7Eh=focal point position; and

7Eh=no information,

where the focal point position=M×10^L cm and M represents the upper order five bits of FOCUS and L represents the lower order two bits of FOCUS.

FIG. **24** illustrates the data structure of the pack "CONSUMER CAMERA **2**". Bytes PC**1** to PC**4** include panning data pertaining to panning information in the vertical direction (VPD), panning speed in the vertical direction (V PANNING SPEED), hand deviation information (IS) and vertical distance information (FOCAL LENGTH).

Panning in the vertical direction (VPD) is defined as follows:

0=same direction as the vertical scanning direction; and

1=opposite direction to the vertical scanning direction.

The panning speed in the vertical direction is defined as follows:

0 to 1Dh=panning speed;

1Eh=not less than 29 lines per field; and

1Fh=no information.

Panning in the horizontal direction (HPD) is defined as follows:

0=same direction as the horizontal scanning direction; and

1=opposite direction to the horizontal scanning direction.

Panning speed in the horizontal direction (H PANNING SPEED) is defined as follows:

0 to 1Dh=PS;

3Eh=not less than 122 pixels per field; and

3Fh=no information,

wherein the panning speed=2×PS and one pixel period=2/(13.5×10^6) second.

Hand deviation correction is defined as follows:

0=on; and

1=off.

Focal length is defined as follows:

[0096]

0–FEh=focal length;

3Dh=not more than F1.0; and

FFh=no information,

where the focal length=M×10^L cm and M represents the upper **7** bits of FOCAL LENGTH and L represents the LSB of FOCAL LENGTH.

The main areas in each of the above discussed video, audio and subcode areas of a track have stored therein auxiliary data which generally is common to all types of magnetic tapes. On the other hand, different optional auxiliary data may be stored in the optional areas, discussed above, by both tape manufacturers and/or users of consumer video tape recorders. Optional auxiliary data that is stored in the optional areas of a track may include character data, teletext signal data, television signal data, or any other data that is included in the vertical blanking interval of a television signal, as well as computer graphics data.

FIG. **25** represents a television tuner in which a composite video signal having additional information in the vertical blanking intervals therein is received by a tuner **100**. Tuner **100** separates the video, audio and audio pilot signals from the supplied signal. The composite video signal is comprised of picture data, two dimensional/one dimensional converting data (e.g., horizontal sync, video sync and vertical blanking signals), as well as system data. The system data includes closed caption (CC), ED, WSS and VBID data. The system data includes data pertaining to the video picture, as well as speech information.

In the digital video tape recorder, two dimensional/one dimensional conversion data, which includes therein system data, is removed from the video signal prior to being recorded on a magnetic tape. If the input signal is directly recorded and directly output when reproduced, a type of recording known as "transparent recording" is accomplished. However, transparent recording generally is not accomplished in digital video tape recorders.

FIG. **26** illustrates the various system data that is included in various types of video signals. It is seen that some of the information (e.g., character multiplexed signal and teletext data) cannot simply be recorded, without further processing thereof, in a digital format. Further, macrovision signals correspond to "copy guard" and, thus, cannot simply be recorded as is.

Referring next to FIG. **27**, the particular types of data stored in the video auxiliary (VAUX) and audio auxiliary (AAUX) areas of a track are shown. As previously discussed, the VAUX area includes data packs having the item value (or header) of 60h to 65h, and the AAUX area of a track includes therein data packs having item values of 50h to 55h. The video and audio data packs "source" and "source control" having the header values of 60h, 61h, 50h and 51h, respectively, are known as "indispensable" data, whereas the

video and audio data packs having headers of 62h–65h and 52h–55h optionally are stored in each of the tracks on the magnetic tape and no information packs having the item value of FFh may be stored in place of these data packs. Furthermore, the above-mentioned CC, EDS, VBID and/or WSS data may be transparently recorded using the closed caption packs having the header values of 65h and 55h as well as the transparent packs having the header values of 56h and 66h.

FIG. **28** is a signal waveform diagram of a closed caption signal which is comprised of 6.5 cycles of a clock run-in signal followed by three start bits **S1**, **S2** and **S3**, a first character data and a second character data. In accordance with the present invention, the first and second character data in the closed caption signal is stored in a VAUX closed caption pack which has the data structure shown in FIG. **17**B, previously discussed. It is noted that closed caption signals generally are inserted in both the first and second fields of a video signal, but EDS signals may also sometimes be included in the second field of the video signal. That is, "raw" closed caption signals and raw EDS data may be stored in a single VAUX closed caption pack.

VAUX closed caption packs have the item value of 65h and are stored in the video auxiliary area of each track, as shown in FIG. **20**. If the closed caption data is not included in the video signal, no information packs instead are stored at these locations. Referring back to FIG. **17**B, the VAUX closed caption pack specifies that the data is to be inserted into the twenty-first line of a field and, thus, it is not necessary to specify this line in a "line" pack. When a digital video signal having closed caption data packs are reproduced from a record medium, the closed caption data automatically is inserted into the twenty-first line of a television signal by an appropriate decoder.

Referring next to FIG. **29**, the closed caption data stored in the closed caption data packs having headers of 65h and 55h are deemed to be indispensable when closed caption signals are included in the television signals. One technique to determine whether a closed caption signal is included in a television signal is by detecting line **21** as a 32fH clock run-in signal 10.5 microseconds after the decay of the horizontal synchronization signal. If it does, the ensuing 16-bit data is extracted therefrom and the 16 bits of data, which is comprised of two 7-bit ascii codes, along with two parity bits, are stored as the upper and lower bites of the respective field in the VAUX closed caption data pack. It is contemplated that U.S. originated video signals recorded in digital format on a record medium are reproduced in Japan which generally does not process the closed caption signals. The VBID data, which includes aspect ratio information, is included in the closed caption data in the television signal and, thus, "indispensable" data in the closed caption signal is extracted therefrom and included in the indispensable data packs having the headers of 60h, 61h, 50h and 51h. Thus, aspect ratio data is included in a pack having a header of 61h so that televisions that do not process the closed caption data properly switch to the proper aspect ratio as identified by the VBID data.

Closed caption signals may include both indispensable and dispensable data and such data is stored in the VAUX closed caption pack. The indispensable data is stored in data packs having headers of 60h, 61h, 50h and 51h and thus are fully reproducible by televisions that are operable to decode the VAUX closed caption packs. In addition, televisions that are unable to decode the VAUX closed caption packs still can restore the closed caption signals to the twenty-first line of the television signal if it at least recognizes the existence of the VAUX closed caption data pack. Further, televisions that are unable to decode and are unable to recognize the existence of VAUX closed caption packs are still able to restore the vertical blanking information by utilizing the data from the packs having the headers of 60h, 61h, 50h and 51h and, thus, various types of televisions and/or video tape recorders are operable to utilize the closed caption data. The data structure of the audio auxiliary closed caption data pack has been previously discussed with reference to FIG. **16**A. This data pack, which has a pack header of 55h, is stored at those locations in the audio auxiliary area of a track as shown in FIG. **18**. Similar to the VAUX closed caption pack, data that is indispensable for reproducing speech signals is stored in the data packs having the headers of 50h and 51h. Thus, a television or video tape recorder that is unable to process the AAUX closed caption pack is still operable to process the indispensable data that is included in the packs having the headers of 50h and 51h.

Data concerning the audio is stored in the VAUX closed caption pack. However, this information also is stored in the audio area of a track so that the audio data (i.e., speech data) can be reproduced even if the VAUX closed caption packs cannot be reproduced. Thus, post-recording of video data in the video area of a track, which would result in the loss of the VAUX closed caption packs, does not cause the audio stored in the audio area of a track to be un-reproducible.

EDS data includes information regarding the particular language of the closed caption data as well as the language (i.e., words) themselves, as previously discussed with respect to FIG. **16**A. FIG. **30** illustrates the relationship between the data stored in the AAUX closed caption pack and the audio mode data stored in the AAUX source pack. As shown, the various types of audio data as well as the locations of the information are reflected in the stored data.

The VBID, WSS and vertical blanking data are stored in the VAUX and AAUX transparent packs, and which have the data structure as shown in FIGS. **33** and **35**, respectively (to be discussed). The VAUX transparent pack, which has the pack header of 66h, and the AAUX transparent pack, which has the pack header of 56h, are stored in the positions as shown in FIG. **31**. These packs are stored at the same location as the closed caption packs, and depending on whether a video tape recorder is adapted to process a transparent pack, either only closed caption packs or both closed caption packs and transparent packs are stored in the digital data in the manner shown in FIG. **32**A. FIG. **32**B identifies the process of a video tape recorder that is adapted to process a transparent pack as well as a video tape recorder that is not adapted to process a transparent pack. Referring next to FIG. **33**, the data structure of a VAUX transparent pack is shown. This data pack includes four DATA TYPE bits which identify the type of data stored in the transparent pack. The data type may specify the data as VBID data, WSS data, EDTV**2** data, as well as to future types of data (e.g., X field **1**, X field **2**) in which different types of data are stored in the different fields of each frame. A maximum of twenty-eight bits are stored in the VAUX transparent pack and, as shown in FIG. **26**, such is possible with clock rates that are less than 1 MHz. FIG. **34**A illustrates a transparent pack having VBID data stored therein and FIG. **34**B illustrates a transparent pack having WSS data stored therein.

FIG. **35** illustrates the data structure of an AAUX transparent pack which, as shown, has a data structure similar to the data structure of the VAUX transparent pack. In addition, since VBID, WSS and EDTV**2** data do not include audio data, the data types of 0000, 0001 and 0010 are not assigned. In this case, "no information" packs may be utilized. Further,

it is preferable to keep the assignment of the data types of the VAUX transparent pack and the AAUX transparent pack the same so as to prevent processing of such information from becoming complex.

Referring back to FIGS. **18** and **20**, the structure of the audio and video auxiliary areas in each of ten tracks are shown. It is seen that each track includes the same pack contents, and if the closed caption pack is written in at least the last pair of tracks (e.g., tracks **9** and **10**), a transparent pack "picks" the closed caption pack even in the event that a magnetic tape which includes only the necessary closed caption packs in each of the ten tracks.

FIG. **36** illustrates the data structure of ten successive tracks which include therein VBID, WSS and closed caption data. Video tape recorders that are operable only to process the closed caption and VBID data, for example, then only the closed caption and VBID data is reproduced and processed which provides this data at predetermined positions in the vertical blanking interval of a video signal. WSS data, however, may be reproduced from the data packs having the pack headers of 60h and 61h and thus will be superimposed at predetermined positions in the vertical blanking period of the video signal. The data structure of the audio auxiliary area, regarding the audio auxiliary transparent pack and closed caption pack, is similar to the video auxiliary area and, thus, description thereof is omitted herein.

As previously discussed with reference to FIGS. **1** and **2**, the camera/video tape recorder of the present invention generates camera setting data which represent the various settings of the camera during imaging of a video image and stores the video signal along with the camera setting data on a magnetic tape. The camera setting data, in accordance with the present invention, are the data packs "consumer camera **1**", "consumer camera **2**", "lens", "gain", "pedestal", "gamma", "detail", "camera preset", "flare", "shading", "knee", and/or "shutter". The data structure of the consumer camera **1** and consumer camera **2** packs have been previously discussed and are shown in FIGS. **23** and **24**, respectively. In addition, date and time data regarding the date and time at which the video signal was produced (i.e., when the picture was taken) is stored in the REC date and REC time packs, or the binary group pack. These data packs are stored in the auxiliary data areas of a track, previously discussed. FIG. **37** is a block diagram of apparatus for recording and reproducing a video signal with camera setting data in accordance with the present invention in which the flow of reproduced camera setting data from the recording/reproducing unit **9** to the display **6** is shown. During a reproduction operation, recording/reproducing unit **9** reproduces the video signal and camera setting data from a magnetic tape and supplies the reproduced camera setting data via the various circuits to mode controller **2** which converts the supplied camera setting data into "display" data and which supplies the display data to display controller **3**. Mode controller **2** is responsive to user commands to determine whether the display data is to be output in either a first output configuration or a second output configuration. Display controller **3** supplies appropriate control signals to display **6** so that display **6** displays the various camera setting data and/or time and date data on a predetermined specified display area AR**0** shown in FIG. **38**, or on a separate LCD display on the camera body. FIG. **39** illustrates the structure of area AR**0** and, as shown, the particular AE mode is shown, and information regarding the shutter speed, the white balance gain, the iris setting and the gain information are shown. FIGS. **40**A to **40**E illustrate different displays of the camera of the present invention corresponding to whether there is any hand deviation (i.e., user control), the particular AE mode, the shutter speed, the iris setting, the white balance (WB) setting and the iris/gain settings, as shown in FIGS. **40**A, **40**B, **40**C, **40**D and **40**E, respectively.

By using the data shown in the apparatus' display, or in a reproducing apparatus which reproduces the video signal and camera setting data, the video signal can be processed accordingly, that is, the video signal can be processed and/or developed automatically or manually by a user in accordance with the various camera setting data that is displayed therewith.

While the present invention has been particularly described in conjunction with preferred embodiments thereof, it will be readily appreciated by those of ordinary skill in the art that various changes may be made without departing from the spirit and scope of the invention. For example, although the present invention has been shown and described as recording and reproducing camera setting data including hand deviation correction data, AE mode data, shutter speed, iris setting, WB data and gain data, the present invention is not limited solely to these types of camera settings and may record and reproduce other types of camera settings, even those that are not currently in use.

As another example, although the present discussion is directed to a particular type of recording format, the present invention is not limited to this format and may be widely applied to other recording formats as well as to other types of recording mediums, including, but not limited to, magnetic tapes, magneto-optical disks, optical disks, computer random access memories, etc.

Therefore, it is intended that the appended claims be interpreted as including the embodiments described herein, the alternative mentioned above, and all equivalents thereto.

What is claimed is:

1. An apparatus for recording and reproducing a video signal with camera setting data on a record medium, comprising:

means for establishing various camera settings in preparation of imaging a video image;

imaging means for imaging the video image to produce a video signal representing the video image;

means for generating camera setting data identifying the various camera settings established for imaging the video image;

recording means for recording the video signal in a first location of a record medium and for recording the camera setting data in a second location of the record medium separate from the first location;

means for modifying at least one parameter of said video signal read from said first location of said record medium in accordance with at least said camera setting data read from said second location of said record medium;

mode control means for converting the camera setting data into display data and determining whether the display data is to be output in either a first output configuration or a second output configuration in accordance with user commands; and

display control means for controlling the display of said display data.

2. The apparatus of claim **1**, further comprising means for generating date and time data representing a date and time at which the video image is imaged; and wherein said recording means is operable to record the date and time data on said record medium.

3. The apparatus of claim **1**, wherein the record medium is comprised of successive tracks each including a video

data area and a video auxiliary area; and said recording means records the video signal in the video data area and records the camera setting data in the video auxiliary area.

4. The apparatus of claim **3**, wherein said recording means records the camera setting data in a common pack structure in the video auxiliary area of each track on the record medium.

5. The apparatus of claim **1**, wherein said means for establishing is operable to establish an iris setting and a shutter speed of the apparatus, and said means for generating is operable to generate camera setting data identifying the established iris setting and shutter speed.

6. The apparatus of claim **1**, wherein said means for establishing is operable to establish a white balance mode and a focusing mode of the apparatus, and said means for generating is operable to generate camera setting data identifying the established white balance mode and focusing mode.

7. The apparatus of claim **1**, wherein said means for establishing is operable to establish a vertical panning speed and a horizontal panning speed of the apparatus, and said means for generating is operable to generate camera setting data identifying the established vertical panning speed and horizontal panning speed.

8. The apparatus of claim **1**, wherein said means for generating is operable to generate said camera setting data including hand deviation data and vertical distance data representing manual control and a distance of the camera from the video image, respectively.

9. The apparatus of claim **1**, wherein said imaging means is a camera.

10. An apparatus for reproducing a video signal and camera setting data from a record medium, comprising:

reproducing means for reproducing from a record medium a video signal representing a video image imaged by a camera and camera setting data identifying various states of the camera during imaging of the video image;

means for generating display data from the reproduced camera setting data;

means for modifying, in accordance with user instructions and the generated display data, at least one parameter of the reproduced video signal to produce a modified video signal;

mode control means for determining whether the display data is to be output in either a first output configuration or a second output configuration in accordance with user commands;

display control means for controlling the display of said display data; and

means for outputting the modified reproduced video signal and the display data.

11. The apparatus of claim **10**, wherein said reproducing means is operable to reproduce from said record medium date and time data along with said video signal and said camera setting data, said date and time data representing a date and time at which the video image is imaged; and wherein said outputting means outputs said date and time data.

12. The apparatus of claim **10**, wherein said reproducing means is operable to reproduce the video signal from a video data area and the camera setting data from a video auxiliary area of each track on said record medium.

13. The apparatus of claim **12**, wherein the camera setting data is stored as common packs in a common pack structure in the video auxiliary area of each track on the record medium; and said reproducing means is operable to reproduce the common packs having the common pack structure from the video auxiliary areas.

14. The apparatus of claim **10**, wherein said reproducing means is operable to reproduce camera setting data identifying an iris setting, a shutter speed, a white balance mode and a focusing mode representing a state of an imaging apparatus during imaging of the video image.

15. The apparatus of claim **14**, further comprising means for displaying the reproduced iris setting, shutter speed, white balance mode and focusing mode to a user.

16. The apparatus of claim **10**, wherein said reproducing means is operable to reproduce camera setting data identifying a vertical panning speed, a horizontal panning speed, hand deviation data and vertical distance data representing a state of an imaging apparatus during panning imaging of the video image.

17. An apparatus for recording and reproducing a video signal with camera setting data to and from a record medium, comprising:

means for establishing various camera settings in preparation of imaging a video image;

means for imaging the video image to produce a video signal representing the video image;

means for generating camera setting data identifying the various camera settings established for imaging the video image;

recording means for recording the video signal in a first location of a record medium and for recording the camera setting data in a second location of the record medium separate from the first location;

reproducing means for reproducing said video signal and said camera setting data from said record medium;

means for modifying at least one parameter of said video signal in accordance with said reproduced camera setting data;

mode control means for converting the camera setting data into display data and determining whether the display data is to be output in either a first output configuration or a second output configuration in accordance with user commands;

display control means for controlling the display of said display data; and

means for outputting the modified reproduced video signal and the display data.

18. A method of recording and reproducing a video signal with camera setting data on a record medium, comprising the steps of:

establishing various camera settings in preparation of imaging a video image;

imaging the video image to produce a video signal representing the video image;

generating camera setting data identifying the various camera settings established for imaging the video image;

recording the video signal in a first location of a record medium and the camera setting data in a second location of the record medium separate from the first location;

modifying at least one parameter of said video signal read from said first location of said record medium in accordance with at least said camera setting data read from said second location of said record medium;

converting the camera setting data into display data;

determining whether the display data is to be output in either a first output configuration or a second output configuration in accordance with user commands; and

controlling the display of said display data.

19. The method of claim 18, further comprising the step of generating date and time data representing a date and time at which the video image is imaged; and wherein said recording step is carried out by recording the video signal, the camera setting data, and the date and time data on the record medium.

20. The method of claim 18, wherein the record medium is comprised of successive tracks each including a video data area and a video auxiliary area; and said recording step is carried out by recording the video signal in the video data area and recording the camera setting data in the video auxiliary area.

21. The method of claim 20, wherein said recording step is carried out by recording the camera setting data in a common pack structure in the video auxiliary area of each track on the record medium.

22. The method of claim 18, wherein said step of establishing is carried out by establishing an iris setting and a shutter speed of an imaging device, and said step of generating is carried out by generating camera setting data identifying the established iris setting and shutter speed.

23. The method of claim 18, wherein said step of establishing is carried out by establishing a white balance mode and a focusing mode of an imaging device, and said step of generating is carried out by generating camera setting data identifying the established white balance mode and focusing mode.

24. The method of claim 18, wherein said step of establishing is carried out by establishing a vertical panning speed and a horizontal panning speed of an imaging device, and said step of generating is carried out by generating camera setting data identifying the established vertical panning speed and horizontal panning speed.

25. The method of claim 18, wherein said step of generating is carried out by generating said camera setting data including hand deviation data and vertical distance data representing manual control and a distance of the camera from the video image during imaging, respectively.

26. A method of reproducing a video signal and camera setting data from a record medium, comprising the steps of:

reproducing from a record medium a video signal representing a video image imaged by a camera and camera setting data identifying various states of the camera during imaging of the video image;

generating display data from the reproduced camera setting data;

determining whether the display data is to be output in either a first output configuration or second output in accordance with user commands;

modifying, in accordance with user instructions and the displayed generated display data, at least one parameter of the reproduced video signal to produce a modified video signal; and

outputting the modified reproduced video signal and the display data.

27. The method of claim 26, wherein said reproducing step is carried out by reproducing from said record medium date and time data along with said video signal and said camera setting data, said date and time data representing a date and time at which the video image is imaged; and further comprising the step of outputting the reproduced date and time data.

28. The method of claim 26, wherein said reproducing step is carried out by reproducing the video signal from a video data area and the camera setting data from a video auxiliary area of each track on said record medium.

29. The method of claim 28, wherein the camera setting data is stored as common packs in a common pack structure in the video auxiliary area of each track on the record medium; and said reproducing step is carried out by reproducing the common packs having the common pack structure from the video auxiliary areas.

30. The method of claim 26, wherein said reproducing step is carried out by reproducing camera setting data identifying an iris setting, a shutter speed, a white balance mode and a focusing mode representing a state of an imaging apparatus during imaging of the video image.

31. The method of claim 30, further comprising the step of displaying the reproduced iris setting, shutter speed, white balance mode and focusing mode to a user.

32. The method of claim 26, wherein said reproducing step is carried out by reproducing camera setting data identifying a vertical panning speed, a horizontal panning speed, hand deviation data and vertical distance data representing a state of an imaging apparatus during panning imaging of the video image.

33. A method of recording and reproducing a video signal with camera setting data to and from a record medium, comprising the steps of:

establishing various camera settings in preparation of imaging a video image;

imaging the video image to produce a video signal representing the video image;

generating camera setting data identifying the various camera settings established for imaging the video image;

recording the video signal in a first location of a record medium and the camera setting data in a second location of the record medium separate from the first location;

reproducing said video signal and said camera setting data from said record;

converting the camera setting data into display data and determining whether the display data is to be output in either a first output configuration or a second output configuration in accordance with user commands;

modifying at least one parameter of said video signal in accordance with said reproduced camera setting data;

controlling the display of said display data; and

outputting the modified reproduced video signal and the generated display data.

* * * * *

EXHIBIT E

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(45) **Date of Patent: Jul. 23, 2002**

(54) **SOLID-STATE IMAGE-SENSING DEVICE AND METHOD FOR PRODUCING THE SAME**

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,343,060 A * 8/1994 Abe 257/229
5,514,887 A * 5/1996 Hokari 257/222
5,581,099 A * 12/1996 Kusaka et al. 257/222
5,625,210 A * 4/1997 Lee et al. 257/292
5,736,756 A * 4/1998 Wakayama et al. 257/223
5,962,882 A * 10/1999 Sin 257/222

* cited by examiner

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(57) **ABSTRACT**

A solid-state image-sensing device has pn-junction sensor parts isolated corresponding to pixels by a device isolation layer. The solid-state image-sensing device includes a first-conductivity-type second semiconductor well region formed between a first-conductivity-type first semiconductor well region and the device isolation layer. When the device is operating, a depletion layer of each sensor part spreads to the first semiconductor well region, which is beneath each of the sensor parts.

7 Claims, 18 Drawing Sheets

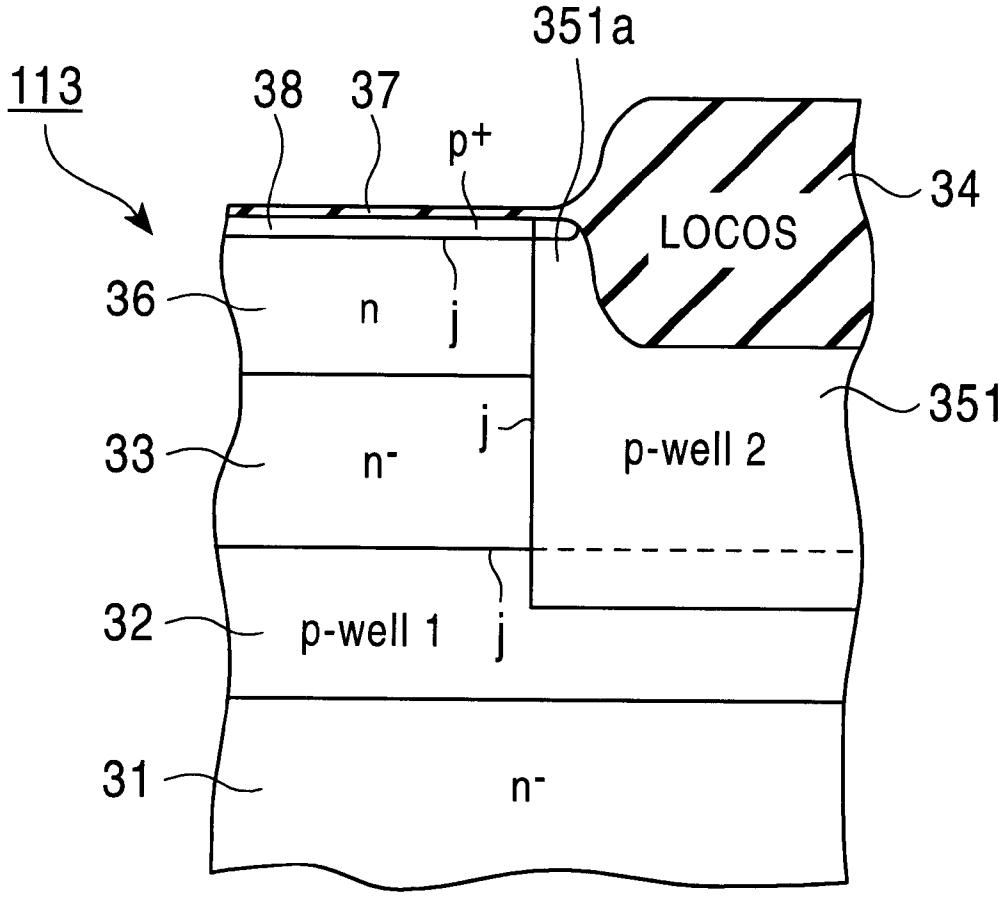


FIG. 1

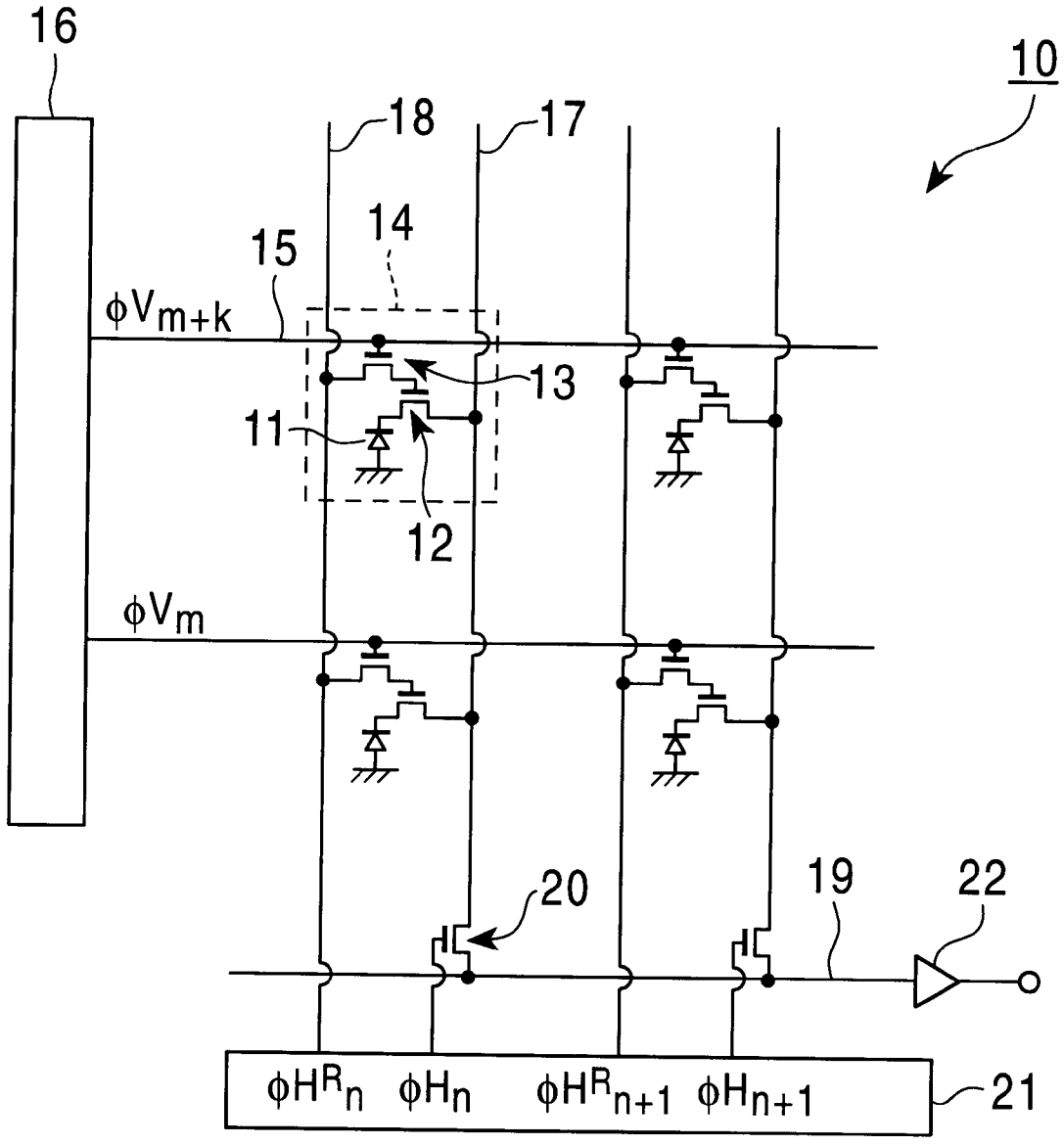

16
10
18
17
14
15
ϕV_{m+k}
13
11
12
ϕV_m
20
19
22
ϕH^R_n ϕH_n ϕH^R_{n+1} ϕH_{n+1}
21

FIG. 2

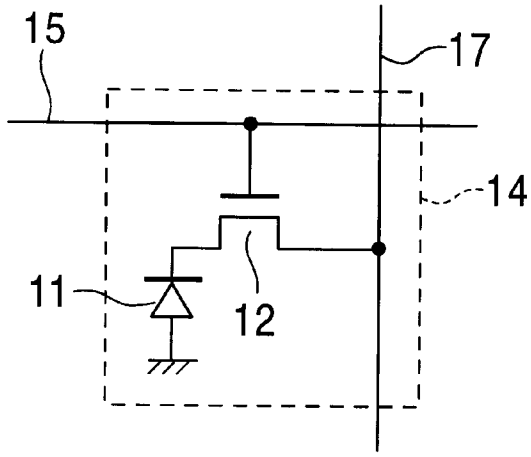


FIG. 3

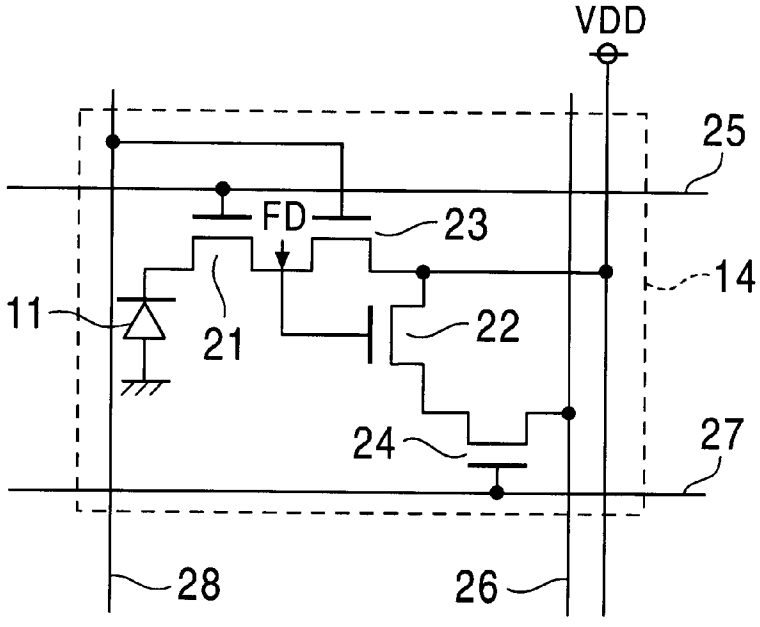


FIG. 4

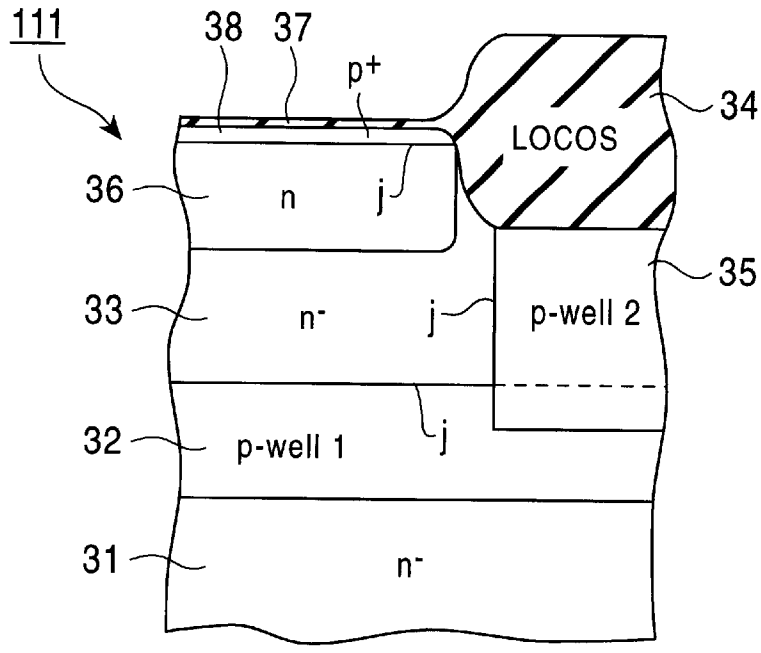

111
38
37
p+
34
LOCOS
36
n
j
35
33
n-
j
p-well 2
j
32
p-well 1
31
n-

FIG. 5

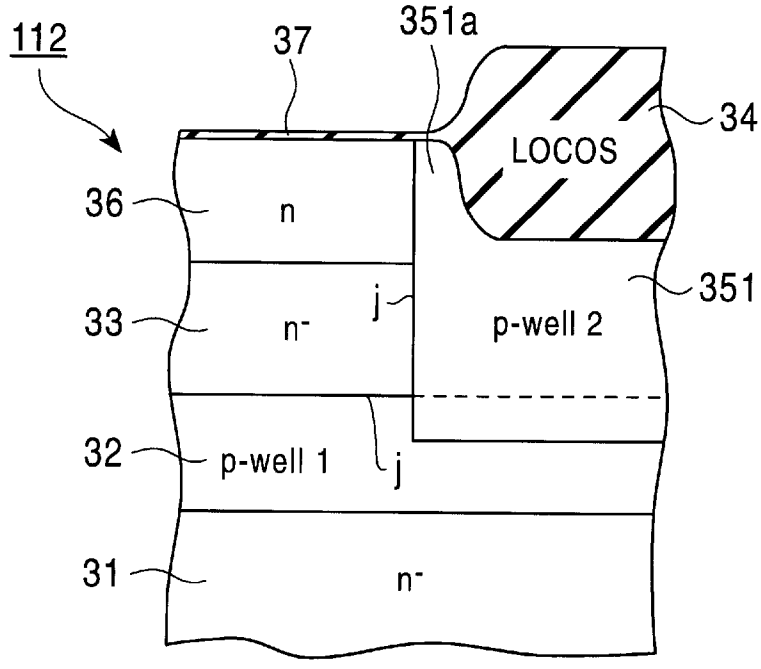

112
37
351a
34
LOCOS
36
n
351
33
n-
j
p-well 2
32
p-well 1
j
31
n-

FIG. 6

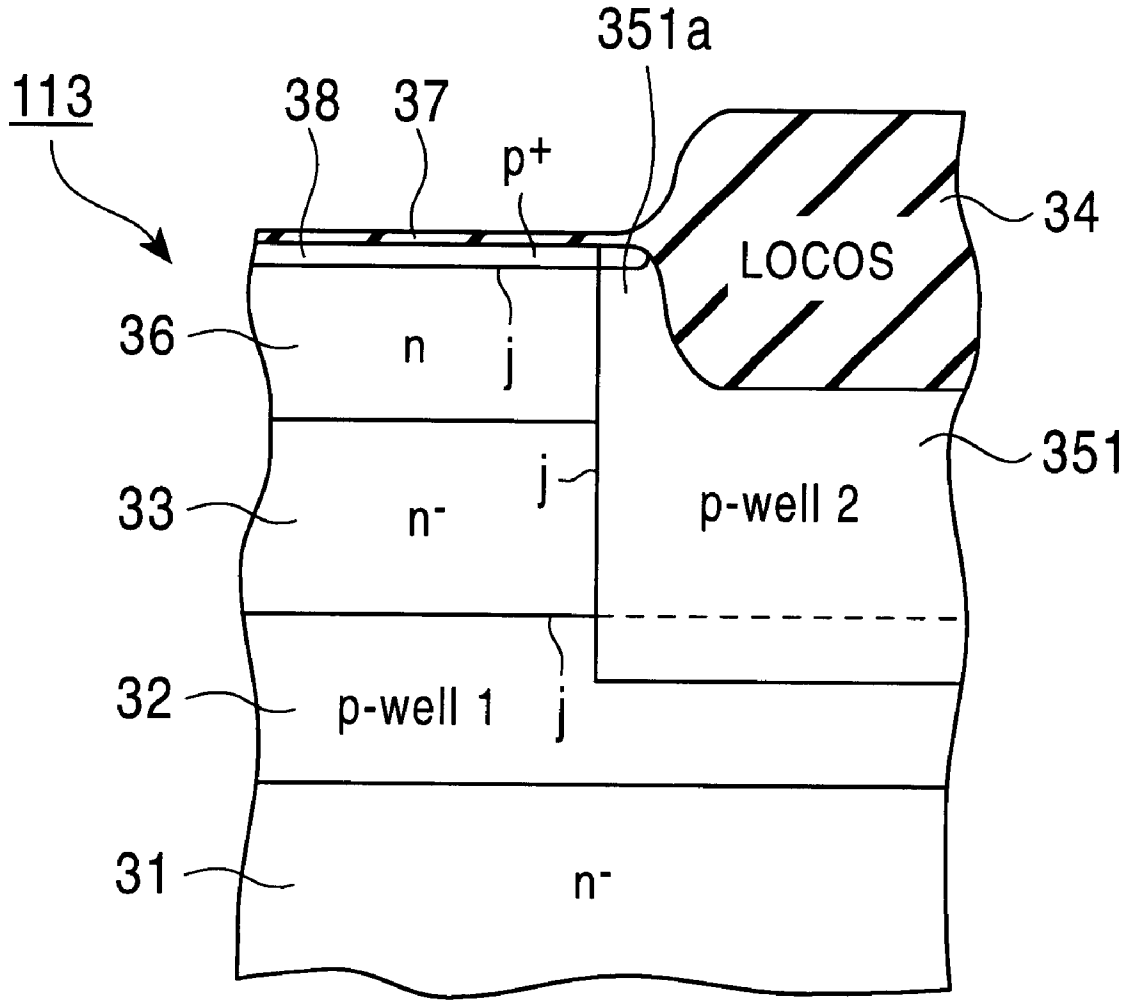


FIG. 7A

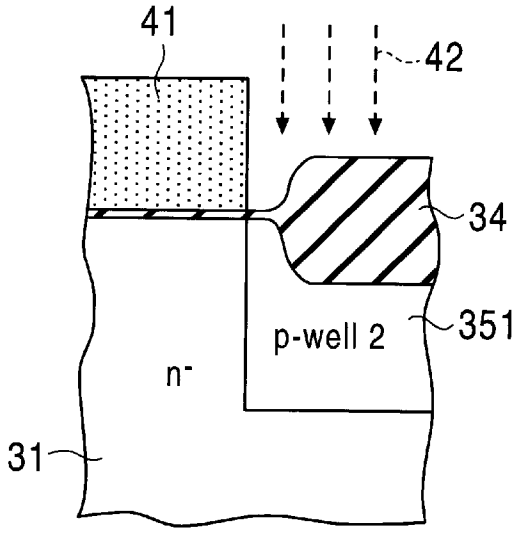


FIG. 7B

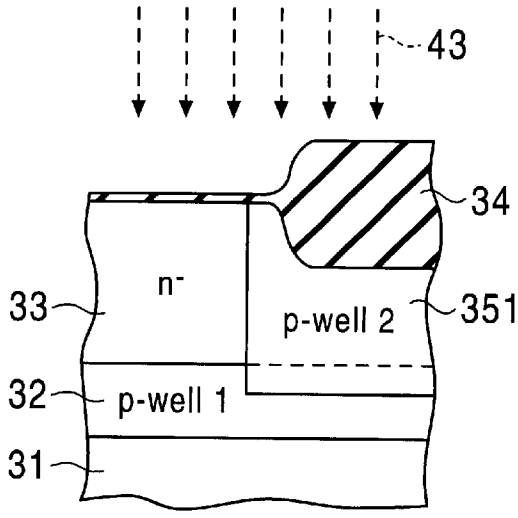


FIG. 7C

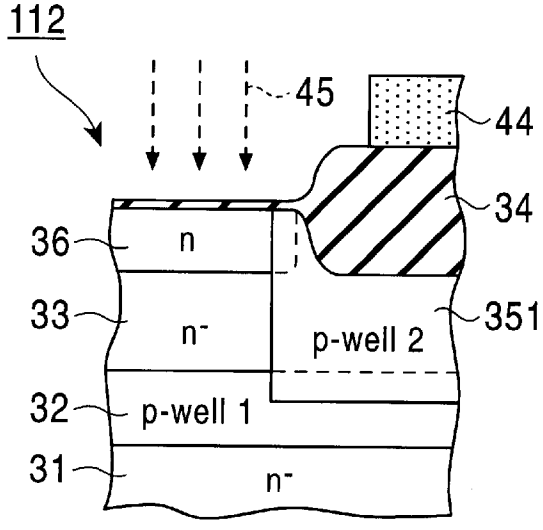


FIG. 7D

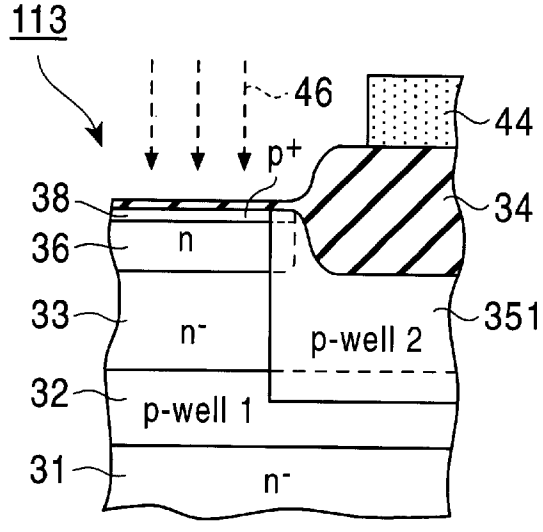


FIG. 8

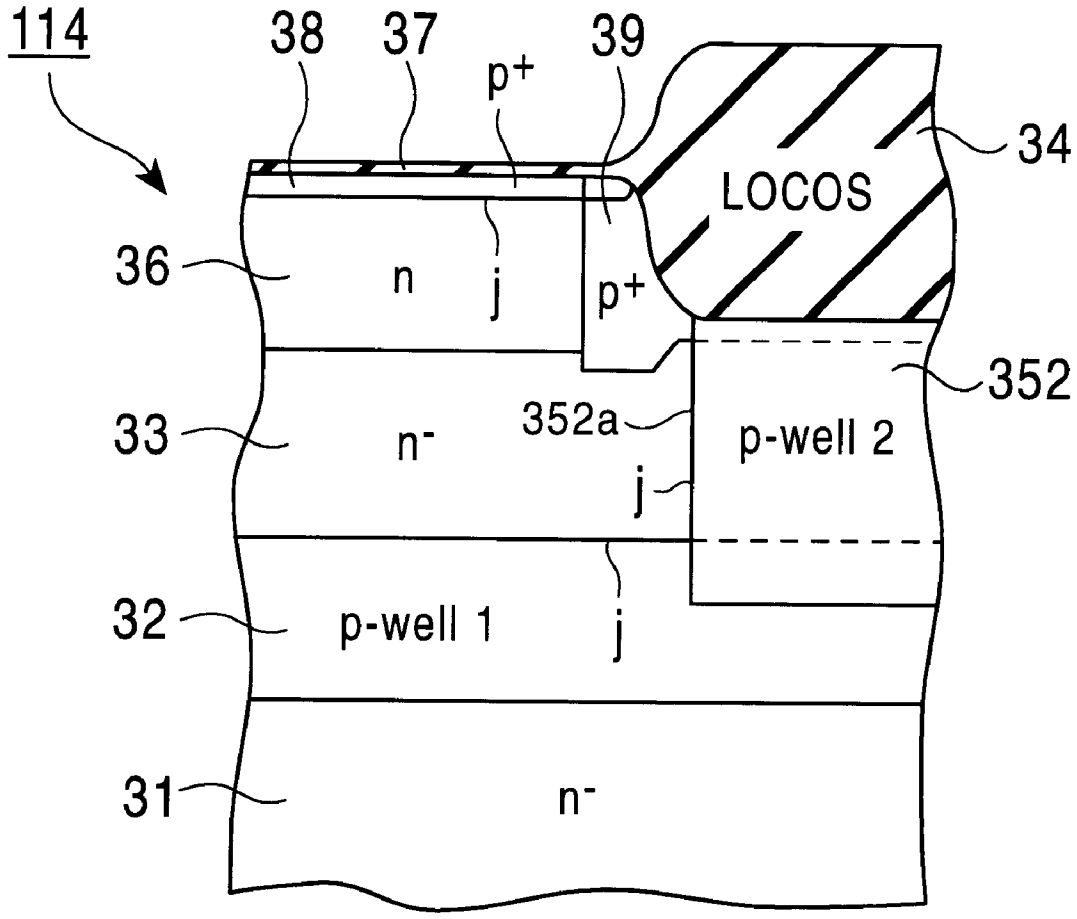

114
38
37
p+
39
34
LOCOS
36
n
j
p+
352
33
n-
352a
p-well 2
j
32
p-well 1
j
31
n-

FIG. 9A

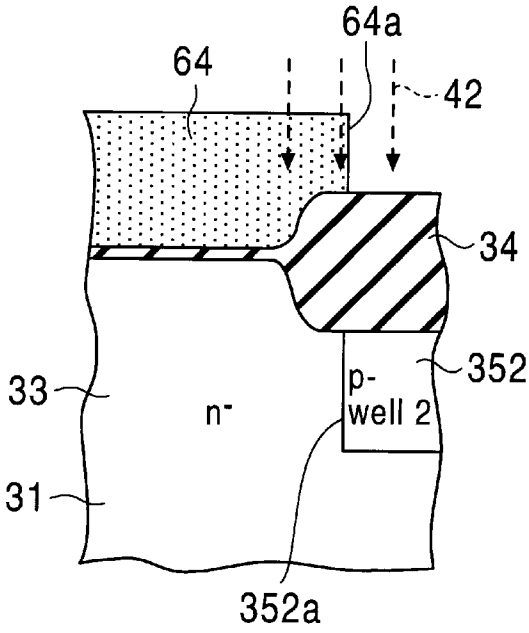


FIG. 9B

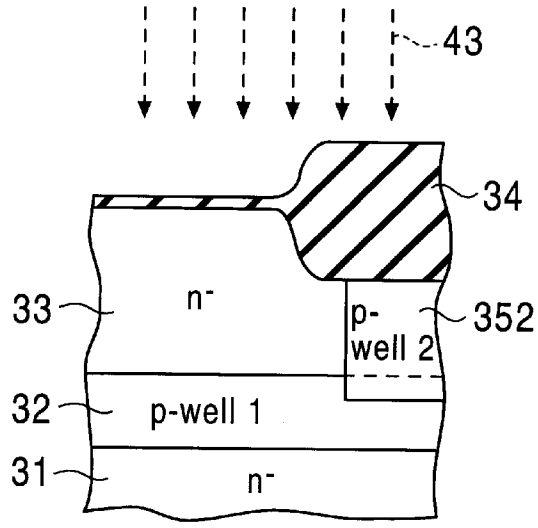


FIG. 9C

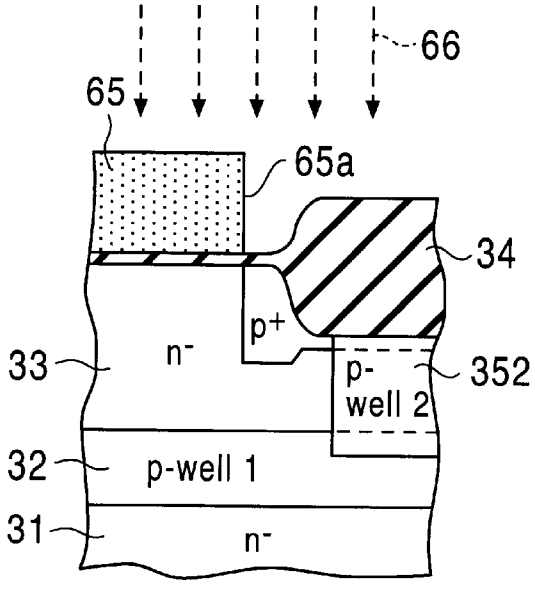


FIG. 9D

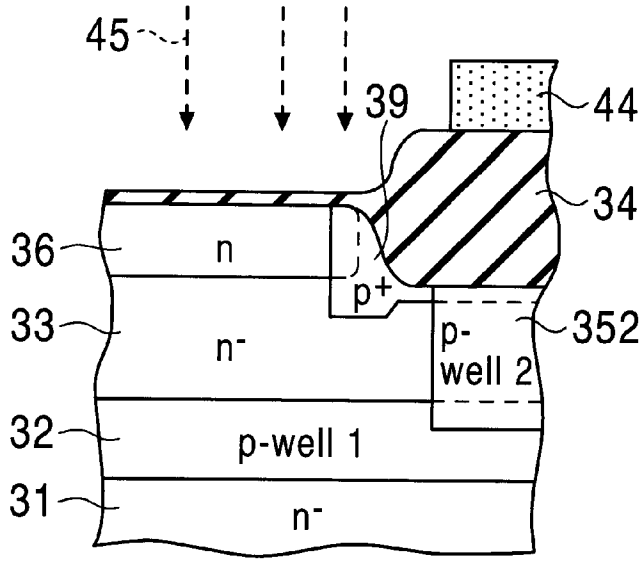

45
39
44
34
36
n
p+
33
n-
p-
well 2
352
32
p-well 1
31
n-

FIG. 9E

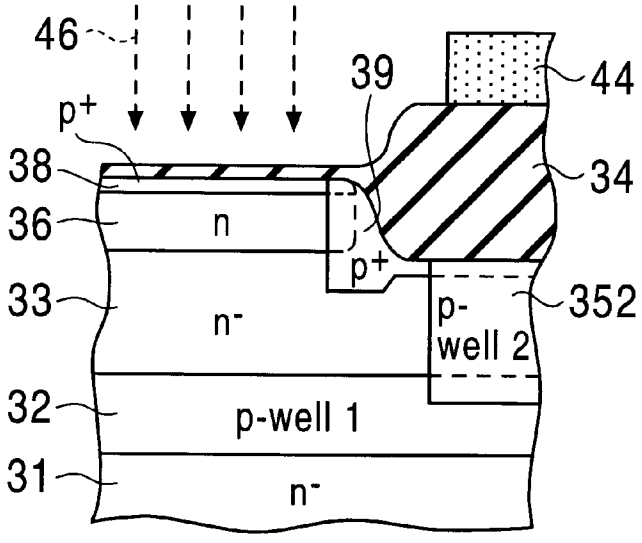

46
39
44
p+
38
34
36
n
p+
33
n-
p-
well 2
352
32
p-well 1
31
n-

FIG. 10A

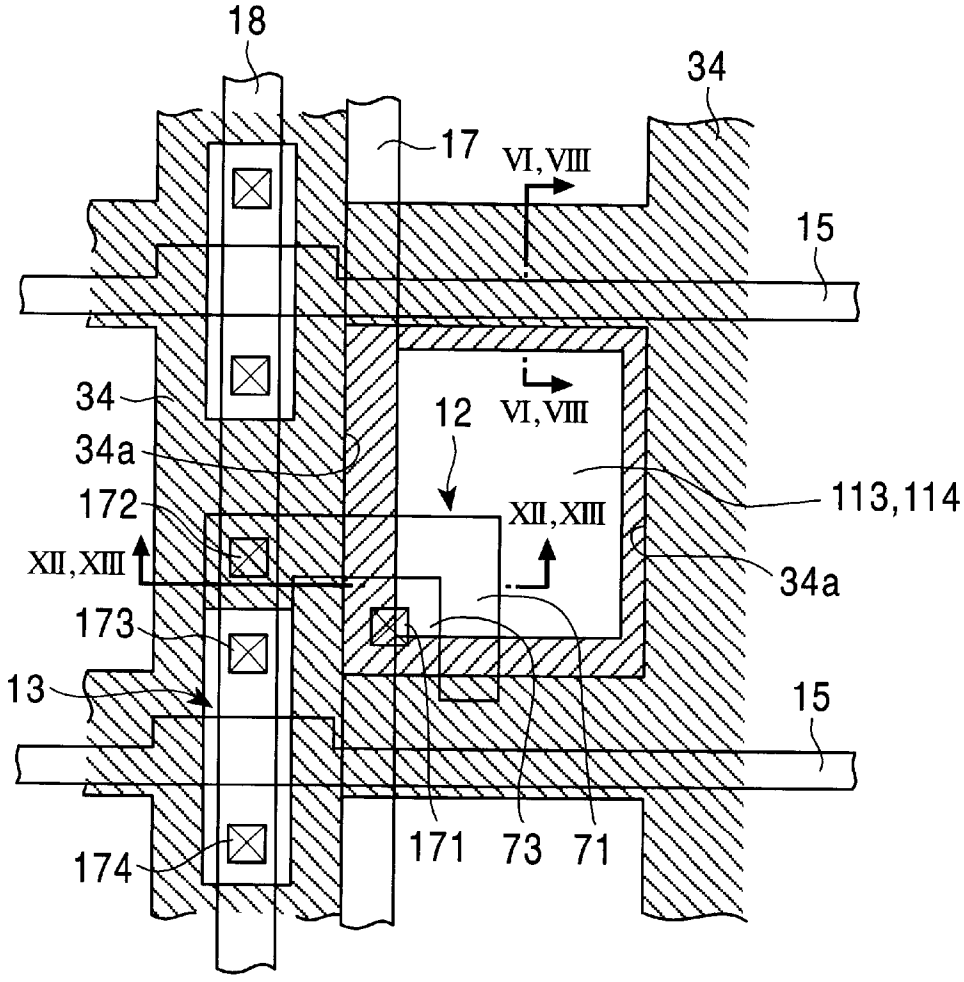


FIG. 10B

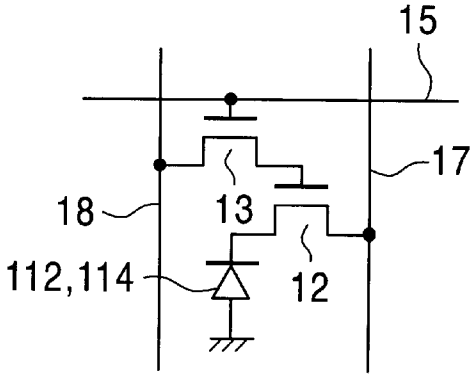


FIG. 11

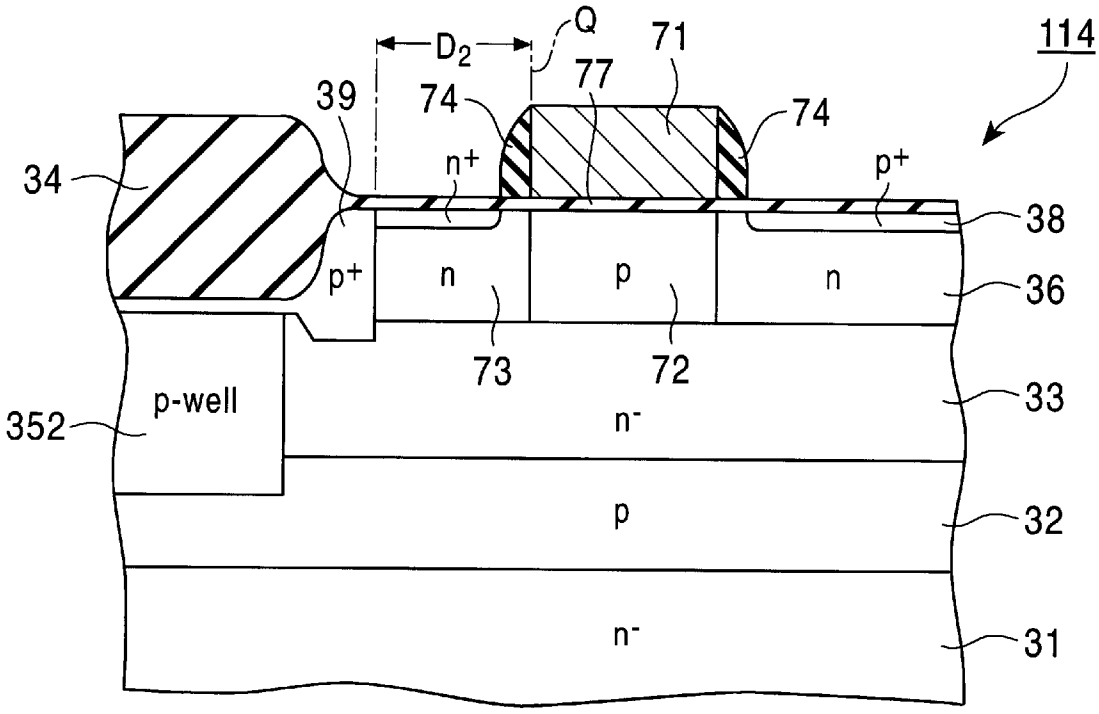


FIG. 12

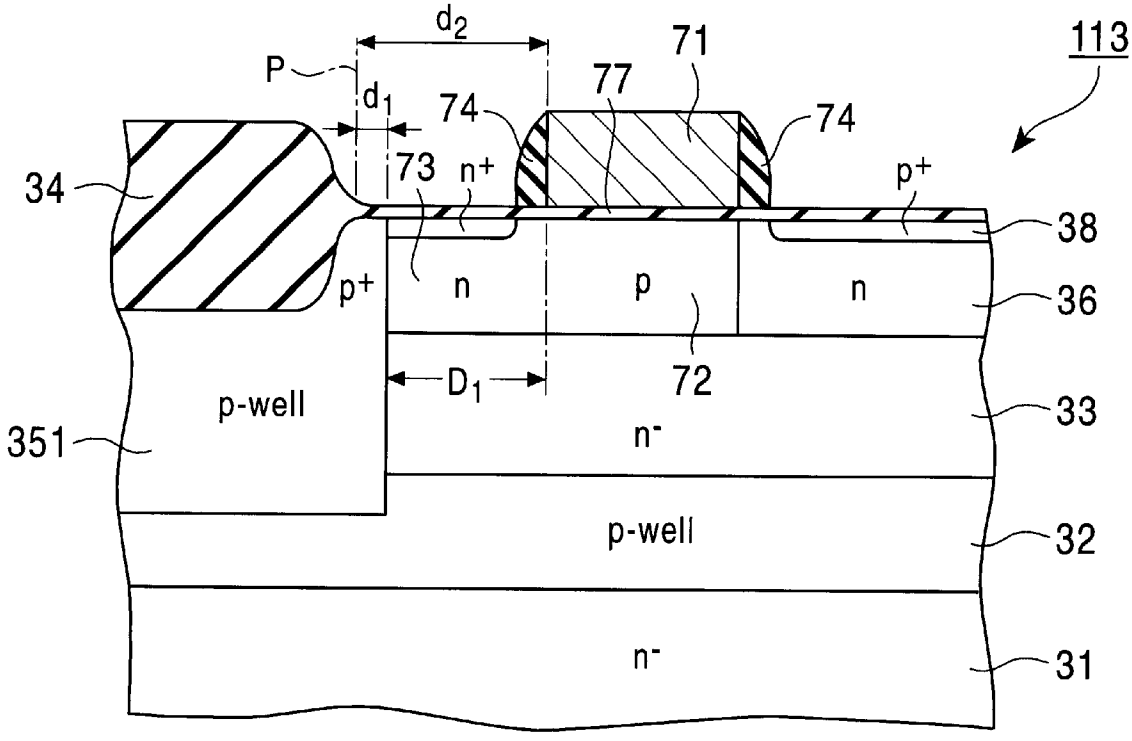

d2
P
d1
74
71
77
74
113
34
73
n+
p+
38
p+
n
p
n
36
D1
72
p-well
351
33
n-
p-well
32
n-
31

FIG. 13A

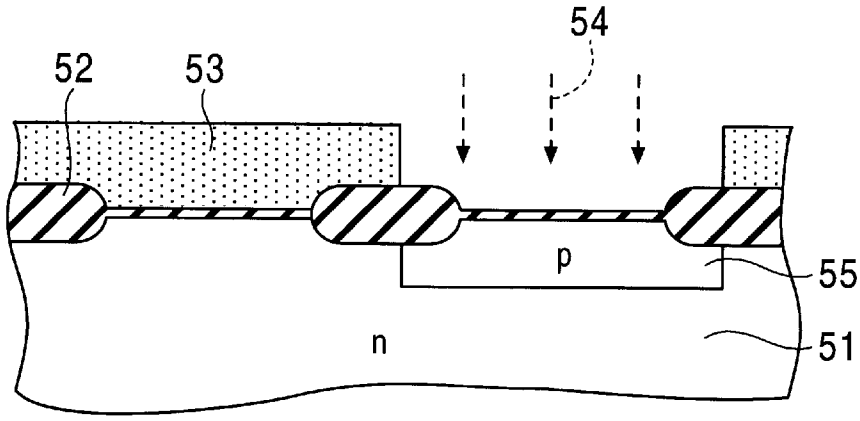


FIG. 13B

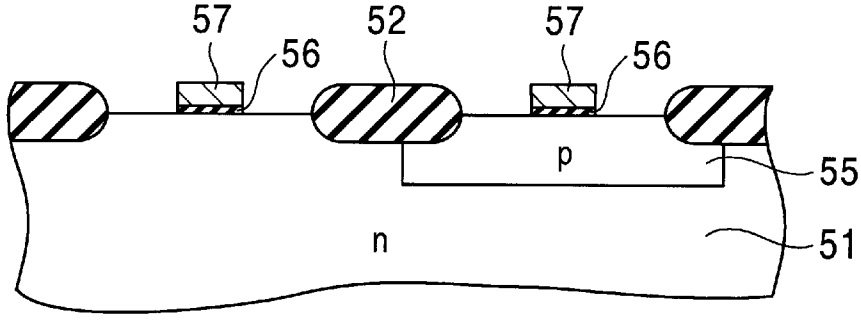


FIG. 13C

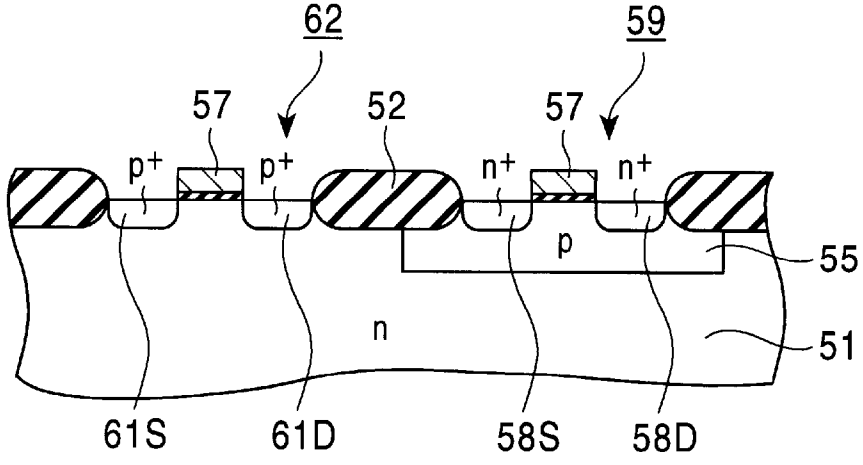


FIG. 14

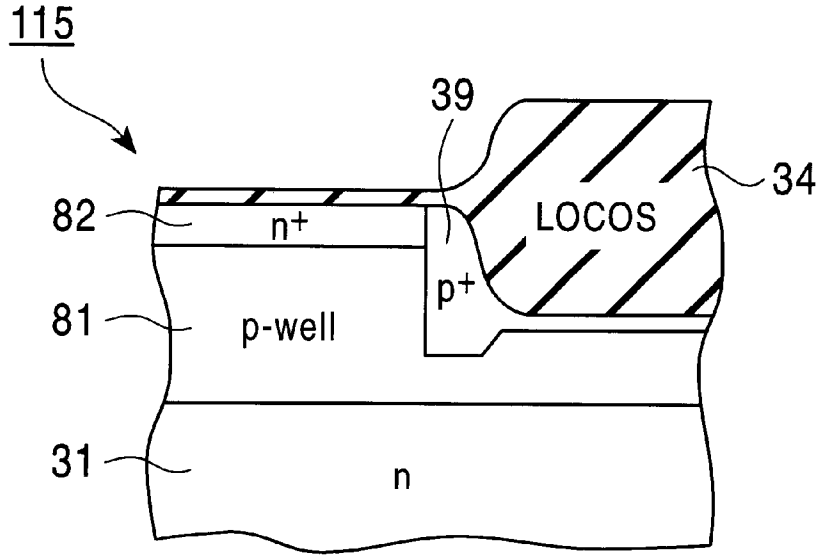

115
39
34
82
n+
LOCOS
p+
81
p-well
31
n

FIG. 15

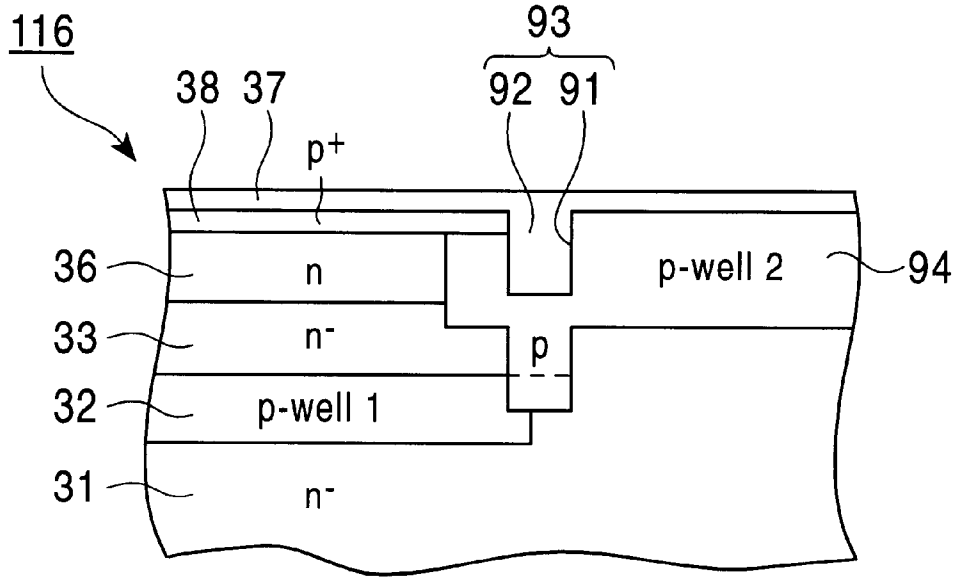

116
93
38 37
92 91
p+
36
n
p-well 2
94
33
n-
p
32
p-well 1
31
n-

FIG. 16

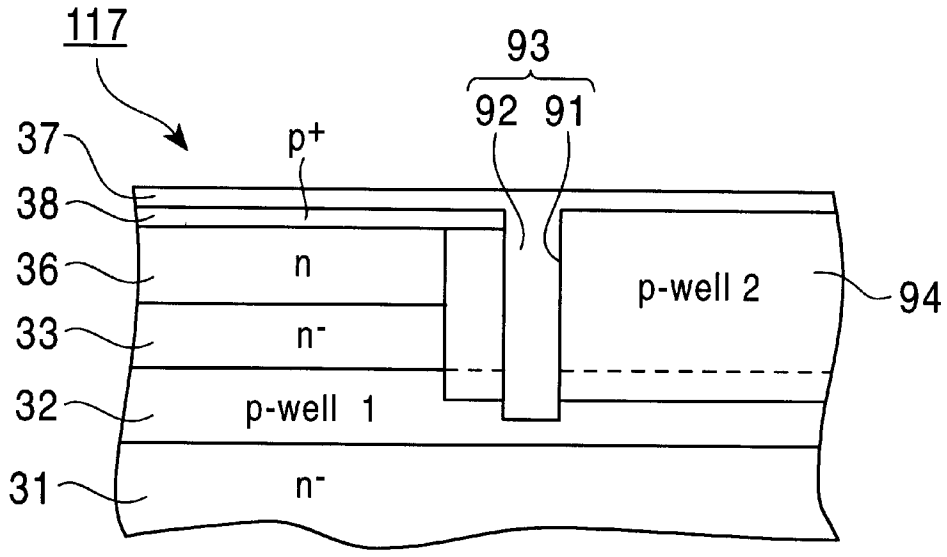

117
93
92 91
37
p+
38
36
n
p-well 2
94
33
n-
32
p-well 1
31
n-

FIG. 17

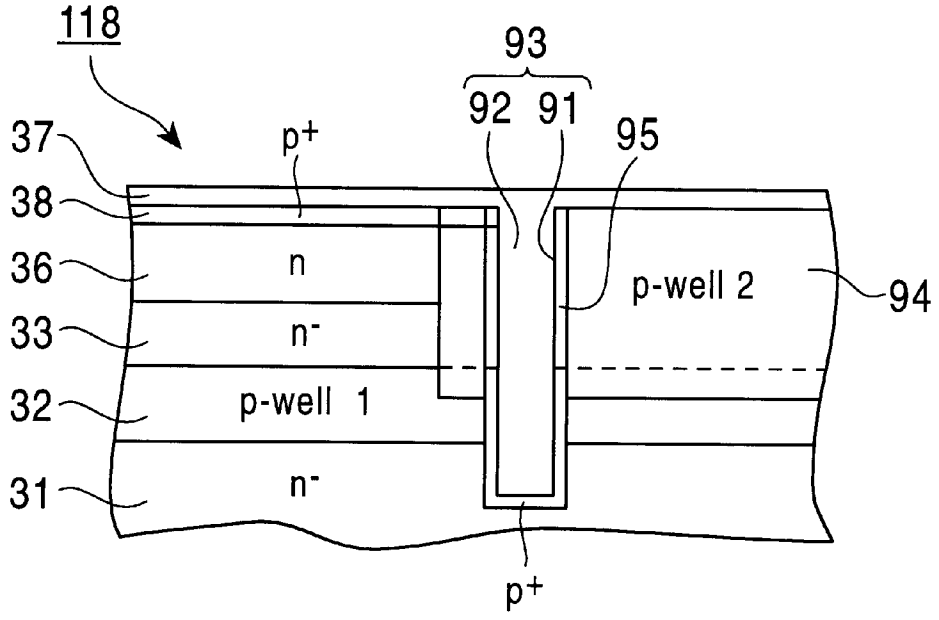

118
93
92 91
95
37
p+
38
36
n
p-well 2
94
33
n-
32
p-well 1
31
n-
p+

FIG. 18A

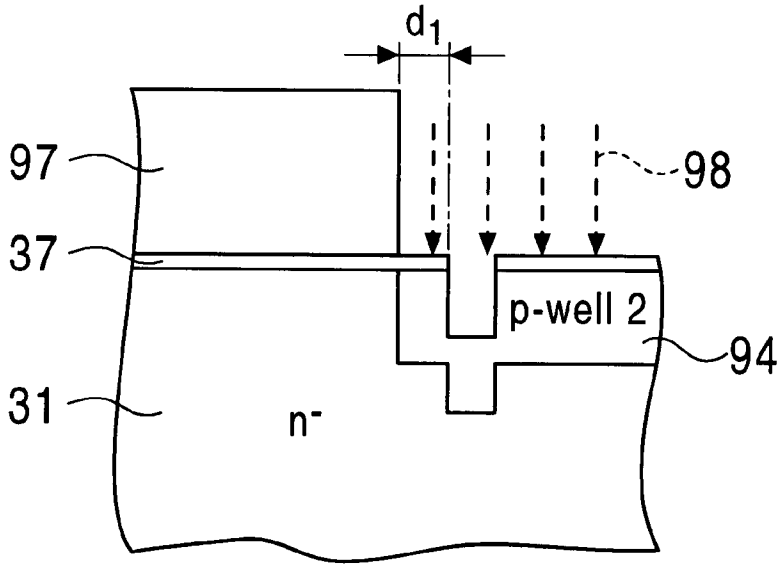


FIG. 18B

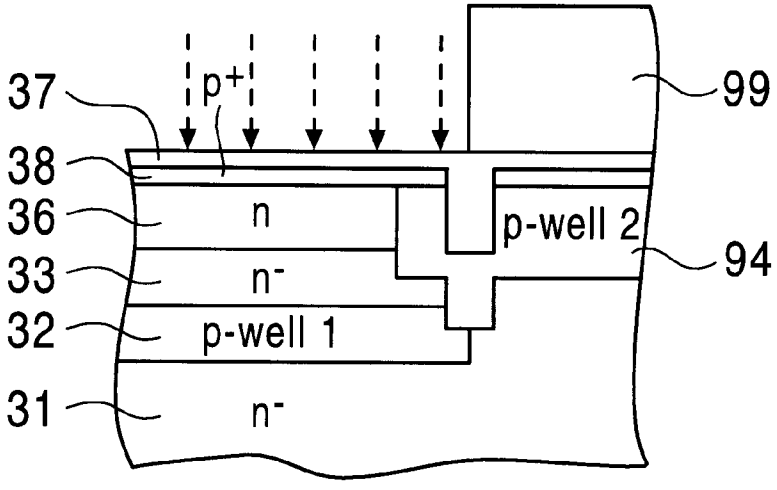


FIG. 19A

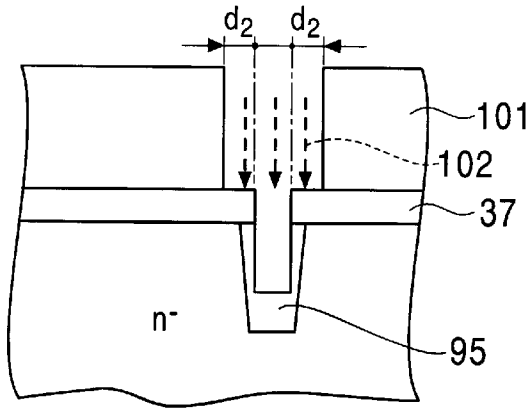


FIG. 19B

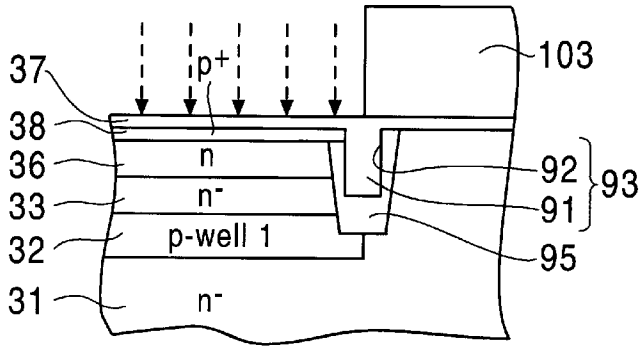


FIG. 19C

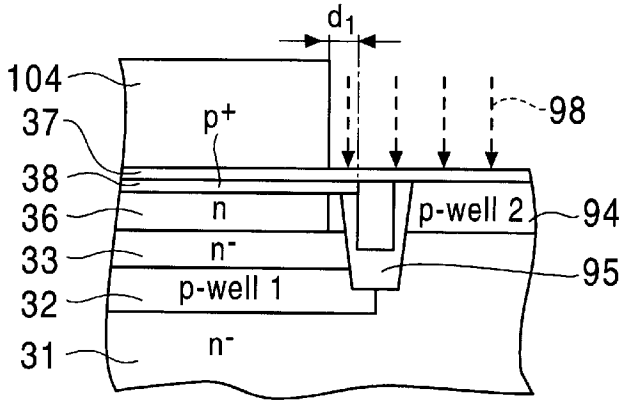


FIG. 20A

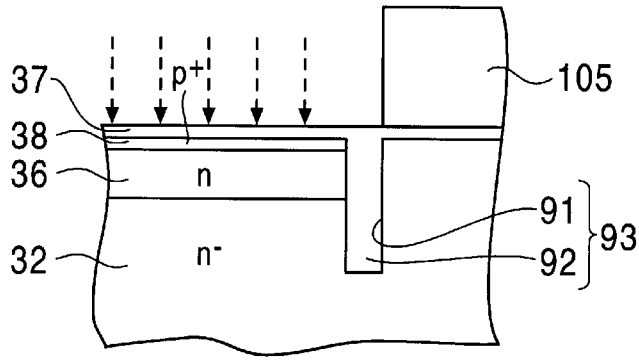


FIG. 20B

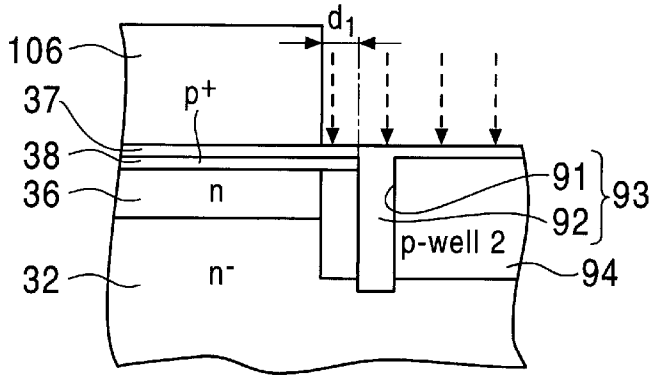


FIG. 20C

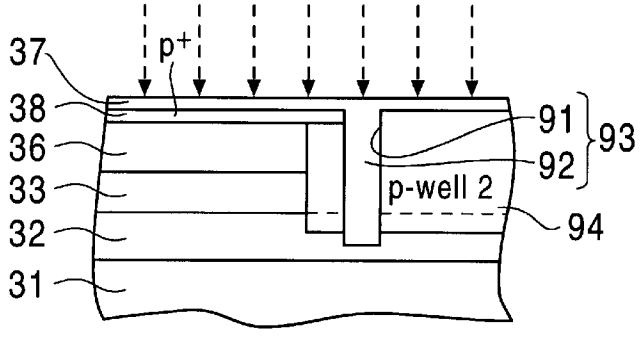
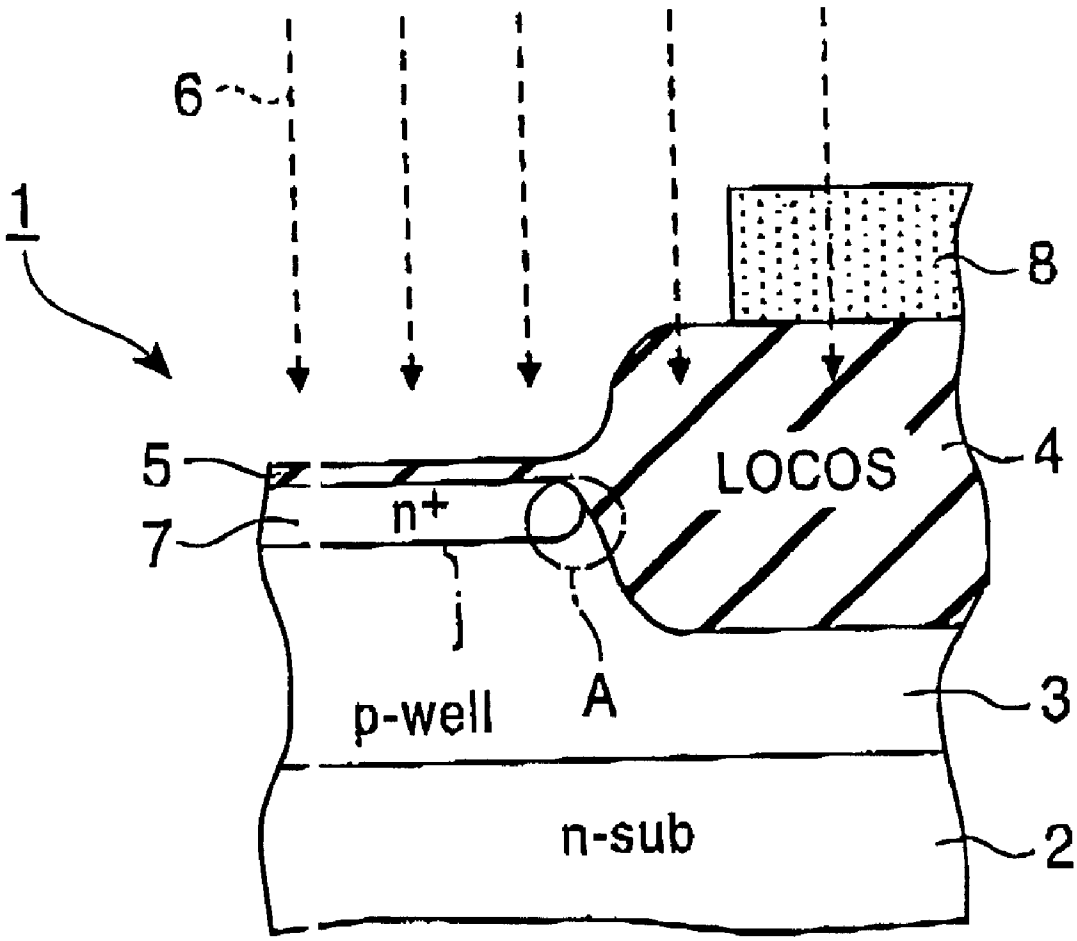


FIG. 21

PRIOR ART



SOLID-STATE IMAGE-SENSING DEVICE AND METHOD FOR PRODUCING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to solid-state image-sensing sensing devices, and particularly to a metal-oxide-semiconductor semiconductor (MOS) or complementary-metal-oxide-semiconductor semiconductor (CMOS) solid-state image-sensing device and a method for producing the device.

2. Description of the Related Art

As a type of solid-state image-sensing device, an MOS or CMOS solid-state image-sensing device is known that includes unit pixels each including a photodiode sensor and a switching device and that reads signal charge accumulated in the sensor by photoelectric conversion, converts the charge into a voltage or current, and outputs it. In the MOS or CMOS solid-state image-sensing device, MOS transistors or CMOS transistors are used as, for example, switching devices for pixel selection and switching devices for reading signal charge. Also in peripheral circuits such as a horizontal scanning circuit and a vertical scanning circuit, MOS transistors or CMOS transistors are used, so that there is an advantage in that the transistors can be produced together with the switching devices.

Hitherto, in a MOS or CMOS solid-state image-sensing device using pn-junction transistors as sensors, the sensors of pixels are formed so that the pixels are isolated in the form of an X-Y matrix by a device isolation layer resulting from local oxidation, i.e., a so-called "LOCOS (local oxidation of silicon) layer".

As shown in FIG. **21**, a photodiode **1** to be used as a sensor is formed by forming a p-type semiconductor well region **3** on, for example, an n-type silicon substrate **2**, forming a device isolation layer (LOCOS layer) **4** resulting from local oxidation, and performing ion implantation of an n-type impurity **6** such as arsenic (As) or phosphorus (P) in the surface of the p-type semiconductor well region **3** through a thin insulating film (e.g., an SiO_2 film) so that an n-type semiconductor layer **7** is formed.

In the sensor (photodiode) **1**, it is necessary that a depletion layer be enlarged for increasing the photoelectric conversion efficiency so that even signal charge photoelectrically converted at a deeper position can be used.

In order to dope the n-type impurity **6** in the formation of the photodiode **1** to be used as a sensor, ion implantation is performed using a photoresist layer **8** aligned on the device isolation layer **4** to protect other regions, as shown in FIG. **21**. Thus, a pn-junction j appears at an end A of the device isolation layer **4**. It is known that a stress generates crystal defects such as dislocation at the end A of the device isolation layer **4**. Accordingly, when the depletion layer, generated by reverse biasing the pn-junction junction j, occurs in the region of at the end of the device isolation layer, which has the crystal defects, a leakage current is increased by the electric field. When the leakage current is increased in the sensor (photodiode) **1**, a signal charge is generated and forms a dark current, even if no light is incident. Since the dark current is generated by the crystal defects, each sensor **1** has a different amount of generated dark current, which appears as nonuniformity of the image quality.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a solid-state image-sensing device designed so that photoelectric conversion efficiency in sensor parts can be increased.

It is another object of the present invention to provide a solid-state image-sensing device designed so that a dark current resulting from leakage current can be reduced, and to provide a method for producing the device.

To these ends, according to an aspect of the present invention, the foregoing objects are achieved through provision of a solid-state image-sensing device having pn-junction sensor parts isolated corresponding to pixels by a device isolation layer. The solid-state image-sensing device includes a first-conductivity-type second semiconductor well region formed between a first-conductivity-type first semiconductor well region and the device isolation layer. In the device, when the device is operating, a depletion layer of each of the sensor parts spreads to the first semiconductor well region, which is beneath each of the sensor parts.

Preferably, the second semiconductor well region is simultaneously formed with the semiconductor well regions formed after the formation of the device isolation layer in a CMOS transistor.

According to another aspect of the present invention, the foregoing objects are achieved through provision of a solid-state image-sensing device having pn-junction sensor parts isolated corresponding to pixels by a device isolation layer resulting from local oxidation. The solid-state image-sensing device includes a semiconductor region of a conductivity type opposite to the conductivity type of a charge accumulating region of each of the sensor parts, and the semiconductor region is formed between the charge accumulating region of each sensor part and the device isolation layer.

Preferably, the solid-state image-sensing device further includes a second semiconductor well region formed between the device isolation layer and a first semiconductor well region beneath the device isolation layer, and when the device is operating, the depletion layer of each of the sensor parts spreads to the first semiconductor well region, which is beneath each of the sensor parts.

The semiconductor region may be formed by extending a portion of a second semiconductor well region formed between the device isolation layer and a first semiconductor well region beneath the device isolation layer.

According to a further aspect of the present invention, the foregoing objects are achieved through provision of a solid-state image-sensing device including pn-junction sensor parts isolated corresponding to pixels by a device isolation layer resulting from trench isolation. The solid-state image-sensing device includes a semiconductor region of a conductivity type opposite to the conductivity type of the charge accumulating region of each of the sensor parts, and the semiconductor region is formed to extend from the device isolation layer to a pixel region.

Preferably, the opposite-conductivity-type semiconductor region is formed by extending a portion of a semiconductor well region.

According to a still further aspect of the present invention, the foregoing objects are achieved through provision of a method for producing a solid-state image-sensing device which includes the step of forming, by performing ion implantation, a semiconductor region after forming a device isolation layer resulting from local oxidation, wherein the device isolation layer isolates pn-junction sensor parts in correspondence with pixels; the conductivity type of the semiconductor region is opposite to the conductivity type of a charge accumulating region of each of the sensor parts; and an end of the semiconductor region is positioned at the side of the parts except for an end of the device isolation layer.

Preferably, the semiconductor region is formed by a second semiconductor well region formed between a first semiconductor well region and the device isolation layer.

In the method, after forming the device isolation layer, the semiconductor region may be formed by forming, beneath the device isolation layer, a second semiconductor well region leading to a first semiconductor well region.

According to yet another aspect of the present invention, the foregoing objects are achieved through provision of a method for producing a solid-state image-sensing device which includes the steps of: forming a device isolation layer resulting from local oxidation, the device isolation layer isolating pn-junction sensor parts corresponding to pixels, and for forming a gate electrode of a read transistor connected to each of the sensor parts; and forming, by performing ion implantation, a semiconductor region of a conductivity type opposite to the conductivity type of the charge accumulating region of each of the sensor parts so that an end of the semiconductor region is positioned at the side of the sensor parts except for an end of the device isolation layer, with the gate electrode being used as a reference position.

According to still another aspect of the present invention, the foregoing objects are achieved through provision of a method for producing a solid-state image-sensing sensing device which includes the step of forming a semiconductor region of a conductivity type opposite to the conductivity type of a charge accumulating region in each of pn-junction sensor parts so as to surround a device isolation layer resulting from trench isolation, wherein the device isolation layer isolates the pn-junction sensor parts corresponding to pixels.

According to a more aspect of the present invention, the foregoing objects are achieved through provision of a method for producing a solid-state image-sensing device which includes the step of forming, after forming, on a semiconductor substrate, trenches for isolating pn-junction sensor parts corresponding to pixels, and after forming a semiconductor region of a conductivity type opposite to the conductivity type of a charge accumulating region of each of the sensor parts so as to surround each trench, a device isolation layer by embedding an insulating material in each trench.

According to the present invention, photoelectric conversion efficiency in sensor parts in a solid-state image-sensing device can be increased, which makes it possible to provide a solid-state image-sensing device with high sensitivity.

According to the present invention, sensor parts having high photoelectric conversion efficiency and a low dark current can be formed without increasing production steps.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing an embodiment of a solid-state image-sensing device according to the present invention;

FIG. **2** is a circuit diagram showing another example of a unit pixel applied to a solid-state image-sensing device of the present invention;

FIG. **3** is a circuit diagram showing another example of a unit pixel applied to a solid-state image-sensing device of the present invention;

FIG. **4** is a main part sectional view showing an embodiment of a sensor in a solid-state image-sensing device according to the present invention;

FIG. **5** is a sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIG. **6** is a sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIGS. **7**A to **7**D are sectional views showing a process for producing the sensors in FIGS. **5** and **6**;

FIG. **8** is a main part sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIGS. **9**A to **9**E are sectional views showing a process for producing the sensor in FIG. **8**;

FIG. **10**A a main part plan view showing an embodiment of a solid-state image-sensing device provided with a sensor according to the present invention, and FIG. **10**B is an equivalent circuit diagram of a unit pixel of the sensor;

FIG. **11** is a sectional view taken on line XII,XIII—XII, XIII in FIG. **10**A in the case where the sensor in FIG. **8** illustrating the present invention is included;

FIG. **12** is a sectional view taken on line XII,XIII—XII, XIII in FIG. **11** in the case where the sensor in FIG. **6** illustrating the present invention is included;

FIGS. **13**A to **13**C are sectional views showing a process for producing a CMOS transistor included in the peripheral circuit of a solid-state image-sensing device;

FIG. **14** is a main part sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIG. **15** is a sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIG. **16** is a sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIG. **17** is a sectional view showing another embodiment of the sensor in the solid-state image-sensing device according to the present invention;

FIGS. **18**A and **18**B are process charts showing a method (according to an embodiment of the present invention) for producing a sensor part obtained by trench device isolation;

FIGS. **19**A, **19**B, and **19**C are process charts showing a method (according to another embodiment of the present invention) for producing a sensor part obtained by trench device isolation;

FIGS. **20**A, **20**B, and **20**C are process charts showing a method (according to another embodiment of the present invention) for producing a sensor part obtained by trench device isolation; and

FIG. **21** is a main part sectional view showing a sensor part in a conventional solid-state image-sensing device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows a solid-state image-sensing device of, for example, a CMOS type, according to an embodiment of the present invention.

A solid-state image-sensing device **10** includes: an image sensing region formed by providing, in the form of a matrix, a plurality of unit pixels **14** in which each unit pixel includes a photodiode (i.e., a pn-junction sensor) **11** for performing photoelectric conversion, a vertical-selection switching device (e.g., a MOS transistor) **13** for selecting a pixel, and a read switching device (e.g., a MOS transistor) **12**; a vertical scanning circuit **16** for outputting vertical scanning pulses ϕV [ϕV_1, . . . ϕV_m, . . . ϕV_{m+k}, . . .] to vertical selection lines **15** to which the control electrodes (so-called

"gate electrodes") of the vertical-selection switching devices **13** for each row are commonly connected; vertical signal lines **17** to which main electrodes of the read switching devices **12** for each column are commonly connected to each column; read pulse lines **18** connected to main electrodes of the vertical-selection switching devices **13**; horizontal switching devices (e.g., MOS transistors) **20** whose main electrodes are connected to the vertical signal lines **17** and horizontal signal lines **19**; a horizontal scanning circuit **21** connected to the control electrodes (so-called "gate electrodes") of the horizontal switching devices **20** and the read pulse lines **18**; and an amplifier **22** connected to the horizontal signal lines **19**.

In each unit pixel **14**, one main electrode of the read switching device **12** is connected to the photodiode **11**, and another main electrode of the switching device **12** is connected to each vertical signal line **17**. One main electrode of the vertical-selection switching device **13** is the control electrode (so-called "gate electrode") of the read switching device **12**, while another main electrode of the switching device **13** is connected to each read pulse line **18**, and the control electrode (so-called "gate electrode") is connected to each vertical selection line **15**.

From the horizontal scanning circuit **21**, horizontal scanning pulses ϕH [ϕH_1, . . . ϕH_n, ϕH_{n+1}, . . .] are supplied to the control electrodes (so-called "gate electrode") of the horizontal switching devices **20**, and horizontal read pulses ϕH^R [$\phi H^R{}_1$, . . . $\phi H^R{}_n$, $\phi H^R{}_{n+1}$, . . .] are supplied to the read pulse lines **18**.

The basic operation of the solid-state image-sensing device **10** is as follows.

The vertical-selection switching device **13** that receives vertical scanning pulse ϕV_m from the vertical scanning circuit **16** and the read pulse $\phi H^R{}_n$ from the horizontal scanning circuit **21** creates a pulse as the product of the pulses ϕV_m and $\phi H^R{}_n$, and uses the product pulse to control the control electrode of the read switching device **12**, whereby signal charge photoelectrically converted by the photodiode **11** is read via the vertical signal line **17**.

The signal charge is led in a horizontal period of the picture to the horizontal signal line **19** via the horizontal switching device **20** controlled by the horizontal scanning pulse ϕH_n from the horizontal scanning circuit **21**. The amplifier **22** converts the signal charge into a signal voltage, and outputs it.

The construction of the unit pixel **14** is not limited to that described above, but may be variously modified, such as those shown in FIGS. **2** and **3**.

In FIG. **2**, a unit pixel **14** includes a photodiode **11** and a read MOS transistor **12** connected thereto. One main electrode of the read MOS transistor **12** is connected to a vertical signal line **17**, and the gate electrode is connected to a vertical selection line **15**.

In FIG. **3**, a unit pixel **14** includes a photodiode **11**, a read MOS transistor **21**, a floating diffusion (FD) amplifying MOS transistor **22**, a FD reset MOS transistor **23**, and a vertical-selection MOS transistor **24**. One main electrode of the read MOS transistor **21** is connected to the photodiode **11**, and another main electrode of the transistor **21** is connected to one main electrode of the FD reset MOS transistor **23**. The FD amplifying MOS transistor **22** is connected between another main electrode of the FD reset MOS transistor **23** and one main electrode of the vertical-selection MOS transistor **24**. The gate electrode of the FD amplifying MOS transistor **22** is connected to a floating diffusion (FD) point at the midpoint of the read MOS transistor **21** and the FD reset MOS transistor **23**. The gate electrode of the read MOS transistor **21** is connected to a vertical-read line **25**. Another main electrode of the FD reset MOS transistor **23** is connected to a power supply VDD, and the gate electrode of the transistor **23** is connected to a horizontal-reset line **28**. Another main electrode of the vertical-selection MOS transistor **24** is connected to a vertical signal line **26**, and the gate electrode of the transistor **24** is connected to a vertical selection line **27**.

FIG. **4** shows a modification of the sensor **11** in the solid-state image-sensing device **10**.

A sensor (photodiode) **111** as the modification is formed by: forming a first semiconductor well region **32** of a first conductivity type, e.g., a p-type, on a silicon semiconductor substrate **31** of a second conductivity type, e.g., an n-type; forming a high-resistance semiconductor region, e.g., a low-concentration n-type semiconductor region **33**, on the first p-type semiconductor well region **32**; forming a second p-type semiconductor region **35** leading to the first p-type semiconductor well region **32**, beneath a device isolation layer (i.e., LOCOS layer) **34** resulting from local oxidation, which isolates the sensor **111** for each pixel; and forming a high-concentration n-type semiconductor region **36** on the surface of the low-concentration n-type semiconductor region **33** isolated by the device isolation layer **34** so that a pn-junction j is formed between the low-concentration n-type semiconductor region **33** and the first p-type semiconductor well region **32** and so that a depletion layer of the sensor part expands to the first p-type semiconductor well region **32** during operation.

The first p-type semiconductor well region **32** is formed at a predetermined depth of the substrate **31**, and the low-concentration n-type semiconductor region **33** is formed on the surface region of the substrate so as to be separated by the first p-type semiconductor well region **32**. The high-concentration n-type semiconductor region **36** acts as a substantial charge-accumulating region.

It is also possible to employ a sensor structure in which a high-concentration p-type semiconductor region **38** is formed at the interface between the high-concentration n-type semiconductor region **36** and an insulating film (e.g., SiO_2 film) **37**. In the sensor **111**, pn-junctions j are formed between the high-concentration n-type semiconductor region **36** and the high-concentration p-type semiconductor region **38** and between the low-concentration n-type semiconductor region **33** and the second p-type semiconductor well region **35**.

The second p-type semiconductor well region **35** can be simultaneously formed when, for example, a p-type semiconductor well of a CMOS transistor in a peripheral circuit is formed.

In the CMOS transistor, after a field insulating layer (so-called "device isolation layer) **52** is formed by local oxidation, as shown in FIGS. **13**A to **13**C, a p-type semiconductor well region **55** is formed (see FIG. **13**A) by performing ion implantation of a p-type impurity **54** such as boron in one device forming region, using a photoresist layer **53** as a mask.

Next, gate electrodes **57** composed of, for example, polycrystal silicon, are formed on the p-type semiconductor well region **55** and the n-type semiconductor substrate **51** as another device forming region (see FIG. **13**B), while providing gate insulating films **56** therebetween.

Next, by using each gate electrode **57** as a mask, and performing self-aligning, ion implantation of an n-type impurity is performed in the p-type semiconductor well

region **55** to form an n-type source region **58**S and a drain region **58**D so that an n-channel MOS transistor **59** is formed, and ion implantation of a p-type impurity is performed in the n-type semiconductor substrate **51** to form a p-type source region **61**S and a drain region **61**D so that a p-channel MOS transistor **62** is formed, whereby a CMOS transistor is obtained.

A process in which the p-type semiconductor well region **55** is formed after forming the field insulating layer **52** is called a "retrograde p-well process".

The above-described second p-type semiconductor well region **35** in FIG. **4** can be formed simultaneously with the p-type semiconductor well region **55** in FIG. **13**. Thus, the sensor **111**, in which the expansion of a depletion layer described below is deepened to increase a photoelectric conversion efficiency, can be formed without increasing the number of producing steps.

In addition, the second p-type semiconductor well region **35** is formed after forming the device isolation layer **34**, as shown in FIG. **4**. Thus, the second p-type semiconductor well region **35** can be selectively formed beneath the device isolation layer **34** excluding the sensor-formed region without being affected by diffusion due to thermal processing performed during the formation of the device isolation layer.

According to the solid-state image-sensing device **10** having the sensors **111** in this embodiment, by selectively forming, beneath only the device isolation layer **34** excluding the sensor region, the second p-type semiconductor well region **35** leading to the first p-type semiconductor well region **32**, and forming pn-junctions with the high-concentration n-type semiconductor region **36**, the low-concentration n-type semiconductor region **33**, and the first p-type semiconductor well region **32**, photodiodes, that is, sensors **111** are formed, whereby the expansion of the depletion layer in each sensor **111** is deepened during operation, and even signal charge photoelectrically converted at a deep position can be accumulated in the high-concentration n-type semiconductor region **36** as a charge accumulating region. Therefore, the photoelectric conversion efficiency increases, making it possible to obtain a solid-state image-sensing device with higher sensitivity.

FIG. **5** shows another embodiment of the sensor **11** (see FIG. **1**) according to the present invention.

A sensor (photodiode) **112** according to this embodiment is intended to increase photoelectric conversion efficiency and to reduce a dark current due to leakage current.

The sensor **112** is formed, similarly to the foregoing description, by: forming a first semiconductor well region **32** of a first conductivity type, e.g., a p-type, on a semiconductor substrate **31** of a second conductivity type, e.g., an n-type; forming a low-concentration n-type semiconductor region **33** on the first p-type semiconductor well region **32**; forming a high-concentration n-type semiconductor region **36** on the surface of the low-concentration n-type semiconductor region **33**, in which pixel isolation is performed by a device isolation layer **34** resulting from local oxidation; and forming a pn-junction j between the low-concentration n-type semiconductor region **33** and the first p-type semiconductor well region **32** so that a depletion layer of the sensor expands to the first p-type semiconductor well region **32** during operation.

In this embodiment, in particular, a second p-type semiconductor well region **351** leading to the first p-type semiconductor well region **32** is formed beneath the device isolation layer **34** for pixel isolation, and part **351***a* of the second p-type semiconductor well region **351** is simultaneously provided being extended between the n-type semiconductor region **36** and the device isolation layer **34**, in which a substantial charge accumulating region of the sensor is formed therebetween.

In other words, an end of the second p-type semiconductor well region **351** is formed so as to be positioned on the sensor side apart from an end of the device isolation layer **34**, and an end of the n-type semiconductor region **36** as the charge accumulating region of the sensor **112** is provided so as to touch an extended portion of the second p-type semiconductor well region **351***a*. In the sensor **112**, a pn-junctions j is also formed between each n-type semiconductor region **33** or **36** and the extended portion of the p-type semiconductor well region **351***a*.

FIGS. **7**A to **7**C show a method for producing the sensor **112**.

Initially, as shown in FIG. **7**A, after forming a device isolation layer **34** used for local oxidation on the surface of an n-type semiconductor substrate **31**, a predetermined pattern photoresist layer **41** in which a photoresist end **41***a* is positioned on the sensor side (in the active region of a photodiode) apart from an end of the device isolation layer **34** is formed so as to cover a region for forming the sensor part of the substrate **31**. The photoresist layer **41** is used as a mask to perform ion implantation of a p-type impurity **42**, whereby a second p-type semiconductor well region **351** is formed. The second p-type semiconductor well region **351** is formed so that an end thereof, namely, an end of the extended portion **351***a* is positioned on the side for forming the sensor part, which is apart from an end of the device isolation layer **34**.

Next, as shown in FIG. **7**B, after removing the photoresist layer **43**, by performing ion implantation of a p-type impurity **43** in the entire region for forming the sensor part, which includes the part beneath the device isolation layer **34**, a first p-type semiconductor well region **32** touching the lower part of the second p-type semiconductor well region **351** is formed at a predetermined depth of the substrate **31**. By forming the first p-type semiconductor well region **32**, a low-concentration n-type semiconductor region **33** including an isolated portion of the substrate **31** is formed in a region surrounded by the first p-type semiconductor well region **32** and the second p-type semiconductor well region **351**.

Next, as shown in FIG. **7**C, by forming a photoresist layer **44** in a part excluding the sensor forming region, and performing ion implantation of an n-type impurity **45**, a high-concentration n-type semiconductor region **36** to be used as a charge accumulating region is formed on the surface of the low-concentration n-type semiconductor region **33**. This forms pn-junctions j between the n-type semiconductor region **33** and the first semiconductor well region **32**, and between each n-type semiconductor region **36** or **33** and the extended portion **351***a* of the second p-type semiconductor well region, whereby the desired photodiode, namely, the sensor **112** is formed.

The impurity concentrations of the regions are as follows:

second semiconductor well region **351**>n-type semiconductor region **36**; and

n-type semiconductor region **36**>n-type semiconductor region **33**.

According to a solid-state image-sensing device provided with the above-described sensor **112**, by forming the second p-type semiconductor well region (so-called "channel stop region") **351** so as to be extended to the sensor side than to the end of the device isolation layer **34**, the pn-junctions of

the photodiode forming the sensor **112** can be isolated from an end of the device isolation layer **34** having crystal defects such as dislocation, in other words, from a semiconductor region in the vicinity of the device isolation layer **34**, whereby, when the pn-junctions are reverse biased, the depletion layer can be generated apart from the end of the device isolation layer **34**.

Accordingly, the generation of a leakage current in the vicinity of the device isolation layer **34** is suppressed, and the dark current decreases.

Similarly to FIG. **4**, in the sensor **112**, the regions **36** and **33** form one n-type semiconductor region constituting the photodiode in connection with the second semiconductor well region **351**, so that the expansion of the depletion layer is deepened and the photoelectric conversion efficiency can be increased.

According to the producing method shown in FIGS. **7**A to **7**C, ion implantation is used to form the second p-type semiconductor well region **351** after forming the device isolation layer **34**. Thus, there is no influence of thermal processing in the formation of the device isolation layer **34**. In other words, the second p-type semiconductor well region **351** can be formed with positional precision without being re-diffused.

Also when forming the second p-type semiconductor well region **351** having the extended portion **351***a*on the sensor side apart from the end of the device isolation layer **34**, its alignment with the device isolation layer **34** is facilitated. Accordingly, the second p-type semiconductor well region **351** can be easily and accurately formed. In addition, in this embodiment, the second p-type semiconductor well region **351** can be simultaneously formed, together with the p-type well region **55** in the production of the peripheral circuit's CMOS transistor shown in the above-described FIGS. **13**A to **13**C. Thus, there is no increase in the number of production steps.

FIG. **6** shows another embodiment of the sensor **11** (see FIG. **1**) according to the present invention.

A sensor (photodiode) **113** according to this embodiment is formed such that, in the above-described sensor structure shown in FIG. **5**, a high-concentration p-type semiconductor region **38** is formed between an n-type semiconductor region **36** to be used as a charge accumulating region and a top insulating film **37** so as to touch a second p-type semiconductor well region **351**. Other components are identical to those in FIG. **5**. Accordingly, the corresponding components are denoted by identical reference numerals, and repeated descriptions are omitted.

The sensor **113** can be produced such that, after using ion implantation to form the n-type semiconductor region **36** shown in FIG. **7**C, a p-type semiconductor region **38** is formed on the surface of the n-type semiconductor region **36** by performing ion implantation of a p-type impurity **46**, as shown in FIG. **7**D.

According to a solid-state image-sensing device provided with the sensor **113** according to this embodiment, by employing a structure having a p-type semiconductor region **38** on the surface of the n-type semiconductor region **36**, all pn-junctions other than that in the gate of a read MOS transistor (not shown) can be provided in the bulk. In other words, in the sensor **113**, in addition to effects in the sensor **112** in FIG. **5**, the dark current can be more reduced because the depletion layer is positioned apart from an interface with the sensor top insulating film **37**, i.e., an $Si\text{-}SiO_2$ interface.

FIG. **8** shows another embodiment of the sensor **11** (see FIG. **1**) according to the present invention.

A sensor (photodiode) **114** according to this embodiment is formed, similarly to the foregoing description, by: forming a first semiconductor well region **32** of a first conductivity type, e.g., a p-type, on a semiconductor substrate **31** of a second conductivity type, e.g., an n-type; forming a low-concentration n-type semiconductor region **33** on the first p-type semiconductor well region **32**; forming a high-concentration n-type semiconductor region **36** on the surface of the low-concentration n-type semiconductor region **33**, in which pixel isolation is performed by a device isolation layer **34** resulting from local oxidation; and forming a pn-junction j between the low-concentration n-type semiconductor region **33** and the first p-type semiconductor well region **32** so that a depletion layer of the sensor expands to the first p-type semiconductor well region **32** during operation.

In this embodiment, in particular, a second p-type semiconductor well region **352** that has an end **352***a* at an inner position than an end of the device isolation layer **34** and that leads to a first p-type semiconductor well region **32** is formed beneath a device isolation layer **34** for pixel isolation, and a p-type semiconductor region, i.e., a so-called "p-type plug region **39**" is formed between an end of the device isolation layer **34** and an n-type semiconductor region **36** to be used as a charge accumulating region. The p-type plug region **39** is formed so as to be connected to the second p-type semiconductor well region **352**.

In addition, in FIG. **8**, a high-concentration p-type semiconductor region **38** is formed on the surface of the n-type semiconductor region **36** so as to partially touch the p-type plug region **39**. In the sensor **114**, pn-junctions j are formed among each n-type semiconductor region **36** or **33**, the p-type semiconductor region **38**, the second p-type semiconductor well region **352**, and the p-type plug region **39**.

FIGS. **9**A to **9**E show a method for producing the sensor **114**.

Initially, as shown in FIG. **9**A, after forming, on the surface of an n-type semiconductor substrate **31**, a device isolation layer **34** resulting from local oxidation, a predetermined pattern photoresist layer **64** that covers a region for forming a sensor and that has an end **64***a* on the device isolation layer **34** is formed, and the photoresist layer **64** is used as a mask to perform ion implantation of a p-type impurity **42**, whereby a second p-type semiconductor well region **352**. The second p-type semiconductor well region **352** is formed so that its end **352***a* is positioned to be inner than the end of the device isolation layer **34**. The second p-type semiconductor well region **352** is simultaneously formed in a process where the p-type semiconductor well region **55** in the peripheral circuit's CMOS transistor is formed as described above.

Next, as shown in FIG. **9**B, after removing the photoresist layer **64**, a first p-type semiconductor well region **32** touching the lower part of the second p-type semiconductor well region **352** is formed at a predetermined depth of the substrate **31** by performing ion implantation of a p-type impurity on the entire region for forming the sensor part, which includes the lower part of the device isolation layer **34**. By forming the first p-type semiconductor well region **32**, a low-concentration n-type semiconductor region **33** including an isolated portion of the substrate **31** is formed in a region surrounded by the first p-type semiconductor well region **32** and the second p-type semiconductor well region **352**.

Next, as shown in FIG. **9**C, a predetermined pattern photoresist layer **65** that covers the region for forming the sensor part and that has an end **65***a* is positioned on the sensor side (in the active region of a photodiode) apart from the end of the device isolation layer **34** is formed. By

masking the photoresist layer **65**, and performing ion implantation of a p-type impurity **66**, a p-type plug region **39** is formed. The p-type plug region **39** is formed so that an end thereof is positioned on the sensor part forming region apart from the end of the device isolation layer **34**. In other words, it is formed so as to extend from the end of the device isolation layer **34**.

Next, as shown in FIG. **9**D, by forming photoresist layer **44** on a part other than the sensor part forming region, and performing ion implantation of an n-type impurity, a high-concentration n-type semiconductor region **36** to be used as a charge accumulating region is formed on the surface of the low-concentration n-type semiconductor region **33**.

Subsequently, as shown in FIG. **9**E, by performing ion implantation of a p-type impurity **46**, a high-concentration p-type semiconductor region **38** is formed on the surface of the n-type semiconductor region **36** so as to touch the p-type plug region **39**. With the above-described process, the desired photodiode, in which main pn-junctions are formed by each n-type semiconductor region **36** or **33** and the first p-type semiconductor well region **32**, in other words, the sensor **114** is obtained.

In this construction, the impurity concentrations of the regions are as follows:

p-type semiconductor region **38**>n-type semiconductor region **36**;

p-type semiconductor well region **352**>n-type semiconductor region **33**; and

p-type plug region **39**>n-type semiconductor region **36**.

According to a solid-state image-sensing device provided with the sensor **114** according to this embodiment, by forming the p-type plug region (used as a channel stop region) **39** between the end of the device isolation layer **34** resulting from local oxidation and the n-type semiconductor region **36** to be used as the charge accumulating region of the sensor **114**, pn-junctions of the photodiode forming the sensor **114** can be isolated from the end of the device isolation layer **34** which has crystal defects such as dislocation, i.e., the semiconductor region in the vicinity of the end of the device isolation layer **34**, whereby, when the pn-junctions are reverse biased, the depletion layer can be generated at a position apart from the device isolation layer **34**. Accordingly, the generation of a leakage current in the vicinity of the end of the device isolation layer **34** can be suppressed, and a dark current can be reduced. Simultaneously, the expansion of the depletion layer is deepened as described above, whereby the photoelectric conversion efficiency can be increased.

In addition, when a structure is employed in which the second p-type semiconductor well region **352** is formed to be inner than the device isolation layer **34** and in which the p-type plug region **39** is formed between the end of the device isolation layer **34** and the n-type semiconductor region **36** of the sensor **114**, the distance between the gate end of the read MOS transistor and the end of the p-type plug region **39** can be more accurately set.

In other words, the sensor structure in FIG. **8** and the sensor structure in FIG. **6** are compared.

When it is assumed that each of the sectional structure of the sensor **114** in FIG. **8** and the sectional structure of the sensor **113** in FIG. **6** is the sectional structure on line VI,VIII—VI,VIII of a plan view showing a main part of an image capturing region in FIG. **10**A, the sectional structure on line XII,XIII—XII,XIII crossing a gate electrode **71** of a read MOS transistor in FIG. **11** is as shown in FIG. **11** for the sensor **114**, and is as shown in FIG. **12** for the sensor **113**. FIG. **10**B, is an equivalent circuit of the unit pixel in FIG. **10**A. In the plan view in FIG. **10**A, there are a hatched part indicating the device isolation layer **34** resulting from local oxidation and an end **34***a* of the device isolation layer. The inversely hatched part indicates the extended portion **351***a* of the second p-type semiconductor well region **351** or the p-type plug region **39**. A read MOS transistor **12** has an L-shaped read gate electrode **71**. A vertical-selection MOS transistor **13** has a gate electrode connected to a vertical selecting line **15**. A vertical signal line **17** and one source-drain region **73** constituting the read MOS transistor **12** are connected by a contact portion **171**, and the gate electrode **71** is connected to one source-drain region of the vertical selecting MOS transistor **13** via a wire (e.g., Al wire), which is not shown, and contact portions **172** and **173**. Another source-drain region of the vertical selecting MOS transistor **13** is connected to a pulse line **18** via a contact portion **174**.

In the sectional structures in FIGS. **11** and **12**, a low-concentration p-type impurity is doped into a channel region **72** beneath a gate electrode **71** constituting the read MOS transistor **12**. Each structure includes a gate insulating film **77** composed of SiO_2, etc., and sidewalls **74** composed of SiO_2, etc.

In the case of the structure of the sensor **112**, an ion implantation process in which no shape is left, in other words, a process of ion implantation in the second p-type semiconductor well region **351**, is performed earlier, as shown in FIG. **12**. Thus, the second p-type semiconductor well region **351** and the gate electrode **71** are respectively formed with the second p-type semiconductor well region **351** aligned with the device isolation layer **34**, and the gate electrode **71** aligned with the device isolation layer **34**. Accordingly, the second p-type semiconductor well region **351** and the gate electrode **71** cannot be directly aligned with each other.

In other words, as shown in FIG. **12**, alignment in the formation of the second p-type semiconductor well region **351** and the gate electrode **71** is performed using, as a reference point p, an end of the device isolation layer **34** left as a shape. Thus, variations occur in respective distances d_1 and d_2, and the precision of the distance D_1 between the gate electrode **71** and the second p-type semiconductor well region **351**, which requires precision, decreases, so that characteristic variation between lots may increase.

Conversely, in the case of the sensor **114**, as shown in FIG. **11**, after forming a read gate electrode **71**, a p-type plug region **39** is formed by performing ion implantation, while using an end of the gate electrode **71** as a reference. Thus, alignment precision between the gate electrode **71** and the p-type plug region **39** is increased to increase the precision of the distance D_2 between the gate electrode **71** and the p-type plug region **39**. This can expand the opening area of the sensor part, reducing the alignment margin. Also, variation between lots can be reduced.

In the structure of the sensor **114** in FIGS. **8** and **11**, the dark current is intended to be further reduced by forming the p-type semiconductor region **38** on the surface of the n-type semiconductor region **36**, and providing, in the bulk, all pn-junctions in portions excluding the gate end. Otherwise, a structure in which the p-type semiconductor region **38** is omitted can be employed.

FIG. **14** shows still another embodiment of the sensor **11** (see FIG. **1**) according to the present invention.

A sensor **115** is formed by: forming a device isolation layer **34** resulting from local oxidation after forming a p-type semiconductor well region **31** of a first conductivity type, e.g., a p-type, on a semiconductor substrate of a second conductivity type, e.g., an n-type; forming, in the device

isolation region, an n-type semiconductor region **82** to be used as a charge accumulating region; forming a pn-junction between the n-type semiconductor region **82** and the p-type semiconductor well region **81** so that a photodiode is formed; and forming a p-type plug region **39** between the n-type semiconductor region **82** and an end of the device isolation layer **34**.

The sensor **115** has a structure in which the p-type plug region **39** is added to the structure in FIG. **15**.

Also in a solid-state image-sensing device provided with the above-described sensor **115**, by forming the p-type plug region **39** between the n-type semiconductor region **82** and the device isolation layer **34**, the leakage current at the end of the device isolation layer **34** can be suppressed, and the dark current can be reduced.

Each of the above-described embodiments describes a case in which the insulating layer resulting from local oxidation is used as a device isolation layer for a solid-state image-sensing device.

The present invention may be applied to a solid-state image-sensing device using, as its device isolation layer, a device isolation layer resulting from trench isolation, so-called called "STI (shallow trench isolation)". Trench device isolation enables micro-fabrication and high integration of pixels, compared with device isolation resulting from local oxidation.

Next, using FIGS. **15** to **17**, an embodiment applied to a solid-state image-sensing device using trench device isolation is described.

FIG. **15** shows another embodiment of the sensor **11** in the above-described solid-state image-sensing device **10**.

A sensor (photodiode) **116** is formed by forming, in a semiconductor substrate **31** of a second conductivity type, e.g., an n-type, a trench device isolation layer **93** composed of a trench **91** for pixel isolation and an insulating layer **92** such as SiO_2, which is embedded in the trench **91**, and sequentially forming, as described above, a first p-type semiconductor well region **32**, a low-concentration n-type semiconductor region **33** thereon, an n-type semiconductor region **36** thereon to be used as a charge accumulating region, and a high-concentration p-type semiconductor region **38** between the surface of the region **36** and an insulating film **37**, in a pixel region on the n-type semiconductor substrate **31**.

In this embodiment, in particular, a second p-type semiconductor well region **94** leading to the first p-type semiconductor well region **32** is formed excluding the side of the sensor **116**, and a portion of the second p-type semiconductor well region **94** is extended projecting on the pixel region side of the sensor **116** so as to surround the interfaces of the trench **91** of the trench device isolation region **93** for pixel isolation.

In this embodiment, the trench **91** is formed at approximately a depth reaching the low-concentration n-type semiconductor well region **33**. The first p-type semiconductor well region **32** is formed so as to end at a portion corresponding to the bottom of the trench device isolation layer **93** in the second p-type semiconductor well region **94**. The second p-type semiconductor well region **94** is formed so that each portion is at a uniform depth, with the trench **93** formed.

FIG. **16** shows another embodiment of the sensor **11** (see FIG. **1**) according to the present invention.

A sensor (photodiode) **117** according to this embodiment is similarly formed as described above by forming, in a semiconductor substrate **31** of a second conductivity type, e.g., an n-type, a trench device isolation layer **93** composed of a trench **91** for pixel isolation and an insulating layer **92** such as SiO_2, which is embedded in the trench **91**, and sequentially forming a first p-type semiconductor well region **32**, a low-concentration n-type semiconductor region **33** thereon, an n-type semiconductor region **36** thereon to be used as a charge accumulating region, and a high-concentration p-type semiconductor region **38** between the surface of the region **36** and an insulating film **37**, in a pixel region on the n-type semiconductor substrate **31**.

In this embodiment, in particular, a second p-type semiconductor well region **94** leading to the first p-type semiconductor well region **32** is formed excluding the side of the sensor **116**, and a portion of the second p-type semiconductor well region **94** is extended projecting on the pixel region side of the sensor **117** so as to surround the interfaces of the trench **91** of the trench device isolation layer **93**.

In this embodiment, the first p-type semiconductor well region **32** is formed overall, and the trench **91** of the trench device isolation layer **93** is formed so as to lead to the first p-type semiconductor well region **32**. Concerning the trench **91**, its bottom and side are surrounded by the first and second p-type semiconductor well regions **32** and **94**.

FIG. **17** shows another embodiment of the sensor **11** (see FIG. **1**) according to the present invention.

A sensor (photodiode) **118** according to this embodiment is similarly formed as described above by: forming, in a semiconductor substrate **31** of a second conductivity type, e.g., an n-type, a trench device isolation layer **93** composed of a trench **91** for pixel isolation and an insulating layer **92** such as SiO_2, which is embedded in the trench **91**; forming a high-concentration p-type plug region **95** at the interfaces of the trench **91**; and sequentially forming a first p-type semiconductor well region **32**, a low-concentration n-type semiconductor region **33** thereon, an n-type semiconductor region **36** thereon to be used as a charge accumulating region, and a high-concentration p-type semiconductor region **38** between the surface of the region **36** and an insulating film **37**, in a pixel region on the n-type semiconductor substrate **31**. The high-concentration p-type plug region **95** covers all the trench's interfaces between the insulating layer **92** and silicon (Si).

In this embodiment, in particular, a second p-type semiconductor well region **94** leading to the first p-type semiconductor well region **32** is formed excluding the side of the sensor **118**, and a portion of the second p-type semiconductor well region **94** is extended projecting on the pixel region side of the sensor **117** so as to surround the interfaces of the trench **91** of the trench device isolation layer **93**.

In this embodiment, the trench **91** is formed leading to the n-type semiconductor substrate **31**, and the first p-type semiconductor well region **32** is formed overall. The trench **91** has a side overall surrounded by the first and second p-type semiconductor well regions **32** and **94**.

FIGS. **18**A to **20**C show producing methods for realizing the above-described sensors **116**, **117**, and **118**.

The production example in FIGS. **18**A and **18**B is described below.

Initially, as shown in FIG. **18**A, an insulating film **37** composed of, for example, SiO_2 is formed on an n-type semiconductor substrate **31**, and a trench **91** for trench isolation is formed on the semiconductor substrate **31**, together with the insulating film **37**. Next, an active region isolated at distance d_1 from an edge of the trench **91**, in other words, a resist mask **97**, is formed, and by performing ion implantation of a p-type impurity via the resist mask **97**, a second p-type semiconductor well region **94** is formed on the semiconductor substrate **31** so as to project into the pixel region side.

At this time, the second p-type semiconductor well region **94** is formed around the sides and bottom of the trench **91** so as to have sufficient width and depth.

Next, as shown in FIG. **18**B, by using chemical vapor deposition (CVD) to embed an insulating film, for example, an SiO_2 film **92**, in the trench **91**, and planarize it, a trench device isolation layer **93** consisting of the trench **91** and the embedded insulating film **92** is formed.

After that, excluding the pixel region, a resist mask **99** is formed so that an end thereof is positioned on the trench device isolation layer **93**. By performing selective ion implantation of p-type and n-type impurities into the pixel region via the resist mask **99**, a first p-type semiconductor well region **32** connected to a second p-type semiconductor well region **94** is formed at a deep position of the substrate **31**, an n-type semiconductor well region **36** to be used as a charge accumulating region is formed on the surface of the substrate **31**, and a high-concentration p-type semiconductor region **38** is formed at the interface between the n-type semiconductor region **36** and the insulating film **37** so as to be connected to the second p-type semiconductor well region **94**.

A portion of the substrate **31** between the top n-type semiconductor region **36** and the p-type semiconductor well region **32** is used as a low-concentration n-type semiconductor region **33**.

Ion implantation for the first p-type semiconductor well region **32**, the n-type semiconductor region **36**, and the high-concentration p-type semiconductor region **38** is shown by one illustration. However, it may be different processes for convenience of forming other portions.

With this process, the desired sensor is formed. This sensor is formed as a so-called "hole accumulation diode (HAD)" sensor by the high-concentration p-type semiconductor region **38**, the n-type semiconductor regions **36** and **33**, and the first p-type semiconductor well region **32**.

The production example in FIGS. **19**A to **19**C is described.

At first, as shown in FIG. **19**A, an insulating film **37** composed of, for example, SiO_2, is formed on the surface of the n-type semiconductor region **31**, and a trench **91** for trench isolation is formed in the semiconductor region **31**, together with the insulating film **37**.

Next, excluding the trench **91** and a portion isolated by predetermined distance d_2 from ends of the trench **91**, a resist mask **101** is formed on the entire surface of the other portions. By performing ion implantation of a p-type impurity via the resist mask **101**, a high-concentration p-type semiconductor layer for connecting a first p-type semiconductor well region **32** and a second p-type semiconductor well region **32**, in other words, a so-called "p-type semiconductor plug layer" **95**, is formed.

The p-type semiconductor plug layer **95** is formed around the sides and bottom of the trench **91** so as to cover the trench **91**.

Next, as shown in FIG. **19**B, by using chemical vapor deposition (CVD) to embed an insulating film, for example, an SiO_2 film **92** in the trench **91**, and planarizing it, a trench device isolation layer **93** consisting of the trench **91** and the embedded insulating film **92** is formed.

Subsequently, a resist mask **103** is formed so that an end thereof is positioned on the trench device isolation layer **93**, excluding the pixel region. By performing selective ion implantation of p-type and n-type impurities via the resist mask **103**, a first p-type semiconductor well region **32** connected to the p-type plug region **95** is formed at a deep position of the substrate **31**, a n-type semiconductor region **36** to be used as a charge accumulating region is formed on the surface of the substrate **31**, and a high-concentration p-type semiconductor region **38** connected to the p-type plug region **95** is formed at the interface of the n-type semiconductor region **36** with the insulating film **37**.

A portion of the substrate **31** between the top n-type semiconductor region **36** and the p-type semiconductor well region **32** is used as a low-concentration n-type semiconductor region **33**.

Ion implantation for the first p-type semiconductor well region **32**, the n-type semiconductor region **36**, and the high-concentration p-type semiconductor region **38** is shown by one illustration. However, it may be different processes for convenience of forming other portions.

Next, as shown in FIG. **19**C, a resist mask **104** is formed in the pixel region so as to be isolated by predetermined distance d_1 across the p-type plug region **95** from an end of the trench **91** of the trench device isolation layer **93**. By performing ion implantation of a p-type impurity via the resist mask **104**, a second p-type semiconductor well region **94** is formed so that part thereof extends from the trench device isolation layer **93** to the pixel region.

The first p-type semiconductor well region **32** and the second p-type semiconductor well region **94** are connected by the p-type plug region **95**.

With this process, the desired sensor is formed.

The production example in FIGS. **20**A to **20**C is described.

At first, as shown in FIG. **20**A, an insulating film **37** composed of, for example, SiO_2, etc., is formed on the surface of an n-type semiconductor substrate **31**, and a trench **92** for trench isolation is formed on the semiconductor substrate **31**, together with the insulating film **37**. Next, by using chemical vapor deposition (CVD) to embed an insulating film, for example, an SiO_2 film **92** in the trench **91**, and planarizing it, a trench device isolation layer **93** consisting of the trench **91** and the embedded insulating film **92** is formed.

Subsequently, excluding the pixel region isolated by the trench device isolation layer **93**, a resist mask **105** is formed. By performing selective ion implantation via the resist mask **105**, an n-type semiconductor region **38** to be used as a charge accumulating region is formed on the surface of the substrate **31**, and a high-concentration p-type semiconductor region **38** is formed on the surface of the p-type semiconductor region **38**.

Although ion implantation for the n-type semiconductor region **36** and the high-concentration p-type semiconductor region **38** is shown by one illustration, it may be different processes for convenience of forming the other portions.

Next, as shown in FIG. **20**B, a resist mask **106** is formed in the pixel region so as to be isolated by distance d_1 from an end of the trench **91** of the trench device isolation layer **93**. By performing ion implantation of a p-type impurity via the resist mask **106**, a second p-type semiconductor well region **94** is formed so that part thereof extends from the trench device isolation layer **93** to the pixel region.

Next, as shown in FIG. **20**C, by performing overall ion implantation of a p-type impurity, a first p-type semiconductor well region **32** connected to the bottom of the second p-type semiconductor well region **94** is formed at a deep position of the substrate **31**. A portion of the substrate **31** between the top n-type semiconductor region **36** and the first p-type semiconductor well region **32** is used as a low-concentration n-type semiconductor region **33**.

With this process, the desired sensor is formed.

The above-described sensor **116** in FIG. **15** can be produced in accordance with, for example, the production

example in FIGS. **19**A and **19**B and the production example in FIGS. **20**A to **20**C. In other words, when the bottom of the second p-type semiconductor well region **94** is shallower than the first p-type semiconductor well region **32**, and a portion therebetween is an n^- semiconductor region **33**, production can be enabled by employing ion implantation in FIGS. **19**A and **19**B in order to connect the first and second p-type semiconductor regions **32** and **94**, and by employing plug ion implantation in FIGS. **20**A to **20**C.

The above-described sensor **117** in FIG. **16** can be produced in accordance with, for example, the production example in FIGS. **20**A to **20**C.

The above-described sensor **118** in FIG. **18** can be produced in accordance with, for example, the production example in FIGS. **19**A to **19**C.

According to a solid-state image-sensing device provided with the above-described sensors **116**, **117**, and **118**, the p-type semiconductor region **94** or the p-type semiconductor regions **94** and **95** are formed so as to extend from the trench device isolation layer **93** to the n-type semiconductor regions **33** and **36** of the sensor. In other words, the semiconductor interface with the trench device isolation layer **93** isolating the sensor **116**, **117**, or **118**, is surrounded by a p-type semiconductor region, for example, the second p-type semiconductor well region **94**, the first and second semiconductor well regions **32** and **94**, or the p-type plug region **95** and the second p-type semiconductor well region **94**, etc.

In the semiconductor interface with the trench device isolation layer **93**, there are crystal defects such as dislocation. This interface having crystal defects is incorporated into a p-type semiconductor region of a conductivity type opposite to the conductivity type of the n-type semiconductor region **36** as a charge accumulating region of the sensor.

With this construction, the photodiode's pn-junction forming the sensor **116**, **117**, or **118** can be isolated from the interface of the trench device isolation layer **93** having crystal defects such as dislocation, and when the pn-junction is reverse biased, depletion in the interface of the trench device isolation layer **93** and its vicinity can be prevented.

Therefore, the generation of leakage current from the interface and its vicinity can be suppressed, and dark current can be reduced.

When the sensor part is formed as a HAD sensor in which the p-type semiconductor region **38** is formed on the surface of the n-type semiconductor region, all pn-junctions are provided in the bulk, excluding those in the gate end, so that the dark current can be further reduced.

In the foregoing embodiments, cases in which the present invention is applied to a CMOS solid-state image-sensing device. However, the present invention may be applied to a MOS solid-state image-sensing device.

What is claimed is:

1. A solid-state image-sensing device having pn-junction sensor parts isolated corresponding to pixels by a device isolation layer, said solid-state image-sensing device comprising

a first-conductivity-type second semiconductor well region formed between a first-conductivity-type first semiconductor well region and said device isolation layer,

wherein, when the device is operating, a depletion layer of each sensor part spreads to the first semiconductor well region, which is beneath each of said sensor parts.

2. A solid-state image-sensing device according to claim **1**, wherein the second semiconductor well region is simultaneously formed with the semiconductor well regions formed after the formation of said device isolation layer in a complementary-metal-oxide-semiconductor transistor.

3. A solid-state image-sensing device having pn-junction sensor parts isolated corresponding to pixels by a device isolation layer resulting from local oxidation, said solid-state image-sensing device comprising a semiconductor region of a conductivity type opposite to the conductivity type of a charge accumulating region of each of the sensor parts, the semiconductor region formed between the charge accumulating region of each sensor part and said device isolation layer.

4. A solid-state image-sensing device according to claim **3**, further comprising

a second semiconductor well region formed between said device isolation layer and a first semiconductor well region beneath said device isolation layer,

wherein, when the device is operating, the depletion layer of each of said sensor parts spreads to said first semiconductor well region, which is beneath each of said sensor parts.

5. A solid-state image-sensing device according to claim **3**, wherein the semiconductor region is formed by extending a portion of a second semiconductor well region formed between said device isolation layer and a first semiconductor well region beneath said device isolation layer.

6. A solid-state image-sensing device including pn-junction sensor parts isolated corresponding to pixels by a device isolation layer resulting from trench isolation, said solid-state image-sensing device comprising

a semiconductor region of a conductivity type opposite to the conductivity type of the charge accumulating region of each of said sensor parts, said semiconductor region formed to extend from said device isolation layer to a pixel region.

7. A solid-state image-sensing device according to claim **6**, wherein the opposite-conductivity-type semiconductor region is formed by extending a portion of a semiconductor well region.

* * * * *

EXHIBIT F

US007138617B2

(12) **United States Patent**
Mabuchi

(10) **Patent No.: US 7,138,617 B2**
(45) **Date of Patent: Nov. 21, 2006**

(54) **SOLID-STATE IMAGE PICKUP DEVICE AND OUTPUT METHOD THEREOF**

(75) Inventor: **Keiji Mabuchi**, Kanagawa (JP)

(73) Assignee: **Sony Corporation** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/355,065**

(22) Filed: **Jan. 31, 2003**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
H01L 27/00 (2006.01)
H04N 5/217 (2006.01)
H04N 3/14 (2006.01)

(52) **U.S. Cl.** ..... **250/208.1**; 250/214 R; 250/214.1; 348/222.1; 348/241; 348/250; 348/294; 348/312; 348/317

(58) **Field of Classification Search** ..... 250/208.1, 250/214 DC, 214 A, 214.1, 214 D, 214 R; 348/241, 242, 245, 257, 312, 317, 222.1, 348/294, 308, 310
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,072,366 A * 6/2000 Maeda et al. ..... 250/214 A
6,353,488 B1 * 3/2002 Hieda et al. 348/207.99
6,822,211 B1 * 11/2004 Hagihara 250/208.1
6,881,942 B1 * 4/2005 Huang et al. 324/309

* cited by examiner

Primary Examiner—Stephone B. Allen
Assistant Examiner—Davienne Monbleau
(74) *Attorney, Agent, or Firm*—Rader, Fishman & Grauer PLLC; Ronald P. Kananen

(57) **ABSTRACT**

A solid-state image pickup device has a differential output configuration for an output stage thereof and an IC in a next stage has a differential amplifier configuration for an input stage thereof. An output buffer unit buffers and outputs a digital signal from a horizontal bus line. At this time, in addition to the normal video signal, the output buffer unit generates an inverted output of the normal video signal. The normal video signal and the inverted output are outputted from a video signal output terminal and an inverted video signal output terminal, respectively, to the outside of a chip. Further, a clock, which is supplied from a timing generator to the output buffer unit, is also buffered and outputted to the outside together with an inverted clock A differential amplifier is used in an input stage of an IC in a next stage, whereby even signals having blunter waveforms can be recognized. This enables increase in speed of the system, addition of capacitance to signal paths, or reduction in size of the output buffer unit of the solid-state image pickup device.

14 Claims, 8 Drawing Sheets

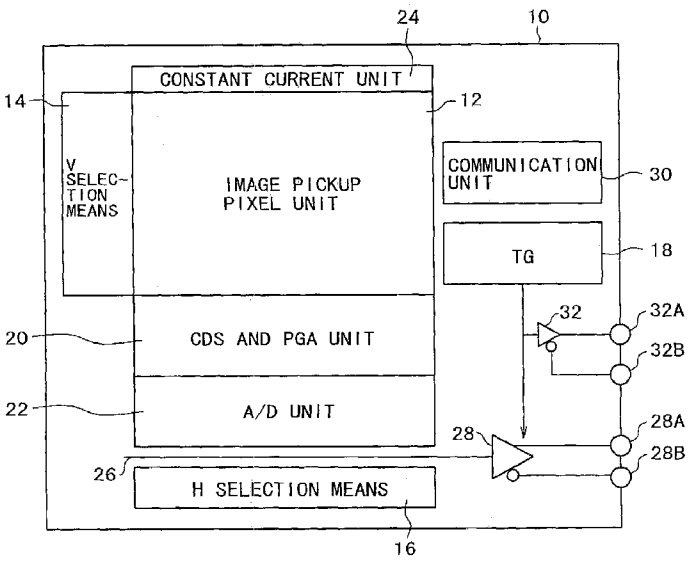
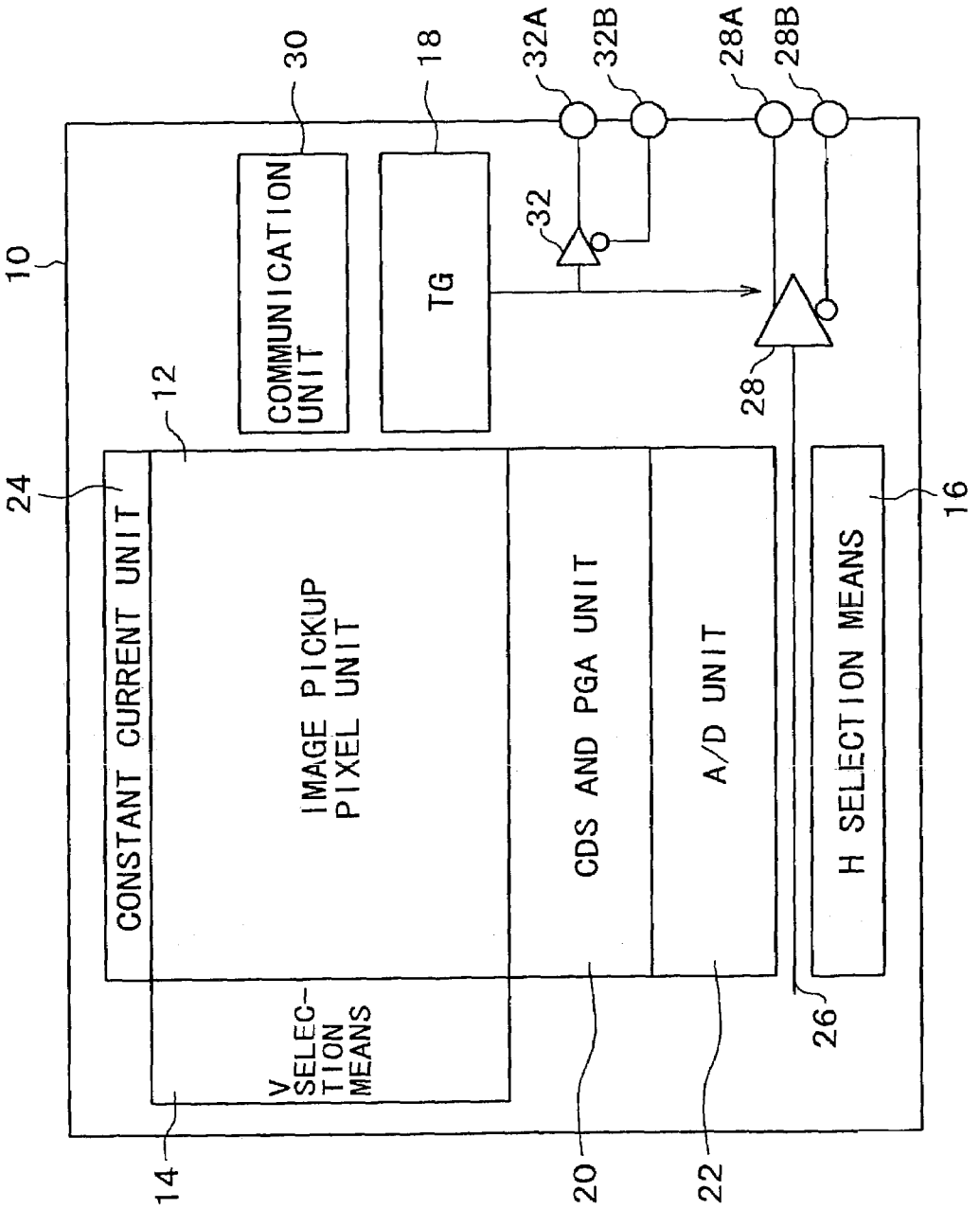


FIG. 1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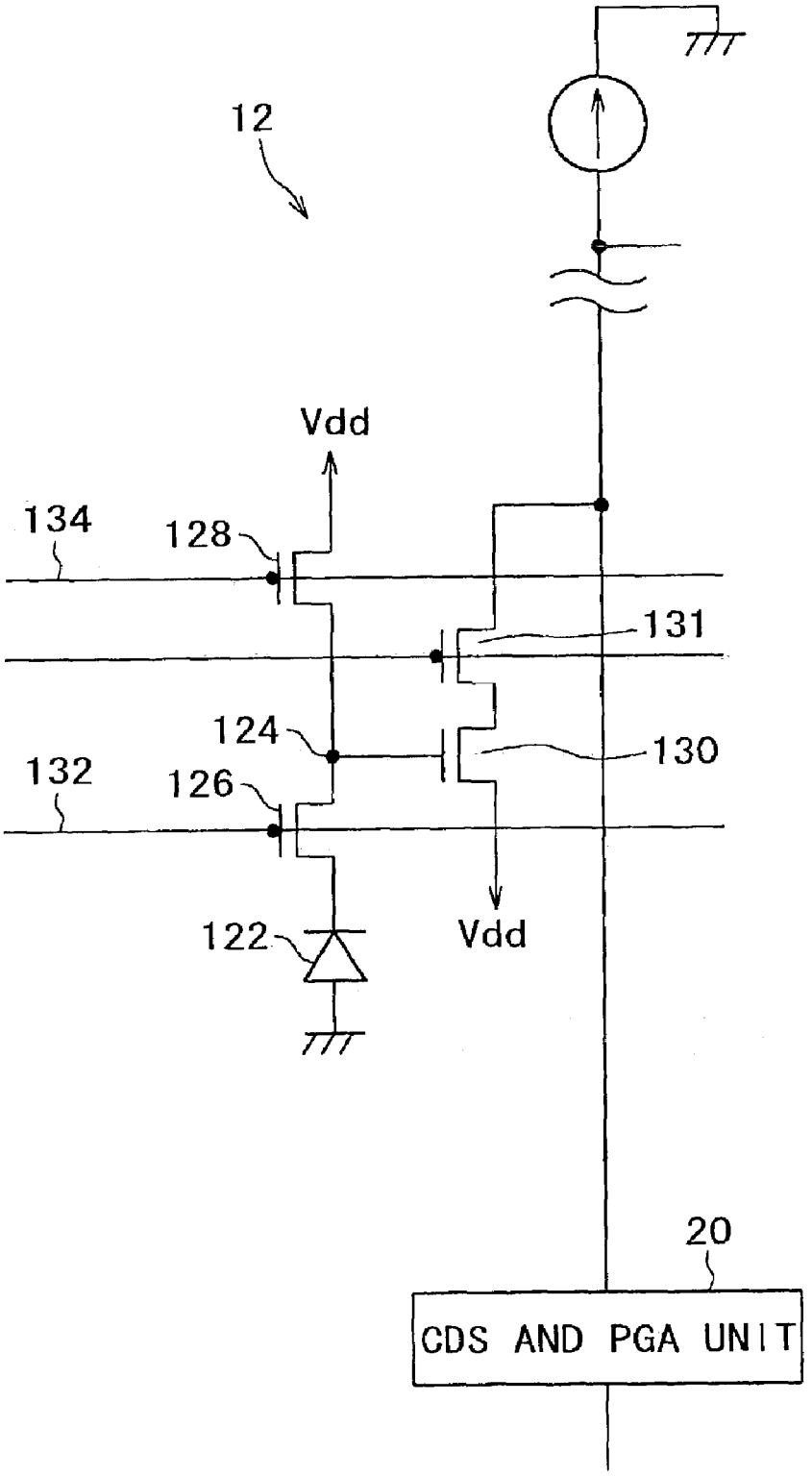
28A
28B
30
32
32A
32B
COMMUNICATION UNIT
TG
CONSTANT CURRENT UNIT
IMAGE PICKUP PIXEL UNIT
V SELECTION MEANS
CDS AND PGA UNIT
A/D UNIT
H SELECTION MEANS

FIG. 2



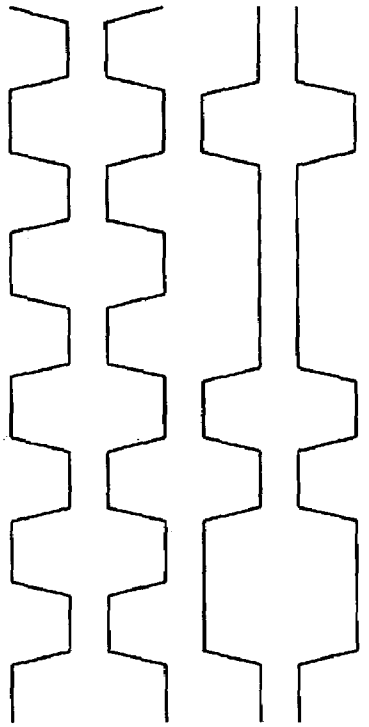


FIG. 3A OUTPUT CLOCK

FIG. 3B INVERTED OUTPUT CLOCK

FIG. 3C ONE VIDEO SIGNAL OUTPUT

FIG. 3D CORRESPONDING INVERTED VIDEO OUTPUT

FIG. 4

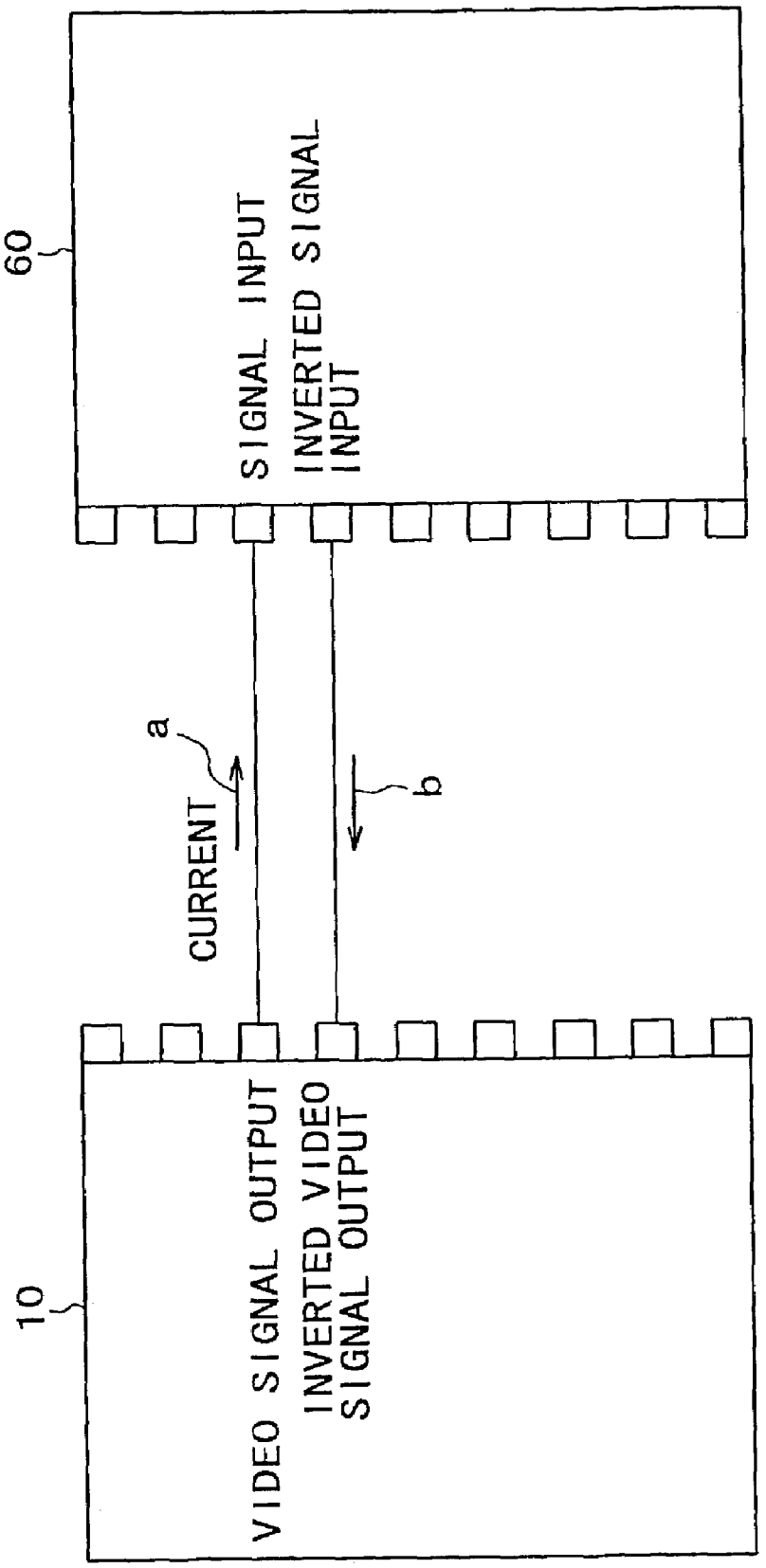
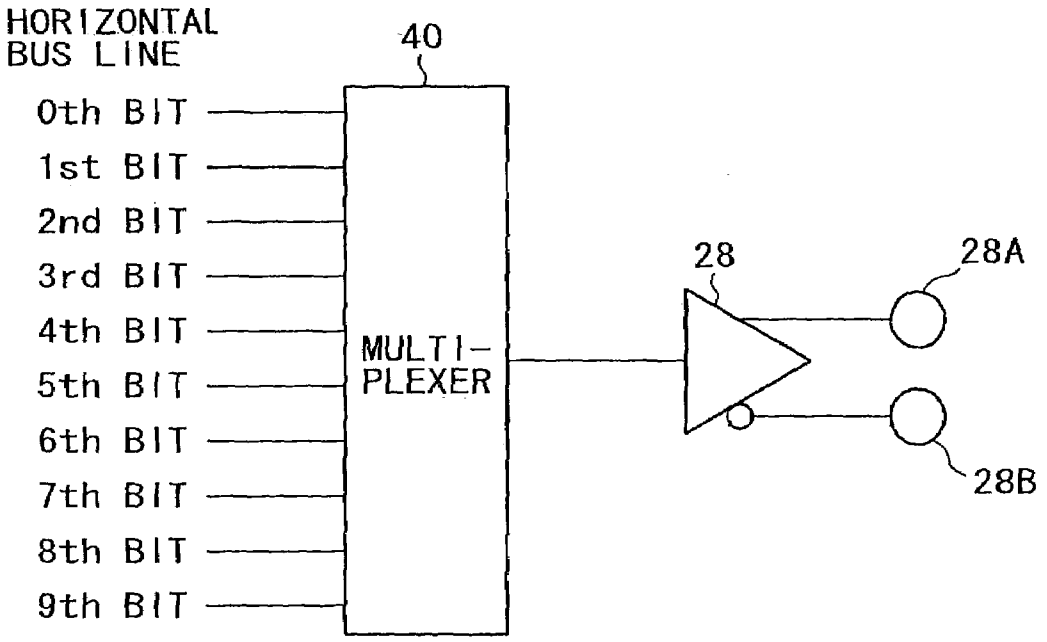

60
SIGNAL INPUT
INVERTED SIGNAL INPUT
a
CURRENT
b
10
VIDEO SIGNAL OUTPUT
INVERTED VIDEO SIGNAL OUTPUT

FIG. 5


HORIZONTAL
BUS LINE
40
0th BIT
1st BIT
2nd BIT
3rd BIT
4th BIT
5th BIT
6th BIT
7th BIT
8th BIT
9th BIT
MULTI-
PLEXER
28
28A
28B

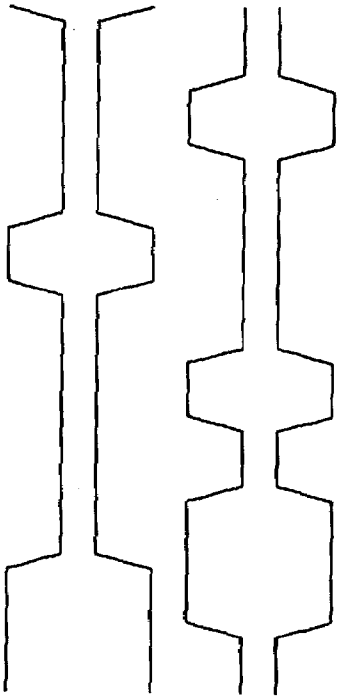


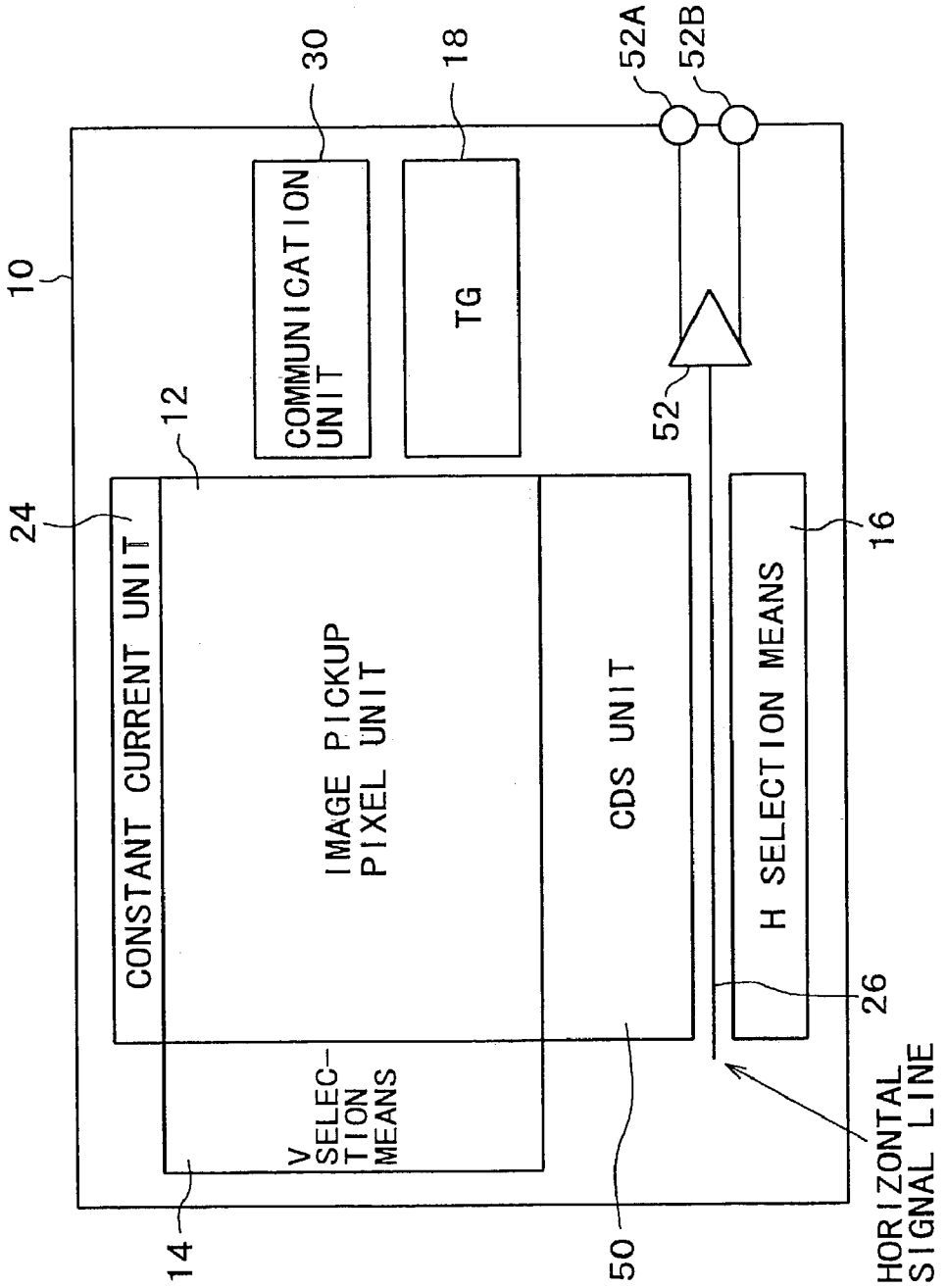
FIG. 6A STROBE

FIG. 6B INVERTED STROBE

FIG. 6C VIDEO SIGNAL OUTPUT

FIG. 6D INVERTED VIDEO SIGNAL OUTPUT

FIG. 7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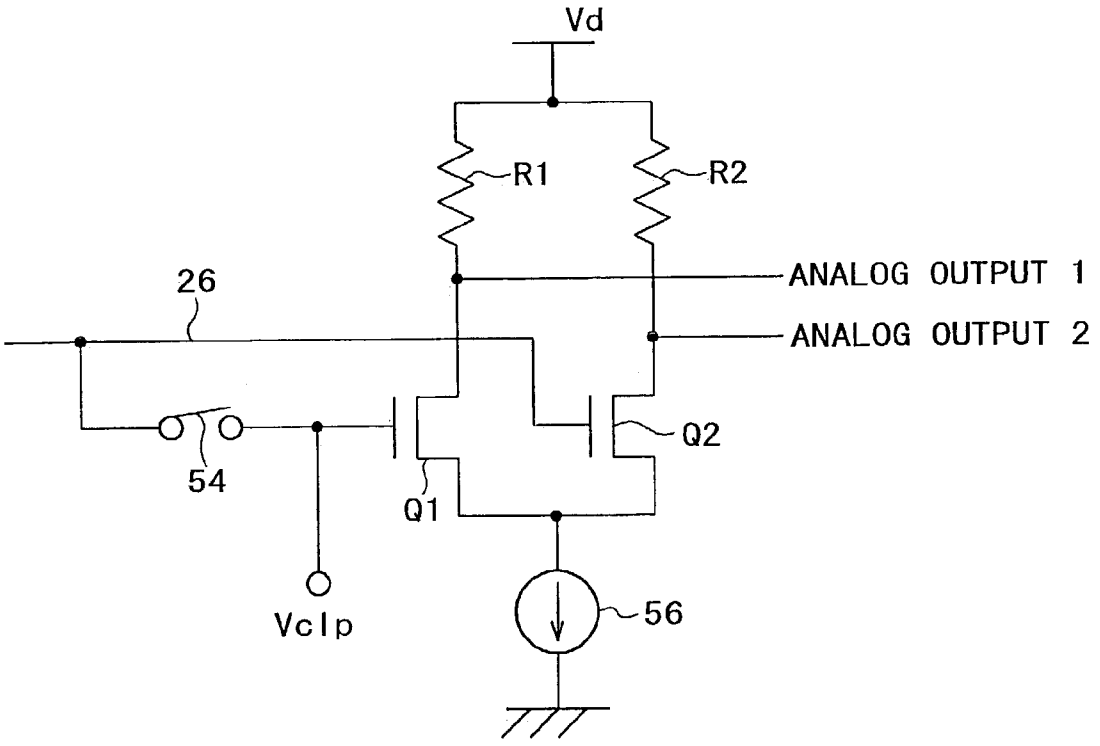
52A
52B
COMMUNICATION UNIT
TG
CONSTANT CURRENT UNIT
IMAGE PICKUP PIXEL UNIT
CDS UNIT
H SELECTION MEANS
V SELECTION MEANS
HORIZONTAL SIGNAL LINE

FIG. 8



SOLID-STATE IMAGE PICKUP DEVICE AND OUTPUT METHOD THEREOF

BACKGROUND OF THE INVENTION

The present invention relates to a solid-state image pickup device and an output method thereof used in various image sensors and camera systems for taking a picture of a subject and outputting a video signal.

Conventionally, in a case of 10-bit digital output, for example, this type of solid-state image pickup device has ten output terminals corresponding to the bit width.

Specifically, in the solid-state image pickup device, each light signal read from an image pickup pixel unit is sampled into 10 bits, the ten output terminals become high or low in synchronism with a clock, and thereby a signal of one pixel is outputted with one clock.

It has recently been important to increase reading speed. In a VGA format with about three hundred thousand pixels, for example, an output rate is 12 MHz, and 30 images per second, which is seen by the human eye to be a smooth moving image, can be outputted.

However, to output 30 images per second from a solid-state image pickup device with three million pixels or 30 million pixels requires high-speed operation at 120 MHz or 1.2 GHz.

Further, even if such an extremely large number of pixels is not required, to construct a camera system having a high time resolution for capturing crash tests on cars and the moment of impact of a ball hit by a baseball batter, for example, requires an output of 100 to 1000 images per second and, thus, requires a high-speed output.

Thus, conventionally, the number of output terminals is increased to provide hundreds of output terminals, whereby video signals are outputted in parallel.

Such a configuration in which output terminals are simply provided in parallel with each other, however, has a large number of output terminals, thus leading to an increase in area and cost of the solid-state image pickup device.

An IC in a next stage also is increased in size with an increased number of input terminals. As a result, various problems occur, such as difficulty in implementation, difficulty in reducing the size of the camera, difficulty in synchronizing many output signals, difficulty in output at high clock speeds because of the problem of synchronization, and the like.

On the other hand, to reduce the number of output the clock speed is increased, however, the time of charging and discharging a capacitance of a path to the IC in the next stage cannot be ignored, and waveforms are blunted. In the worst case, signals do not reach a high/low level of the IC in the next stage, and consequently the IC in the next stage cannot recognize the signals.

Such a problem occurs not only when the clock speed is to be increased but also when the capacitance in a signal path is increased for some reason, for example, because the path to the IC in the next stage is desired to be lengthened for use in an endoscope.

Further, output at a high clock speed causes undesired radiation to be emitted from the signal path between the solid-state image pickup device and the IC in the next stage and, thus, affects operation of other electronic apparatuses and the solid-state image pickup device itself. Audio/video apparatuses, for example, cause degradation in sound quality/picture quality.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a solid-state image pickup device and an output method thereof that can realize the super-high speed of video signals and reduce undesired radiation.

In order to achieve the above object, according to an aspect of the present invention, there is provided a solid-state image pickup device comprising: an image pickup pixel unit including a plurality of pixels; a signal processing unit for subjecting a video signal outputted from the image pickup pixel unit to predetermined signal processing; and an output buffer unit for outputting the video signal processed by the signal processing unit, wherein the output buffer unit outputs the video signal and an inverted video signal obtained by inverting the video signal.

Further, according to another aspect of the present invention, there is provided an output method of a solid-state image pickup device, the solid-state image pickup device including: an image pickup pixel unit including a plurality of pixels; a signal processing unit for subjecting a video signal outputted from the image pickup pixel unit to predetermined signal processing; and an output buffer unit for outputting the video signal processed by the signal processing unit, and the output method comprises: outputting the video signal and an inverted video signal obtained by inverting the video signal from the output buffer unit.

The solid-state image pickup device according to the present invention outputs the video signal and the inverted video signal of the video signal from the output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize the super-high speed of video signals.

Further, the output method according to the present invention outputs the video signal and the inverted video signal of the video signal from the output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize the super-high speed of video signals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of an outline of a solid-state image pickup device according to a first embodiment of the present invention;

FIG. **2** is a circuit diagram of an outline of a unit pixel of the solid-state image pickup device shown in FIG. **1**;

FIGS. **3**A, **3**B, **3**C, and **3**D are timing charts showing signal waveforms in an output stage of the solid-state image pickup device shown in FIG. **1**;

FIG. **4** is a block diagram showing an example of a connection between the solid-state image pickup device shown in FIG. **1** and an IC in a next stage;

FIG. **5** is a block diagram showing a configuration of an output buffer unit in a solid-state image pickup device according to a second embodiment of the present invention;

FIGS. **6**A, **6**B, **6**C, and **6**D are timing charts showing signal waveforms in an output stage of the solid-state image pickup device shown in FIG. **5**;

FIG. **7** is a plan view of an outline of a solid-state image pickup device according to a third embodiment of the present invention; and

FIG. **8** is a circuit diagram showing an example of a configuration of a differential output amplifier provided in the solid-state image pickup device shown in FIG. **7**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of a solid-state image pickup device and an output method thereof according to the present invention will hereinafter be described.

The output methods of the solid-state image pickup devices according to the embodiments use a differential output configuration and an IC in a next stage that uses a differential-amplifier configuration for input, whereby a super-high speed of a video signal is realized while controlling an increase in clock speed. It is thereby possible to alleviate the problem of undesired radiation and to reduce the number of output terminals by serial output. Further, as later described, it is more desirable to use a strobe signal output.

Concrete examples of the present invention will be described hereinafter.

FIG. **1** is a plan view of an outline of a solid-state image pickup device according to a first embodiment of the present invention, showing the main components necessary for a description of the solid-state image pickup device as a whole according to the first embodiment.

The solid-state image pickup device according to the first embodiment is specifically a CMOS-type image sensor. The solid-state image pickup device according to the first embodiment includes an image pickup pixel unit **12**, V-selection means **14**, H-selection means **16**, a timing generator (TG) **18**, a CDS and PGA unit **20**, an A/D unit **22**, a constant current unit **24**, a horizontal bus line **26**, an output buffer unit **28**, a communication unit **30** and the like, which are formed on a semiconductor chip **10**.

The image pickup pixel unit **12** has a large number of pixels arranged in the form of a two-dimensional matrix. As shown in FIG. **2**, each of the pixels includes a photodiode **122**, serving as a photoelectric converting device for generating a signal charge corresponding to an amount of light received and storing the signal charge, and MOS transistors, such as a transfer transistor **126**, for transferring the signal charge converted and stored by the photodiode **122** to a floating diffusion part (FD part) **124**, a reset transistor **128** for resetting a potential of the FD part **124**, an amplifying transistor **130** for outputting an output signal corresponding to the potential of the FD part **124**, and an address transistor **131** for selecting a pixel.

Further, the image pickup pixel unit **12** has various driving wirings **132** and **134** arranged in a horizontal direction for driving and controlling the MOS transistors. The pixels of the image pickup pixel unit **12** are sequentially selected in units of a horizontal line (pixel row) in a vertical direction by the V-selection means **14**. The MOS transistors of each of the pixels are controlled by various pulse signals from the timing generator **18**. Thereby, a signal of each of the pixels is outputted to the CDS and PGA unit **20** via a vertical signal line for each pixel column.

The CDS and PGA unit **20** has a CDS and PGA circuit for each pixel column of the image pickup pixel unit **12**. The CDS and PGA unit **20** subjects a pixel signal-read from each pixel column of the image pickup pixel unit **12** to signal processing, such as CDS (correlated double sampling) and PGA (programmable gain control), and then outputs a resulting pixel signal to the A/D unit **22**.

The A/D unit **22** has an A/D conversion circuit for each pixel column of the image pickup pixel unit **12**. The A/D unit **22** converts the pixel signal of each pixel column from the CDS and PGA unit **20** from analog signal form to digital signal form and then outputs the result.

The H-selection means **16** selects digital signal outputs from the A/D unit **22** in a horizontal direction and then outputs the digital signal outputs to the horizontal bus line **26**. It is to be noted that the first embodiment adopts 10-bit output and has ten horizontal bus lines **26**.

The constant current unit **24** supplies the image pickup pixel unit **12** as described above with a constant current for each pixel column.

The timing generator **18** supplies parts other than the pixels of the image pickup pixel unit **12** as described above with various timing signals.

The output buffer unit **28** outputs a digital signal supplied thereto from the horizontal bus line **26** to external terminals of the semiconductor chip **10**.

The communication unit **30** communicates with the outside of the semiconductor chip **10**. The communication unit **30** performs operations such as, for example, controlling an operating mode of the timing generator **18** and outputting parameters indicating the conditions of the semiconductor chip **10** to the outside.

In the above configuration of the first embodiment, the method of outputting a video signal by the output buffer unit **28** and a clock of the timing generator **18** constitutes main characteristic parts of the first embodiment.

First, the output buffer unit **28** in the first embodiment buffers and outputs a digital signal from the horizontal bus line **26**. At this time, in addition to the normal video signal, the output buffer unit **28** generates an inverted output of the normal video signal.

The normal video signal and the inverted output are outputted from a video signal output terminal **28**A and an inverted video signal output terminal **28**B, respectively, to the outside of the chip **10**.

It is to be noted that though omitted in FIG. **1**, the inverted video signal is formed by 10 bits so as to correspond to the video signal of 10 bits, and output terminals **28**A and **28**B total 20 (20 bits).

Next, the timing generator **18** supplies a clock (output clock) to the output buffer unit **28**. The clock is buffered by another output buffer unit **32**, and the clock and a clock obtained by inverting the clock are outputted to the outside from output terminals **32**A and **32**B, respectively.

FIGS. **3**A, **3**B, **3**C, and **3**D are timing charts showing signal waveforms in the first embodiment. FIG. **3**A shows the output clock; FIG. **3**B shows the inverted output clock; FIG. **3**C shows one video signal; and FIG. **3**D shows an inverted video signal corresponding to the video signal shown in FIG. **3**C.

In this case, the signals are changed at both a rising edge and a falling edge of the output clock, and 10 bits per pixel are outputted in half a clock cycle of the output clock.

FIG. **4** is a block diagram showing an example of a connection between the solid-state image pickup device (semiconductor chip **10**) and an IC **60** in a next stage.

The IC **60** in the next stage includes a signal processing circuit, a DSP (Digital Signal Processor) and the like for receiving the video signal and the inverted video signal and performing various kinds of signal processing. The IC **60** in the next stage has a differential amplifier in an input stage thereof, and it is therefore able to recognize even the input signals having waveforms blunted beyond a conventionally-allowable range. This enables a super-high speed of the

system, an addition of capacitance to a signal path, or a reduction in the size of the output buffer of the solid-state image pickup device.

When the output signals are changed to a high and a low, charging and discharging current paths flow in the directions of arrows a and b shown in FIG. **4**, for example. However, the output and the inverted output cause currents to flow in opposite directions. Therefore, when the paths are disposed adjacent to each other, undesired radiations can be reduced by canceling each other. The above description of the video signals also applies to the output clocks.

It is to be noted that while the example shown in FIG. **1** is a CMOS-type image sensor as an example of a configuration of the solid-state image pickup device, the present invention is not limited to the above-described configuration, and it is similarly applicable to solid-state image pickup devices in general that output digital video signals.

A second embodiment of the present invention will be described next.

While the first embodiment described above has a total of 20 parallel terminals as video signal and inverted video signal output terminals, the second embodiment of the present invention has one video signal output terminal and one inverted video signal output terminal for output by time division. It is to be noted that as in the first embodiment described above, the second embodiment has ten horizontal bus lines.

FIG. **5** is a block diagram showing a configuration of an output buffer unit in the second embodiment.

As shown in FIG. **5**, in the second embodiment, a multiplexer **40** is provided between the horizontal bus lines **26** and the output buffer unit **28**.

The multiplexer **40** selects the horizontal bus lines **26** in appropriate timing. A signal of a selected horizontal bus line **26** is inputted to the output buffer unit **28**, buffered by the output buffer unit **28**, and then led to the video signal output terminal **28**A and the inverted-signal output terminal **28**B.

Thus, by outputting a 10-bit video signal to the outside of the chip with ten or more clocks, it is possible to reduce the number of output terminals as compared with the foregoing first embodiment. The reduction in the number of output terminals, therefore, makes it possible to miniaturize the solid-state image pickup device and a camera or the like using the solid-state image pickup device. Further, since the second embodiment has a total of two output terminals, it is easy to control a phase difference between output signals to within an allowable range, and it is thus easier to increase clock speed.

With such a configuration, it is desirable to output a strobe signal instead of the clock signal described above.

The strobe signal is inverted in timing in which the video signal is not inverted.

FIGS. **6**A, **6**B, **6**C, and **6**D are timing charts showing signal waveforms in the second embodiment. FIG. **6**A shows a strobe signal; FIG. **6**B shows an inverted strobe signal; FIG. **6**C shows one video signal; and FIG. **6**D shows an inverted video signal corresponding to the video signal shown in FIG. **6**C.

In this case, since either one of the video signal or the strobe signal is inverted, only a load of one of the signals is put on the device outputs in the timing of each clock, and the load is constant. By obtaining an exclusive disjunction of the strobe signal and the video signal, a clock can be reproduced in an IC in a next stage.

A third embodiment of the present invention will next be described.

FIG. **7** is a plan view of an outline of a solid-state image pickup device according to a third embodiment of the present invention, showing main components necessary for a description of the solid-state image pickup device as a whole according to the third embodiment.

The solid-state image pickup device according to the third embodiment is formed by omitting the A/D unit **22** shown in FIG. **1**, using a CDS unit **50** that omits a PGA unit in place of the CDS and PGA unit **20** shown in FIG. **1**, and using an analog differential output amplifier **52** in place of the output buffer unit **28** shown in FIG. **1**. The solid-state image pickup device according to the third embodiment thereby produces analog output.

Incidentally, the CDS unit **50** is the same as the CDS unit of the CDS and PGA unit **20**. The other parts are the same as in the example shown in FIG. **1**. Therefore, the other parts are identified by the same reference numerals as in FIG. **1**, and their description will be omitted.

In such a configuration, the differential-output amplifier **52** outputs a signal from a horizontal bus line **26** (horizontal signal line) to the outside of the chip. At this time, the differential-output amplifier **52** outputs the signal in the form of differential signals of an analog video signal and an inverted analog video signal.

FIG. **8** is a circuit diagram showing an example of a configuration of the differential-output amplifier **52**.

As shown in FIG. **8**, the differential-output amplifier **52** has a differential circuit with resistances R**1** and R**2** and MOS transistors Q**1** and Q**2** between a driving power supply Vd and a constant-current source **56**. The analog video signal and the inverted analog video signal mentioned above are outputted as an analog output **1** and an analog output **2** from a node of the resistance R**1** and the MOS transistor Q**1** and a node of the resistance R**2** and the MOS transistor Q**2**.

An input stage of the MOS transistors Q**1** and Q**2** is also of a differential type. The horizontal bus line **26** (horizontal signal line) is connected to a gate of one MOS transistor Q**2**, and a clamping voltage Vclp is applied to a gate of the other MOS transistor Q**1**.

A clamping switch **54** is inserted between the horizontal signal line **26** and the clamping voltage Vclp. The horizontal signal line **26** is reset to the clamping voltage Vclp via the clamping switch **54**.

After the clamping switch **54** is opened, a signal from the CDS unit **50** is put on the horizontal bus line **26**, and a difference between the signal and the clamping voltage Vclp is amplified and then outputted to the analog output **1** and the analog output **2**.

Incidentally, depending on the load setting, a two-stage configuration in which a differential amplifier with a higher driving capability is disposed in a succeeding stage may be used, or a configuration in which output is produced through a voltage follower may be used.

Such analog output inherently requires one video output terminal and is, therefore, advantageous for miniaturization of the device.

In this example, two outputs are required, but do not present a great problem in miniaturization of the device. Further, when one of the two analog outputs is at a high potential, the other is at a low potential. Thus, for the same reason described in the example of FIG. **3**, currents flowing through wirings to an IC in a next stage are in directions opposite to each other, and thereby undesired radiation is reduced. Further, less susceptibility to noise superimposed on paths to the IC in the next stage is obtained.

It is thereby possible to alleviate a problem associated with high-speed clock output, a problem associated with a

long distance to the IC in the next stage, or a problem of the presence of an adjacent apparatus susceptible to radiation.

It is to be noted that while the example shown in FIG. **7** is also a CMOS-type image sensor as an example of a configuration of a solid-state image pickup device, the present invention is not limited to the above-described configuration and is similarly applicable to CCD-type solid-state image pickup devices and solid-state image pickup devices in general that output analog video signals.

As described above, a solid-state image pickup device according to the present invention outputs a video signal and an inverted video signal of the video signal from an output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize super-high speed video signals.

Further, an output method of a solid-state image pickup device according to the present invention outputs a video signal and an inverted video signal of the video signal from an output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize super-high speed of video signals.

In the foregoing first embodiment, in particular, a differential amplifier is used in the input stage of the IC in the next stage, and it is able to recognize even signals having blunter waveforms. This enables an increase in speed of the system, an addition of capacitance to signal paths, or a reduction in size of the output buffer unit of the solid-state image pickup device. When the output signals are changed, the charging and discharging currents of the paths flow in the directions of the arrows shown in FIG. **4**, for example. However, the output and the inverted output flow in opposite directions. Therefore, when the paths are disposed adjacent to each other, undesired radiations can be reduced by canceling each other.

Further, in addition to the effects of the first embodiment, the foregoing second embodiment makes it possible to reduce the number of output terminals. The reduction in the number of output terminals, therefore, makes it possible to miniaturize the solid-state image pickup device and a camera using the solid-state image pickup device. Further, since the second embodiment has two signal output terminals including an inverted signal output terminal, it is easy to control a phase difference between output signals to within an allowable range, and it is thus easier to increase clock speed.

Further, the foregoing third embodiment has the effect of alleviating the problem of undesired radiation and obtaining less susceptibility to noise superimposed on paths to an IC in a next stage.

What is claimed is:

1. A solid-state image pickup device comprising:
- an image pickup pixel unit including a plurality of pixels;
- a signal processing unit for subjecting a video signal outputted from said image pickup pixel unit to predetermined signal processing;
- an output buffer unit for outputting the video signal processed by said signal processing unit; and
- a communication unit that controls a timing mode of the signal processing unit and outputs parameters corresponding to operating conditions of the image pickup device,
- wherein said output buffer unit outputs said video signal and an inverted video signal obtained by inverting said video signal, said outputs being configured for connection to a next stage that is separate from the image pickup device and to accommodate a cancellation of undesired radiation from the paths of the video signal and the inverted video signal between the image pickup device and the next stage.

2. A solid-state image pickup device as claimed in claim **1**, wherein said output buffer unit has an output terminal for outputting said video signal and an output terminal for outputting said inverted video signal.

3. A solid-state image pickup device as claimed in claim **1**, further comprising an analog/digital conversion unit for converting the video signal into a digital signal in a stage preceding said output buffer unit, wherein said video signal and said inverted video signal outputted from said output buffer unit are digital signals.

4. A solid-state image pickup device as claimed in claim **1**, further comprising a timing signal generating unit for generating a timing signal, wherein a clock in synchronism with an output of said video signal and an inverted clock of the clock are outputted by using said timing signal.

5. A solid-state image pickup device as claimed in claim **1**, wherein the pixels of said image pickup pixel unit are arranged in a form of a two-dimensional matrix.

6. A solid-state image pickup device as claimed in claim **5**, wherein each of the pixels of said image pickup pixel unit includes:
- a photoelectric converting device;
- transfer means for transferring a signal charge converted and stored by said photoelectric converting device to a floating diffusion part;
- reset means for resetting a potential of said floating diffusion part; and
- amplifying means for outputting an output signal corresponding to the potential of said floating diffusion part.

7. A solid-state image pickup device as claimed in claim **6**, further comprising:
- vertical selection means for selecting each horizontal pixel row of said image pickup pixel unit in a vertical direction; and
- pixel driving means for driving each pixel of a pixel row selected by said vertical selection means via pixel driving wiring.

8. An output method of a solid-state image pickup device, said solid-state image pickup device including an image pickup pixel unit including a plurality of pixels; a signal processing unit for subjecting a video signal outputted from said image pickup pixel unit to predetermined signal processing; and an output buffer unit for outputting the video signal processed by said signal processing unit, said output method comprising:
- outputting said video signal and an inverted video signal obtained by inverting said video signal using outputs from said output buffer unit, wherein said video signal and said inverted video signal outputs are configured for connection to a next stage that is separate from the image pickup device and to accommodate a cancellation of undesired radiation from the paths of the video signal and the inverted video signal between the image pickup device and the next stage; and
- outputting a signal indicating conditions of said image pickup device.

9. An output method of a solid-state image pickup device as claimed in claim **8**, wherein said video signal and said inverted video signal are digital signals.

10. An output method of a solid-state image pickup device as claimed in claim **8**, wherein a clock in synchronism with

an output of said video signal and an inverted clock of the clock are outputted by using a timing signal.

11. A system including a solid-state image pickup device, said system comprising:

an image pickup pixel unit including a plurality of pixels;

a signal processing unit for subjecting a video signal outputted from said image pickup pixel unit to predetermined signal processing;

an output buffer unit for outputting the video signal processed by said signal processing unit; and

a signal processing circuit formed on a substrate separate from said solid-state image pickup device, for receiving the signal from said output buffer unit; and

a communication unit that controls a timing mode of the signal processing unit and outputs parameters corresponding to operating conditions of said pickup device,

wherein said output buffer unit outputs said video signal and an inverted video signal obtained by inverting said video signal via a first terminal and a second terminal, respectively, and

wherein wiring for connecting said signal processing circuit to said first terminal and wiring for connecting said signal processing circuit to said second terminal are disposed adjacent to each other and are configured to accommodate a cancellation of undesired radiation from the paths of the video signal and the inverted video signal between the image pickup device and the signal processing circuit.

12. A system including a solid-state image pickup device as claimed in claim **11**, wherein each of the pixels of said image pickup pixel unit includes:

a photoelectric converting device;

transfer means for transferring a signal charge converted and stored by said photoelectric converting device to a floating diffusion part;

reset means for resetting a potential of said floating diffusion part; and

amplifying means for outputting an output signal corresponding to the potential of said floating diffusion part.

13. A solid-state image pickup device comprising:

an image pickup pixel unit including a plurality of pixels;

a signal processing unit for subjecting a video signal outputted from said image pickup pixel unit to predetermined signal processing; and

means, including an output buffer unit, for outputting the video signal processed by said signal processing unit at a timing determined by a timing generator; and

a communication unit that controls a timing mode of the signal processing unit and outputs parameters corresponding to operating conditions of said pickup device,

wherein said output buffer unit outputs said video signal and an inverted video signal obtained by inverting said video signal, and wherein said outputs of said output buffer are configured for connection to the signal processing unit and to accommodate a cancellation of undesired radiation from the paths of the video signal and the inverted video signal between the image pickup pixel unit and the signal processing unit.

14. A solid-state image pickup device comprising:

an image pickup pixel unit including a plurality of pixels;

a signal processing unit for subjecting a video signal outputted from said image pickup pixel unit to predetermined signal processing; and

an output buffer unit for outputting the video signal processed by said signal processing unit,

wherein said output buffer unit outputs said video signal and an inverted video signal obtained by inverting said video signal, and

wherein said image pickup pixel unit, said signal processing unit, and said output buffer unit are formed on the same chip, and wherein said outputs of said output buffer are configured for connection to a next stage that is separate from the image pickup device and to accommodate a cancellation of undesired radiation from the paths of the video signal and the inverted video signal between the image pickup device and the next stage.

* * * * *

EXHIBIT G

US007304287B2

(12) **United States Patent**
Mabuchi

(10) **Patent No.: US 7,304,287 B2**
(45) **Date of Patent: *Dec. 4, 2007**

(54) **SOLID-STATE IMAGE PICKUP DEVICE AND OUTPUT METHOD THEREOF**

(75) Inventor: **Keiji Mabuchi**, Kanagawa (JP)

(73) Assignee: **Sony Corporation** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: **Nov. 17, 2006**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
H04N 5/00 (2006.01)
H04N 5/21 (2006.01)
H01L 27/00 (2006.01)

(52) **U.S. Cl.** ..... **250/208.1**; 250/214 A; 250/214.1; 250/214 R; 348/222.1; 348/241; 348/294; 348/300

(58) **Field of Classification Search** ..... 250/208.1, 250/214 DC, 214 A, 214.1, 214 R; 348/222.1, 348/294, 308, 310, 250, 241, 242, 245, 257, 348/300

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,072,366	A	6/2000	Maeda et al.
6,353,488	B1	3/2002	Hieda et al.
6,822,211	B2	11/2004	Hagihara
6,881,942	B2	4/2005	Huang et al.

Primary Examiner—Davienne Monbleau
(74) *Attorney, Agent, or Firm*—Rader Fishman & Grauer PLLC; Ronald P. Kananen

(57) **ABSTRACT**

A solid-state image pickup device has a differential output configuration for an output stage thereof and an IC in a next stage has a differential amplifier configuration for an input stage thereof. An output buffer unit buffers and outputs a digital signal from a horizontal bus line. At this time, in addition to the normal video signal, the output buffer unit generates an inverted output of the normal video signal. The normal video signal and the inverted output are outputted from a video signal output terminal and an inverted video signal output terminal, respectively, to the outside of a chip. Further, a clock, which is supplied from a timing generator to the output buffer unit, also is buffered and outputted to the outside together with an inverted clock. A differential amplifier is used in an input stage of an IC in a next stage, whereby even signals having blunter waveforms can be recognized. This enables an increase in the speed of the system, an addition of capacitance to signal paths, or a reduction in size of the output buffer unit of the solid-state image pickup device.

8 Claims, 8 Drawing Sheets

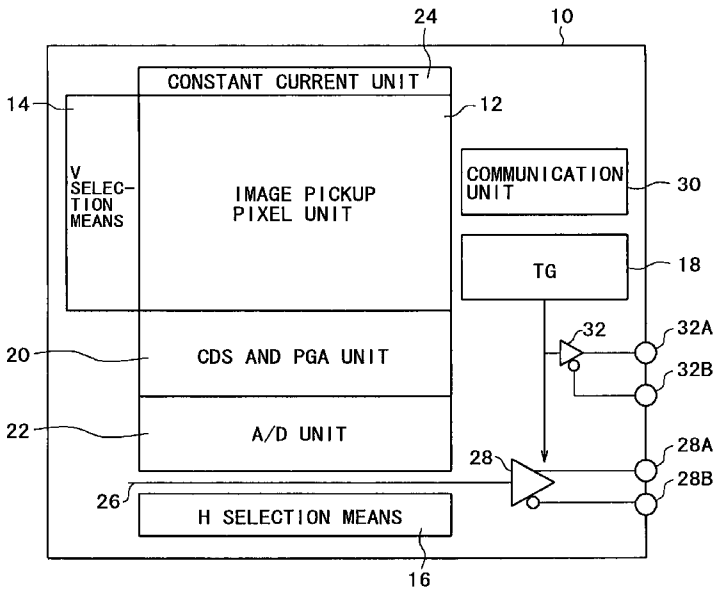


FIG. 1

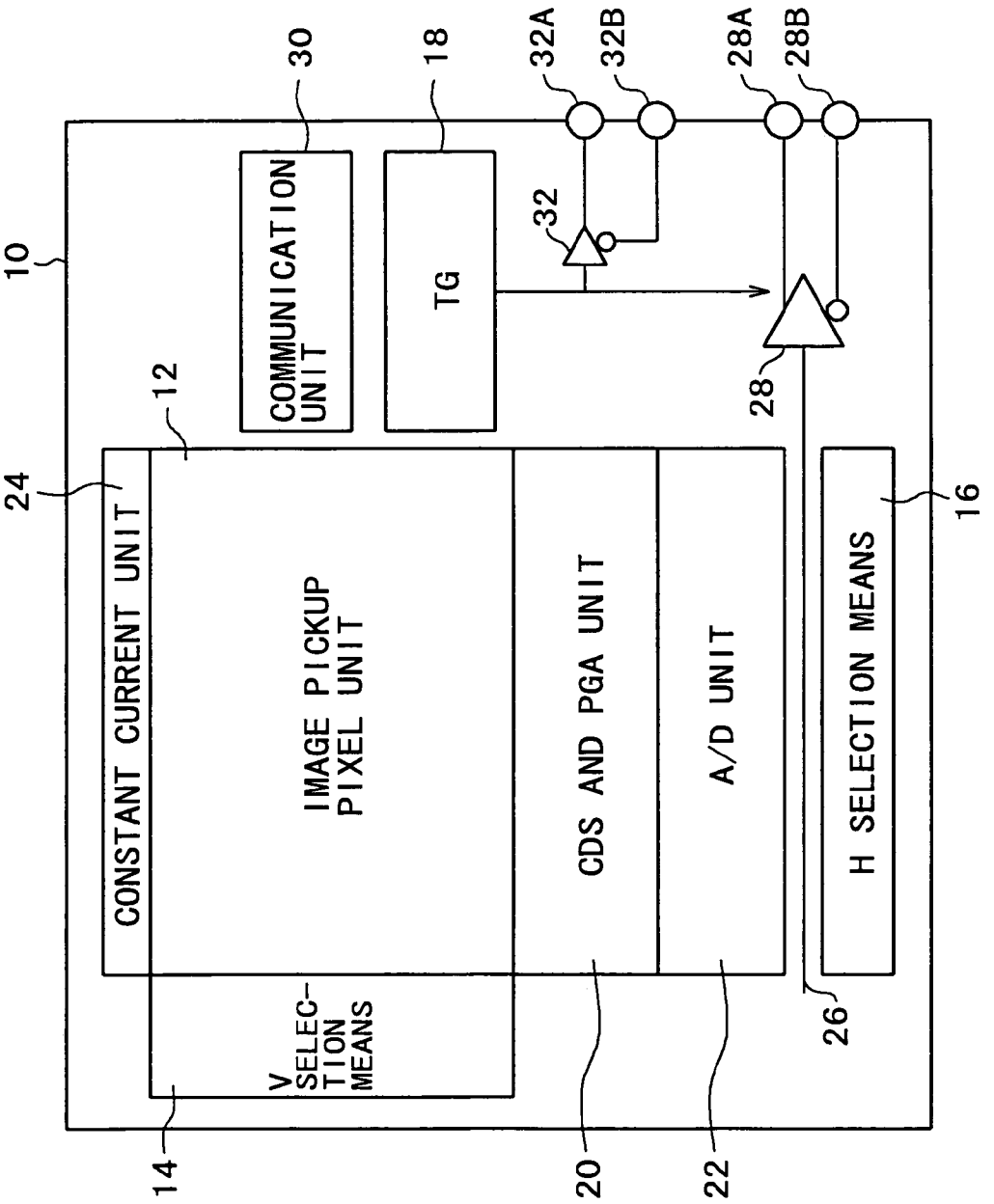
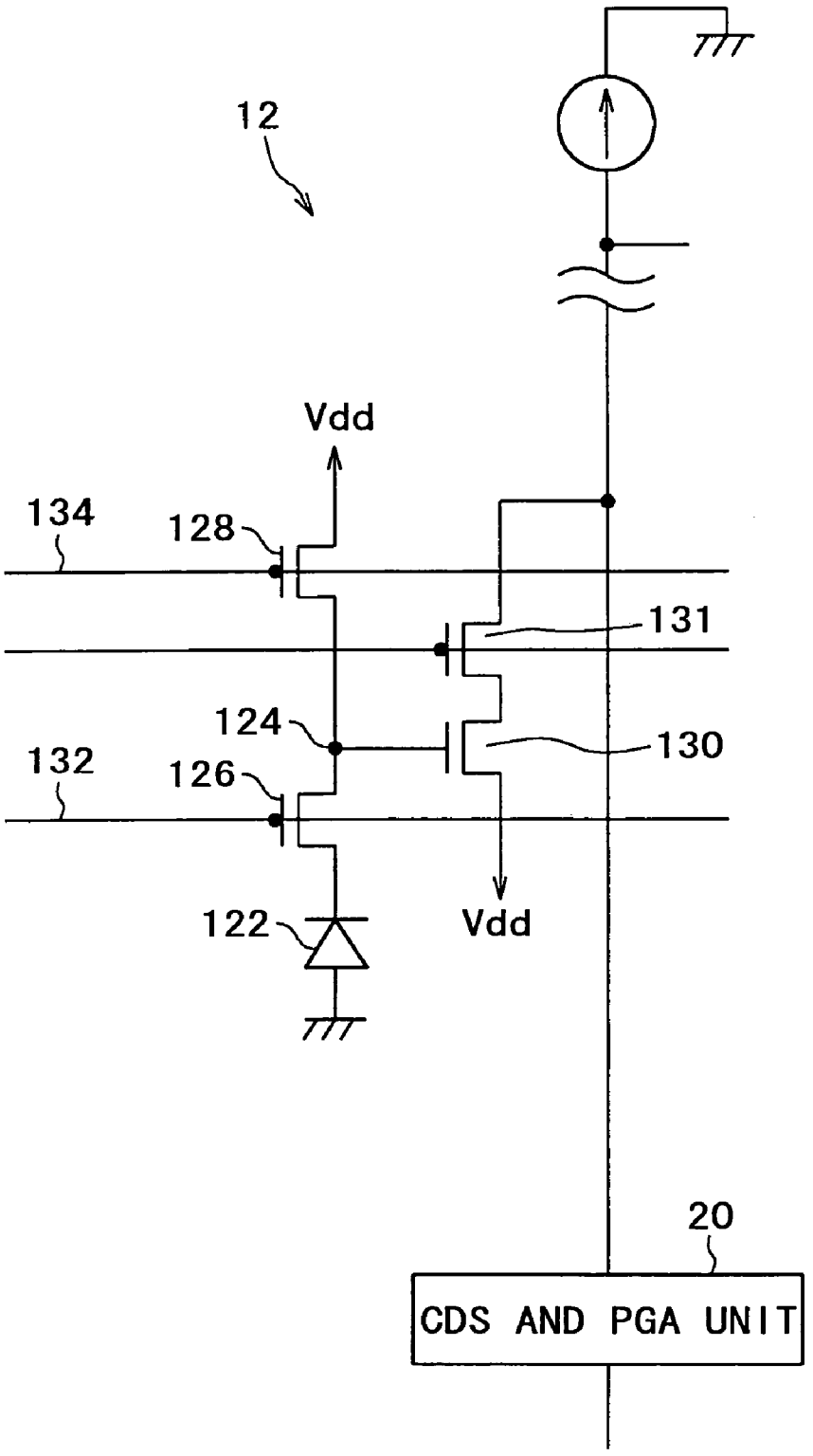

10
12
24
16
30
18
32A
32B
28A
28B
32
28
26
14
20
22
COMMUNICATION UNIT
TG
CONSTANT CURRENT UNIT
IMAGE PICKUP PIXEL UNIT
CDS AND PGA UNIT
A/D UNIT
H SELECTION MEANS
V SELECTION MEANS

FIG. 2



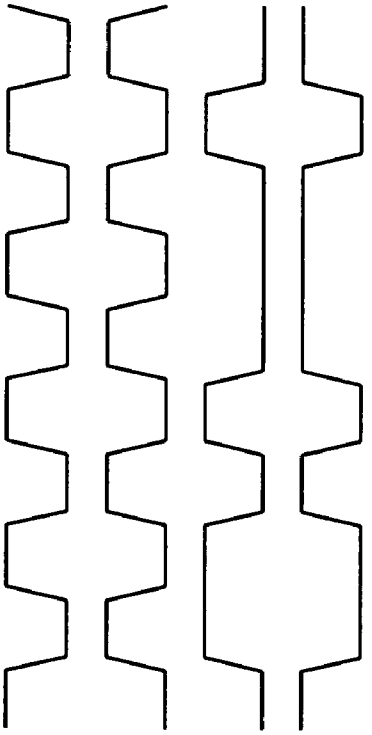


FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 4

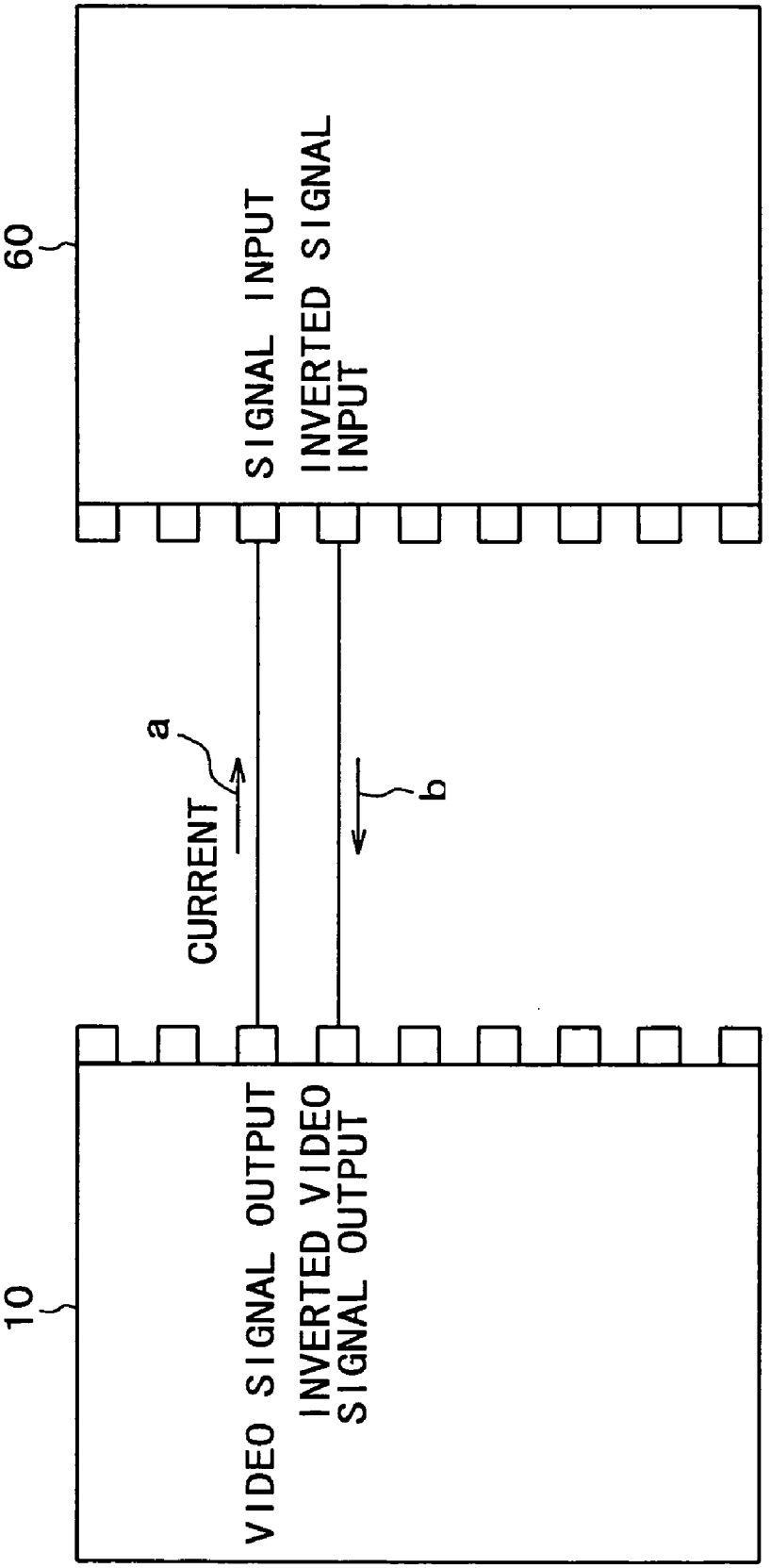
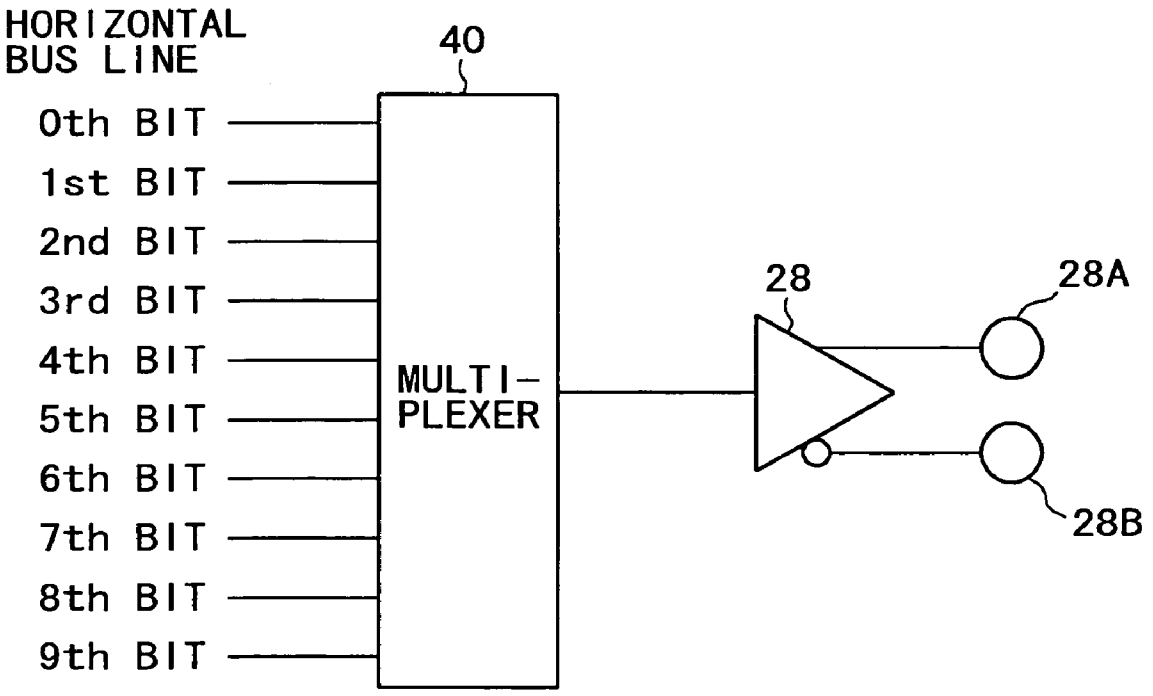

60
SIGNAL INPUT
INVERTED SIGNAL INPUT
a
CURRENT
b
10
VIDEO SIGNAL OUTPUT
INVERTED VIDEO SIGNAL OUTPUT

FIG. 5


HORIZONTAL
BUS LINE
40
0th BIT
1st BIT
2nd BIT
3rd BIT
4th BIT
5th BIT
6th BIT
7th BIT
8th BIT
9th BIT
MULTI-
PLEXER
28
28A
28B

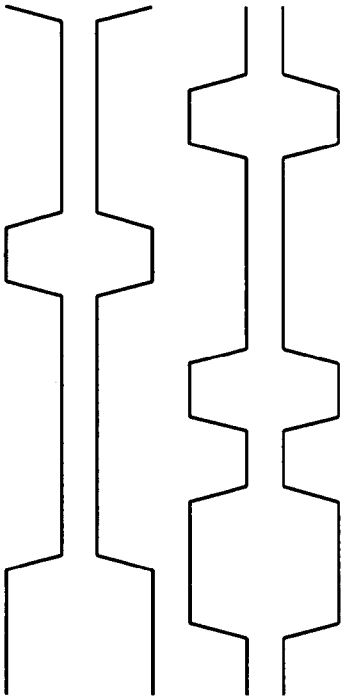


FIG. 6A STROBE

FIG. 6B INVERTED STROBE

FIG. 6C VIDEO SIGNAL OUTPUT

FIG. 6D INVERTED VIDEO SIGNAL OUTPUT

FIG. 7

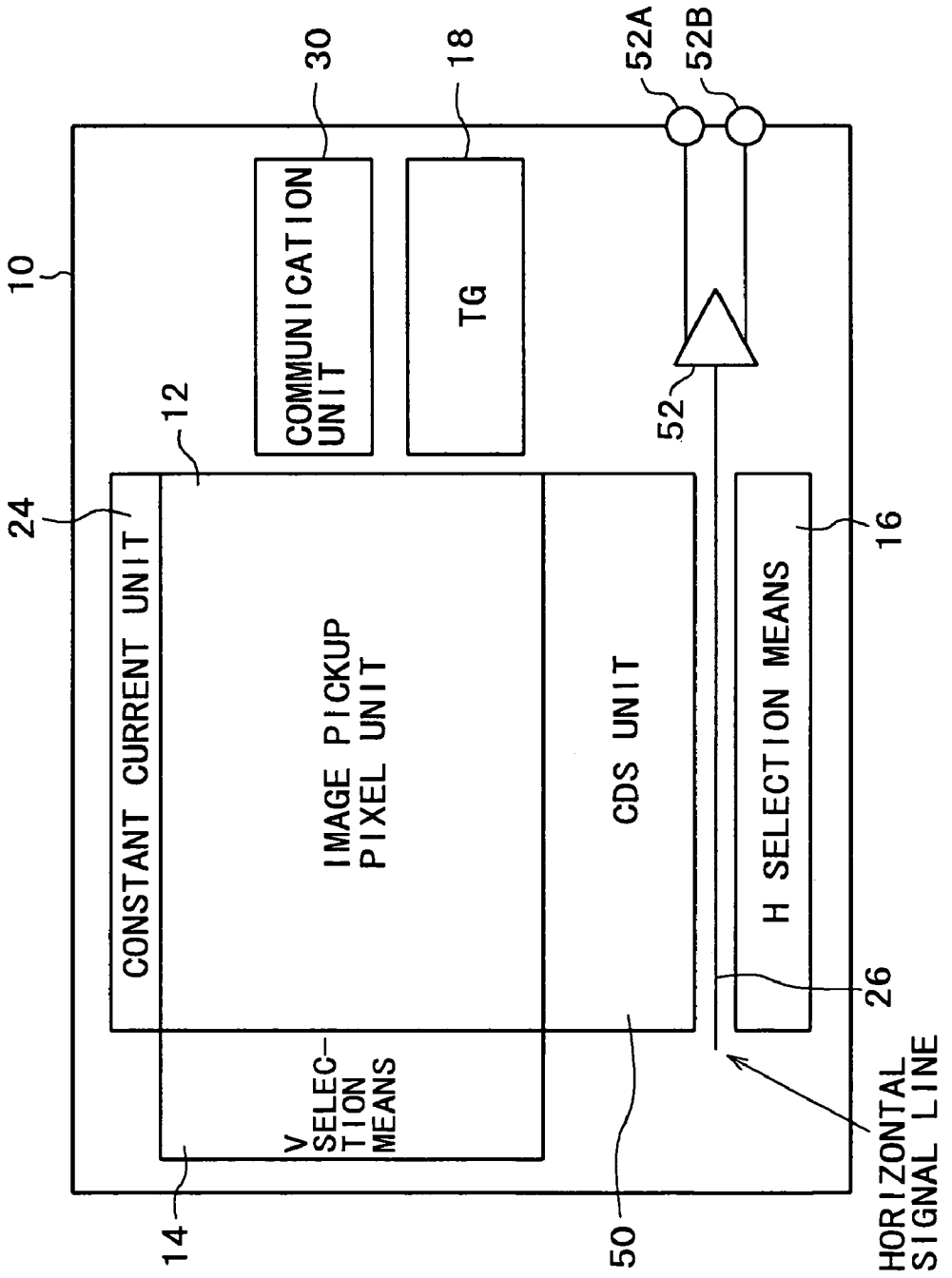
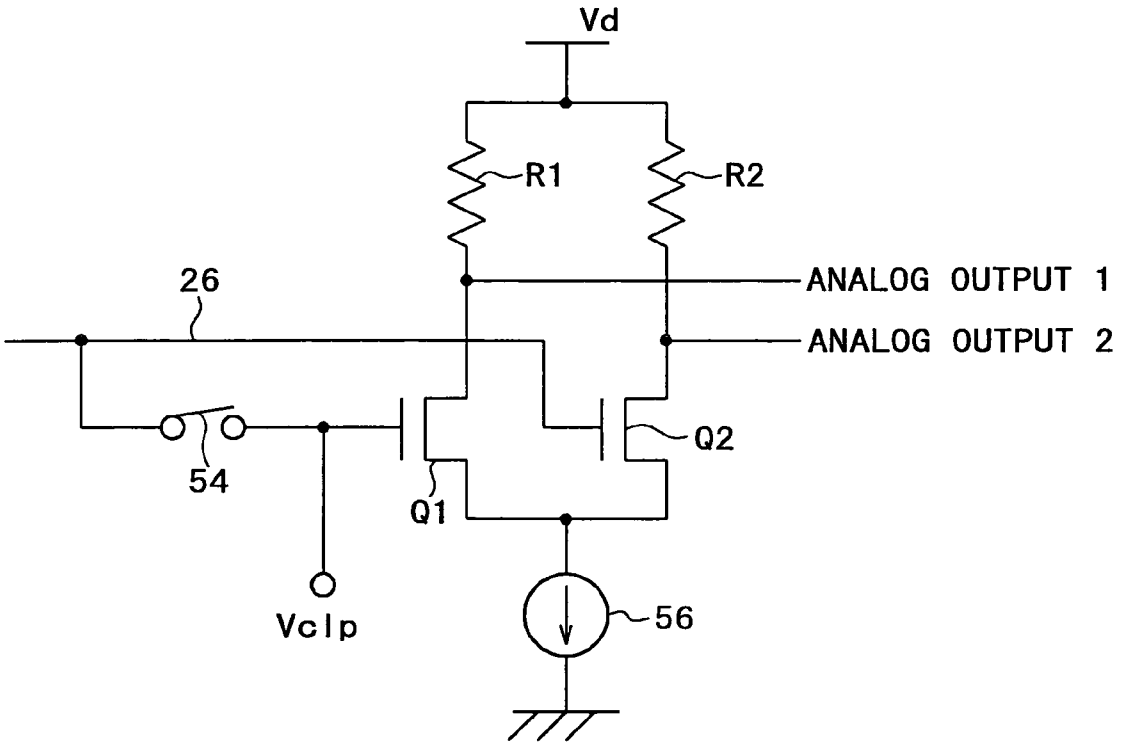

10
12
24
30
18
52A
52B
52
16
26
14
50
COMMUNICATION UNIT
TG
CONSTANT CURRENT UNIT
IMAGE PICKUP PIXEL UNIT
CDS UNIT
H SELECTION MEANS
V SELECTION MEANS
HORIZONTAL SIGNAL LINE

FIG. 8



SOLID-STATE IMAGE PICKUP DEVICE AND OUTPUT METHOD THEREOF

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 10/355,065, filed on Jan. 31, 2003 now U.S. Pat. No. 7,138,617, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a solid-state image pickup device and an output method thereof used in various image sensors and camera systems for taking a picture of a subject and outputting a video signal.

Conventionally, in a case of 10-bit digital output, for example, this type of solid-state image pickup device has ten output terminals corresponding to the bit width.

Specifically, in the solid-state image pickup device, each light signal read from an image pickup pixel unit is sampled into 10 bits, the ten output terminals become high or low in synchronism with a clock, and thereby a signal of one pixel is outputted with one clock.

It has recently been important to increase reading speed. In a VGA format with about three hundred thousand pixels, for example, an output rate is 12 MHz, and 30 images per second, which is seen by the human eye to be a smooth moving image, can be outputted.

However, to output 30 images per second from a solid-state image pickup device with three million pixels or 30 million pixels requires high-speed operation at 120 MHz or 1.2 GHz.

Further, even if such an extremely large number of pixels is not required, to construct a camera system required to have a high time resolution for crash tests on cars and the moment of impact of a ball hit by a baseball batter, for example, requires an output of 100 to 1000 images per second and, thus, a high-speed output.

Thus, conventionally, the number of output terminals is increased to provide hundreds of output terminals, whereby video signals are outputted in parallel.

Such a configuration in which output terminals are simply provided in parallel with each other, however, has a large number of output terminals, thus leading to an increase in area and cost of the solid-state image pickup device.

An IC in a next stage also is increased in size with an increased number of input terminals. As a result, various problems occur, such as difficulty in implementation, difficulty in reducing the size of the camera, difficulty in synchronizing many output signals, difficulty in output at high clock speeds because of the problem of synchronization, and the like.

On the other hand, to reduce the number of output terminals requires an increase in the clock speed. When the clock speed is increased, however, the time of charging and discharging a capacitance of a path to the IC in the next stage cannot be ignored, and waveforms are blunted. In the worst case, signals do not reach a high/low level of the IC in the next stage, and consequently the IC in the next stage cannot recognize the signals.

Such a problem occurs not only when the clock speed is to be increased but also when the capacitance in a signal path is increased for some reason, for example, because the path to the IC in the next stage is desired to be lengthened for use in an endoscope.

Further, output at a high clock speed causes undesired radiation to be emitted from the signal path between the solid-state image pickup device and the IC in the next stage and, thus, affects operation of other electronic apparatuses and the solid-state image pickup device itself. Audio/video apparatuses, for example, cause degradation in sound quality/picture quality.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a solid-state image pickup device and an output method thereof that can realize the super-high speed of video signals and reduce undesired radiation.

In order to achieve the above object, according to an aspect of the present invention, there is provided a solid-state image pickup device comprising: an image pickup pixel unit including a plurality of pixels; a signal processing unit for subjecting a video signal outputted from the image pickup pixel unit to predetermined signal processing; and an output buffer unit for outputting the video signal processed by the signal processing unit, wherein the output buffer unit outputs the video signal and an inverted video signal obtained by inverting the video signal.

Further, according to another aspect of the present invention, there is provided an output method of a solid-state image pickup device, the solid-state image pickup device including: an image pickup pixel unit including a plurality of pixels; a signal processing unit for subjecting a video signal outputted from the image pickup pixel unit to predetermined signal processing; and an output buffer unit for outputting the video signal processed by the signal processing unit, and the output method comprises: outputting the video signal and an inverted video signal obtained by inverting the video signal from the output buffer unit.

The solid-state image pickup device according to the present invention outputs the video signal and the inverted video signal of the video signal from the output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize the super-high speed of video signals.

Further, the output method according to the present invention outputs the video signal and the inverted video signal of the video signal from the output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it, is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize the super-high speed of video signals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of an outline of a solid-state image pickup device according to a first embodiment of the present invention;

FIG. **2** is a circuit diagram of an outline of a unit pixel of the solid-state image pickup device shown in FIG. **1**;

FIGS. **3**A, **3**B, **3**C, and **3**D are timing charts showing signal waveforms in an output stage of the solid-state image pickup device shown in FIG. **1**;

FIG. **4** is a block diagram showing an example of a connection between the solid-state image pickup device shown in FIG. **1** and an IC in a next stage;

FIG. **5** is a block diagram showing a configuration of an output buffer unit in a solid-state image pickup device according to a second embodiment of the present invention;

FIGS. **6**A, **6**B, **6**C, and **6**D are timing charts showing signal waveforms in an output stage of the solid-state image pickup device shown in FIG. **5**;

FIG. **7** is a plan view of an outline of a solid-state image pickup device according to a third embodiment of the present invention; and

FIG. **8** is a circuit diagram showing an example of a configuration of a differential output amplifier provided in the solid-state image pickup device shown in FIG. **7**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of a solid-state image pickup device and an output method thereof according to the present invention will hereinafter be described.

The output methods of the solid-state image pickup devices according to the embodiments use a differential output configuration and an IC in a next stage that uses a differential-amplifier configuration for input, whereby a super-high speed of a video signal is realized while controlling an increase in clock speed. It is thereby possible to alleviate the problem of undesired radiation and to reduce the number of output terminals by serial output. Further, as later described, it is more desirable to use a strobe signal output.

Concrete examples of the present invention will be described hereinafter.

FIG. **1** is a plan view of an outline of a solid-state image pickup device according to a first embodiment of the present invention, showing the main components necessary for a description of the solid-state image pickup device as a whole according to the first embodiment.

The solid-state image pickup device according to the first embodiment is specifically a CMOS-type image sensor. The solid-state image pickup device according to the first embodiment includes an image pickup pixel unit **12**, V-selection means **14**, H-selection means **16**, a timing generator (TG) **18**, a CDS and PGA unit **20**, an A/D unit **22**, a constant current unit **24**, a horizontal bus line **26**, an output buffer unit **28**, a communication unit **30** and the like, which are formed on a semiconductor chip **10**.

The image pickup pixel unit **12** has a large number of pixels arranged in the form of a two-dimensional matrix. As shown in FIG. **2**, each of the pixels includes a photodiode **122**, serving as a photoelectric converting device for generating a signal charge corresponding to an amount of light received and storing the signal charge, and MOS transistors, such as a transfer transistor **126**, for transferring the signal charge converted and stored by the photodiode **122** to a floating diffusion part (FD part) **124**, a reset transistor **128** for resetting a potential of the FD part **124**, an amplifying transistor **130** for outputting an output signal corresponding to the potential of the FD part **124**, and an address transistor **131** for selecting a pixel.

Further, the image pickup pixel unit **12** has various driving wirings **132** and **134** arranged in a horizontal direction for driving and controlling the MOS transistors. The pixels of the image pickup pixel unit **12** are sequentially selected in units of a horizontal line (pixel row) in a vertical direction by the V-selection means **14**. The MOS transistors of each of the pixels are controlled by various pulse signals from the timing generator **18**. Thereby, a signal of each of the pixels is outputted to the CDS and PGA unit **20** via a vertical signal line for each pixel column.

The CDS and PGA unit **20** has a CDS and PGA circuit for each pixel column of the image pickup pixel unit **12**. The CDS and PGA unit **20** subjects a pixel signal read from each pixel column of the image pickup pixel unit **12** to signal processing, such as CDS (correlated double sampling) and PGA (programmable gain control), and then outputs a resulting pixel signal to the A/D unit **22**.

The A/D unit **22** has an A/D conversion circuit for each pixel column of the image pickup pixel unit **12**. The A/D unit **22** converts the pixel signal of each pixel column from the CDS and PGA unit **20** from analog signal form to digital signal form and then outputs the result.

The H-selection means **16** selects digital signal outputs from the A/D unit **22** in a horizontal direction and then outputs the digital signal outputs to the horizontal bus line **26**. It is to be noted that the first embodiment adopts 10-bit output and has ten horizontal bus lines **26**.

The constant current unit **24** supplies the image pickup pixel unit **12** as described above with a constant current for each pixel column.

The timing generator **18** supplies parts other than the pixels of the image pickup pixel unit **12** as described above with various timing signals.

The output buffer unit **28** outputs a digital signal supplied thereto from the horizontal bus line **26** to external terminals of the semiconductor chip **10**.

The communication unit **30** communicates with the outside of the semiconductor chip **10**. The communication unit **30** performs operations such as, for example, controlling an operating mode of the timing generator **18** and outputting parameters indicating the conditions of the semiconductor chip **10** to the outside.

In the above configuration of the first embodiment, the method of outputting a video signal by the output buffer unit **28** and a clock of the timing generator **18** constitutes main characteristic parts of the first embodiment.

First, the output buffer unit **28** in the first embodiment buffers and outputs a digital signal from the horizontal bus line **26**. At this time, in addition to the normal video signal, the output buffer unit **28** generates an inverted output of the normal video signal.

The normal video signal and the inverted output are outputted from a video signal output terminal **28**A and an inverted video signal output terminal **28**B, respectively, to the outside of the chip **10**.

It is to be noted that though omitted in FIG. **1**, the inverted video signal is formed by 10 bits so as to correspond to the video signal of 10 bits, and output terminals **28**A and **28**B total 20 (20 bits).

Next, the timing generator **18** supplies a clock (output clock) to the output buffer unit **28**. The clock is buffered by another output buffer unit **32**, and the clock and a clock obtained by inverting the clock are outputted to the outside from output terminals **32**A and **32**B, respectively.

FIGS. **3**A, **3**B, **3**C, and **3**D are timing charts showing signal waveforms in the first embodiment. FIG. **3**A shows the output clock; FIG. **3**B shows the inverted output clock; FIG. **3**C shows one video signal; and FIG. **3**D shows an inverted video signal corresponding to the video signal shown in FIG. **3**C.

In this case, the signals are changed at both a rising edge and a falling edge of the output clock, and 10 bits per pixel are outputted in half a clock cycle of the output clock.

FIG. **4** is a block diagram showing an example of a connection between the solid-state image pickup device (semiconductor chip **10**) and an IC **60** in a next stage.

The IC **60** in the next stage includes a signal processing circuit, a DSP (Digital Signal Processor) and the like for receiving the video signal and the inverted video signal and performing various kinds of signal processing. The IC **60** in the next stage has a differential amplifier in an input stage thereof, and it is therefore able to recognize even the input signals having waveforms blunted beyond a conventionally-allowable range. This enables a super-high speed of the system, an addition of capacitance to a signal path, or a reduction in the size of the output buffer of the solid-state image pickup device.

When the output signals are changed to a high and a low, charging and discharging current paths flow in the directions of arrows a and b shown in FIG. **4**, for example. However, the output and the inverted output cause currents to flow in opposite directions. Therefore, when the paths are disposed adjacent to each other, undesired radiations can be reduced by canceling each other. The above description of the video signals also applies to the output clocks.

It is to be noted that while the example shown in FIG. **1** is a CMOS-type image sensor as an example of a configuration of the solid-state image pickup device, the present invention is not limited to the above-described configuration, and it is similarly applicable to solid-state image pickup devices in general that output digital video signals.

A second embodiment of the present invention will be described next.

While the first embodiment described above has a total of 20 parallel terminals as video signal and inverted video signal output terminals, the second embodiment of the present invention has one video signal output terminal and one inverted video signal output terminal for output by time division. It is to be noted that as in the first embodiment described above, the second embodiment has ten horizontal bus lines.

FIG. **5** is a block diagram showing a configuration of an output buffer unit in the second embodiment.

As shown in FIG. **5**, in the second embodiment, a multiplexer **40** is provided between the horizontal bus lines **26** and the output buffer unit **28**.

The multiplexer **40** selects the horizontal bus lines **26** in appropriate timing. A signal of a selected horizontal bus line **26** is inputted to the output buffer unit **28**, buffered by the output buffer unit **28**, and then led to the video signal output terminal **28**A and the inverted-signal output terminal **28**B.

Thus, by outputting a 10-bit video signal to the outside of the chip with ten or more clocks, it is possible to reduce the number of output terminals as compared with the foregoing first embodiment. The reduction in the number of output terminals, therefore, makes it possible to miniaturize the solid-state image pickup device and a camera or the like using the solid-state image pickup device. Further, since the second embodiment has a total of two output terminals, it is easy to control a phase difference between output signals to within an allowable range, and it is thus easier to increase clock speed.

With such a configuration, it is desirable to output a strobe signal instead of the clock signal described above.

The strobe signal is inverted in timing in which the video signal is not inverted.

FIGS. **6**A, **6**B, **6**C, and **6**D are timing charts showing signal waveforms in the second embodiment. FIG. **6**A shows a strobe signal; FIG. **6**B shows an inverted strobe signal; FIG. **6**C shows one video signal; and FIG. **6**D shows an inverted video signal corresponding to the video signal shown in FIG. **6**C.

In this case, since either one of the video signal or the strobe signal is inverted, only a load of one of the signals is put on the device outputs in the timing of each clock, and the load is constant. By obtaining an exclusive disjunction of the strobe signal and the video signal, a clock can be reproduced in an IC in a next stage.

A third embodiment of the present invention will next be described.

FIG. **7** is a plan view of an outline of a solid-state image pickup device according to a third embodiment of the present invention, showing main components necessary for a description of the solid-state image pickup device as a whole according to the third embodiment.

The solid-state image pickup device according to the third embodiment is formed by omitting the A/D unit **22** shown in FIG. **1**, using a CDS unit **50** that omits a PGA unit in place of the CDS and PGA unit **20** shown in FIG. **1**, and using an analog differential output amplifier **52** in place of the output buffer unit **28** shown in FIG. **1**. The solid-state image pickup device according to the third embodiment thereby produces analog output.

Incidentally, the CDS unit **50** is the same as the CDS unit of the CDS and PGA unit **20**. The other parts are the same as in the example shown in FIG. **1**. Therefore, the other parts are identified by the same reference numerals as in FIG. **1**, and their description will be omitted.

In such a configuration, the differential-output amplifier **52** outputs a signal from a horizontal bus line **26** (horizontal signal line) to the outside of the chip. At this time, the differential-output amplifier **52** outputs the signal in the form of differential signals of an analog video signal and an inverted analog video signal.

FIG. **8** is a circuit diagram showing an example of a configuration of the differential-output amplifier **52**.

As shown in FIG. **8**, the differential-output amplifier **52** has a differential circuit with resistances R**1** and R**2** and MOS transistors Q**1** and Q**2** between a driving power supply Vd and a constant-current source **56**. The analog video signal and the inverted analog video signal mentioned above are outputted as an analog output **1** and an analog output **2** from a node of the resistance R**1** and the MOS transistor Q**1** and a node of the resistance R**2** and the MOS transistor Q**2**.

An input stage of the MOS transistors Q**1** and Q**2** is also of a differential type. The horizontal bus line **26** (horizontal signal line) is connected to a gate of one MOS transistor Q**2**, and a clamping voltage Vclp is applied to a gate of the other MOS transistor Q**1**.

A clamping switch **54** is inserted between the horizontal signal line **26** and the clamping voltage Vclp. The horizontal signal line **26** is reset to the clamping voltage Vclp via the clamping switch **54**.

After the clamping switch **54** is opened, a signal from the CDS unit **50** is put on the horizontal bus line **26**, and a difference between the signal and the clamping voltage Vclp is amplified and then outputted to the analog output **1** and the analog output **2**.

Incidentally, depending on the load setting, a two-stage configuration in which a differential amplifier with a higher driving capability is disposed in a succeeding stage may be used, or a configuration in which output is produced through a voltage follower may be used.

Such analog output inherently requires one video output terminal and is, therefore, advantageous for miniaturization of the device.

In this example, two outputs are required, but do not present a great problem in miniaturization of the device. Further, when one of the two analog outputs is at a high potential, the other is at a low potential. Thus, for the same reason described in the example of FIG. **3**, currents flowing through wirings to an IC in a next stage are in directions opposite to each other, and thereby undesired radiation is reduced. Further, less susceptibility to noise superimposed on paths to the IC in the next stage is obtained.

It is thereby possible to alleviate a problem associated with high-speed clock output, a problem associated with a long distance to the IC in the next stage, or a problem of the presence of an adjacent apparatus susceptible to radiation.

It is to be noted that while the example shown in FIG. **7** is also a CMOS-type image sensor as an example of a configuration of a solid-state image pickup device, the present invention is not limited to the above-described configuration and is similarly applicable to CCD-type solid-state image pickup devices and solid-state image pickup devices in general that output analog video signals.

As described above, a solid-state image pickup device according to the present invention outputs a video signal and an inverted video signal of the video signal from an output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize super-high speed video signals.

Further, an output method of a solid-state image pickup device according to the present invention outputs a video signal and an inverted video signal of the video signal from an output buffer unit. Therefore, by using a differential circuit in an input stage of a circuit in a next stage, it is possible to realize a configuration that enables even signals blunted to some degree to be detected reliably, and thereby to realize super-high speed of video signals.

In the foregoing first embodiment, in particular, a differential amplifier is used in the input stage of the IC in the next stage, and it is able to recognize even signals having blunter waveforms. This enables an increase in speed of the system, an addition of capacitance to signal paths, or a reduction in size of the output buffer unit of the solid-state image pickup device. When the output signals are changed, the charging and discharging currents of the paths flow in the directions of the arrows shown in FIG. **4**, for example. However, the output and the inverted output flow in opposite directions. Therefore, when the paths are disposed adjacent to each other, undesired radiations can be reduced by canceling each other.

Further, in addition to the effects of the first embodiment, the foregoing second embodiment makes it possible to reduce the number of output terminals. The reduction in the number of output terminals, therefore, makes it possible to miniaturize the solid-state image pickup device and a camera using the solid-state image pickup device. Further, since the second embodiment has two signal output terminals including an inverted signal output terminal, it is easy to control a phase difference between output signals to within an allowable range, and it is thus easier to increase clock speed.

Further, the foregoing third embodiment has the effect of alleviating the problem of undesired radiation and obtaining less susceptibility to noise superimposed on paths to an IC in a next stage.

What is claimed is:

1. A solid-state image pickup device comprising:

an image pickup pixel unit including a plurality of pixels;

an analog-to-digital converting unit configured to subject a pixel signal outputted from said image pickup pixel unit to predetermined signal processing; and an output buffer unit for outputting the pixel signal processed by said analog-to-digital converting unit;

wherein said output buffer unit outputs said pixel signal and an inverted pixel signal obtained by inverting said pixel signal, and

wherein said pixel signal and inverted pixel signal outputs of said output buffer unit are configured for connection to a next stage that is separate from the image pickup device.

2. A solid-state image pickup device as claimed in claim **1**, wherein said image pickup pixel unit, said analog-to-digital converting unit and said output buffer unit are formed on a same chip.

3. The solid-state image pickup device of claim **1**, wherein said pixel signal and inverted pixel signal outputs of said output buffer unit are configured to accommodate a cancellation of an undesired radiation from the paths of the pixel signal and the inverted pixel signal between the image pickup device and the next stage.

4. The solid-state image pickup device of claim **1**, wherein said image pickup device resides in a first chip and the next stage resides in a second chip that is outside the first chip.

5. A solid-state image pickup device comprising:

an image pickup pixel unit including a plurality of pixels;

a correlated double sampling unit configured to subject a pixel signal outputted from said image pickup pixel unit to predetermined signal processing; and

an output buffer unit for outputting the pixel signal processed by said correlated double sampling unit;

wherein said output buffer unit outputs said pixel signal and an inverted pixel signal obtained by inverting said pixel signal, and

wherein said pixel signal and inverted pixel signal outputs of said output buffer unit are configured for connection to a next stage that is separate from the image pickup device.

6. A solid-state image pickup device as claimed in claim **5**, wherein said image pickup pixel unit, said correlated double sampling unit and said output buffer are formed on a same chip.

7. The solid-state image pickup device of claim **5**, wherein said pixel signal and inverted pixel signal outputs of said output buffer unit are configured to accommodate a cancellation of an undesired radiation from the paths of the pixel signal and the inverted pixel signal between the image pickup device and the next stage.

8. The solid-state image pickup device of claim **5**, wherein said image pickup device resides in a first chip and the next stage resides in a second chip that is separate from the first chip.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

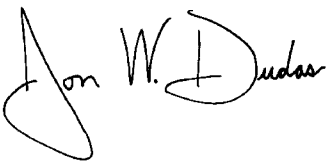
PATENT NO. : 7,304,287 B2
APPLICATION NO. : 11/600849
DATED : December 4, 2007
INVENTOR(S) : Keiji Mabuchi

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page
Item (54) should be read as follows:
--IMAGE PICKUP DEVICE WITH PIXEL SIGNAL AND INVERTED PIXEL SIGNAL OUTPUTS--

Signed and Sealed this

Twenty-ninth Day of April, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,304,287 B2
APPLICATION NO. : 11/600849
DATED : December 4, 2007
INVENTOR(S) : Keiji Mabuchi

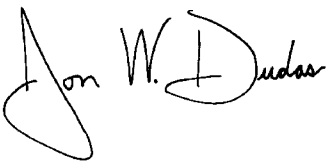
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page
Item (54) and Column 1, lines 1 and 2 should be read as follows:
--IMAGE PICKUP DEVICE WITH PIXEL SIGNAL AND INVERTED PIXEL SIGNAL OUTPUTS--

This certificate supersedes the Certificate of Correction issued April 29, 2008.

Signed and Sealed this

Twentieth Day of May, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

NOTICE OF ASSIGNMENT TO UNITED STATES MAGISTRATE JUDGE FOR DISCOVERY

This case has been assigned to District Judge James V. Selna and the assigned discovery Magistrate Judge is Arthur Nakazato.

The case number on all documents filed with the Court should read as follows:

SACV13- 546 JVS (ANx)

Pursuant to General Order 05-07 of the United States District Court for the Central District of California, the Magistrate Judge has been designated to hear discovery related motions.

All discovery related motions should be noticed on the calendar of the Magistrate Judge

---

NOTICE TO COUNSEL

A copy of this notice must be served with the summons and complaint on all defendants (if a removal action is filed, a copy of this notice must be served on all plaintiffs).

Subsequent documents must be filed at the following location:

[ ] **Western Division**
312 N. Spring St., Rm. G-8
Los Angeles, CA 90012

[ ] **Southern Division**
411 West Fourth St., Rm. 1-053
Santa Ana, CA 92701-4516

[ ] **Eastern Division**
3470 Twelfth St., Rm. 134
Riverside, CA 92501

Failure to file at the proper location will result in your documents being returned to you.

Victor M. Felix (Bar No. 179622)
Mathieu G. Blackston (Bar No. 241540)
PROCOPIO CORY, HARGREAVES & SAVITCH LLP
525 B Street, Suite 2200
San Diego, CA 92101
Telephone: (619) 238-1900
Facsimile: (619) 235-0398
Email: vmf@procopio.com; mgb@procopio.com

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

SONY CORPORATION, a Japanese corporation,

PLAINTIFF(S)

v.

RED.COM, INC., dba Red Digital Cinema, a Washington corporation,

DEFENDANT(S).

CASE NUMBER

SACV13-00546 JVS (ANx)

SUMMONS

TO: DEFENDANT(S):

A lawsuit has been filed against you.

Within 21 days after service of this summons on you (not counting the day you received it), you must serve on the plaintiff an answer to the attached complaint or a motion under Rule 12 of the Federal Rules of Civil Procedure. The answer or motion must be served on the plaintiff's attorney, Victor M. Felix, whose address is PROCOPIO CORY, HARGREAVES & SAVITCH LLP, 525 B Street, Suite 2200, San Diego, CA 92101. If you fail to do so, judgment by default will be entered against you for the relief demanded in the complaint. You also must file your answer or motion with the court.

Dated: APR - 5 2013

Clerk, U.S. District Court

By: A. Gonzal
Deputy Clerk

(Seal of the Court)

[Use 60 days if the defendant is the United States or a United States agency, or is an officer or employee of the United States. Allowed 60 days by Rule 12(a)(3)].

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

I. (a) PLAINTIFFS (Check box if you are representing yourself ☐)

SONY CORPORATION

DEFENDANTS (Check box if you are representing yourself ☐)

RED.COM, INC., dba Red Digital Cinema

(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.)

Victor M. Felix
PROCOPIO CORY, HARGREAVES & SAVITCH LLP
525 B Street, Suite 2200, San Diego, CA 92101 (619) 238-1900

(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.)

II. BASIS OF JURISDICTION (Place an X in one box only.)

- ☐ 1. U.S. Government Plaintiff
- ☒ 3. Federal Question (U.S. Government Not a Party)
- ☐ 2. U.S. Government Defendant
- ☐ 4. Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES-For Diversity Cases Only
(Place an X in one box for plaintiff and one for defendant)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business In this State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business In Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. ORIGIN (Place an X in one box only.)

☒ 1. Original Proceeding ☐ 2. Removed from State Court ☐ 3. Remanded from Appellate Court ☐ 4. Reinstated or Reopened ☐ 5. Transferred from Another District (Specify) ☐ 6. Multi-District Litigation

V. REQUESTED IN COMPLAINT: JURY DEMAND: ☒ Yes ☐ No (Check "Yes" only if demanded in complaint.)

CLASS ACTION under F.R.Cv.P. 23: ☐ Yes ☐ No ☐ **MONEY DEMANDED IN COMPLAINT:** $ _____

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write a brief statement of cause. Do not cite jurisdictional statutes unless diversity.)
35 U.S.C. § 271 et seq., Patent Infringement

VII. NATURE OF SUIT (Place an X in one box only).

OTHER STATUTES
- ☐ 375 False Claims Act
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce/ICC Rates/Etc.
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced & Corrupt Org.
- ☐ 480 Consumer Credit
- ☐ 490 Cable/Sat TV
- ☐ 850 Securities/Commodities/Exchange
- ☐ 890 Other Statutory Actions
- ☐ 891 Agricultural Acts
- ☐ 893 Environmental Matters
- ☐ 895 Freedom of Info. Act
- ☐ 896 Arbitration
- ☐ 899 Admin. Procedures Act/Review of Appeal of Agency Decision
- ☐ 950 Constitutionality of State Statutes

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loan (Excl. Vet.)
- ☐ 153 Recovery of Overpayment of Vet. Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability
- ☐ 196 Franchise

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment

REAL PROPERTY CONT.
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

TORTS
PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Fed. Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury
- ☐ 362 Personal Injury-Med Malpratice
- ☐ 365 Personal Injury-Product Liability
- ☐ 367 Health Care/ Pharmaceutical Personal Injury Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

IMMIGRATION
- ☐ 462 Naturalization Application
- ☐ 465 Other Immigration Actions

TORTS
PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth In Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

CIVIL RIGHTS
- ☐ 440 Other Civil Rights
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accomodations
- ☐ 445 American with Disabilities-Employment
- ☐ 446 American with Disabilities-Other
- ☐ 448 Education

PRISONER PETITIONS
Habeas Corpus:
- ☐ 463 Alien Detainee
- ☐ 510 Motions to Vacate Sentence
- ☐ 530 General
- ☐ 535 Death Penalty

Other:
- ☐ 540 Mandamus/Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition
- ☐ 560 Civil Detainee Conditions of Confinement

FORFEITURE/PENALTY
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 690 Other

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt. Relations
- ☐ 740 Railway Labor Act
- ☐ 751 Family and Medical Leave Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Employee Ret. Inc. Security Act

PROPERTY RIGHTS
- ☐ 820 Copyrights
- ☒ 830 Patent
- ☐ 840 Trademark

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405 (g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405 (g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS-Third Party 26 USC 7609

FOR OFFICE USE ONLY: Case Number: **SACV13-00546 JVS (ANx)**

AFTER COMPLETING PAGE 1 OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED ON PAGE 2.

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA

CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has this action been previously filed in this court and dismissed, remanded or closed? ☒ NO ☐ YES

If yes, list case number(s): _____

VIII(b). RELATED CASES: Have any cases been previously filed in this court that are related to the present case? ☒ NO ☐ YES

If yes, list case number(s): _____

Civil cases are deemed related if a previously filed case and the present case:

(Check all boxes that apply)
- ☐ A. Arise from the same or closely related transactions, happenings, or events; or
- ☐ B. Call for determination of the same or substantially related or similar questions of law and fact; or
- ☐ C. For other reasons would entail substantial duplication of labor if heard by different judges; or
- ☐ D. Involve the same patent, trademark or copyright, and one of the factors identified above in a, b or c also is present.

IX. VENUE: (When completing the following information, use an additional sheet if necessary.)

(a) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named plaintiff resides.

☐ Check here if the government, its agencies or employees is a named plaintiff. If this box is checked, go to item (b).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
	Japan

(b) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named defendant resides.

☐ Check here if the government, its agencies or employees is a named defendant. If this box is checked, go to item (c).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Orange	

(c) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** claim arose.
NOTE: In land condemnation cases, use the location of the tract of land involved.

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Orange	

***Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, or San Luis Obispo Counties**
Note: In land condemnation cases, use the location of the tract of land involved

X. SIGNATURE OF ATTORNEY (OR SELF-REPRESENTED LITIGANT): _____ DATE: April 5, 2013

Notice to Counsel/Parties: The CV-71 (JS-44) Civil Cover Sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law. This form, approved by the Judicial Conference of the United States in September 1974, is required pursuant to Local Rule 3-1 is not filed but is used by the Clerk of the Court for the purpose of statistics, venue and initiating the civil docket sheet. (For more detailed instructions, see separate instructions sheet).

Key to Statistical codes relating to Social Security Cases:

Nature of Suit Code	Abbreviation	Substantive Statement of Cause of Action
861	HIA	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405 (g))
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405 (g))
864	SSID	All claims for supplemental security income payments based upon disability filed under Title 16 of the Social Security Act, as amended.
865	RSI	All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405 (g))