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RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

DMR

SPANSION LLC,

Plaintiff,

v.

MACRONIX INTERNATIONAL CO., LTD.;
MACRONIX AMERICA, INC.;
ACER INC.;
ACER AMERICA CORPORATION;
ASUSTEK COMPUTER, INC.;
ASUS COMPUTER INTERNATIONAL;
BELKIN INTERNATIONAL, INC.,
D-LINK CORPORATION;
D-LINK SYSTEM, INC.;
NETGEAR INC;
NINTENDO CO., LTD.;
NINTENDO OF AMERICA, INC.

Defendants.

CASE NO.: CV13-03566

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff, Spansion LLC ("Spansion"), for its Complaint against Defendants Macronix International Co., Ltd. and Macronix America, Inc. ("Macronix Defendants"); Acer Inc. and Acer America Corporation ("Acer Defendants"); ASUSTek Computer Inc. and Asus Computer International (America) ("Asus Defendants"); Belkin International, Inc. ("Belkin"); D-Link Corporation and D-Link System, Inc ("D-Link Defendants"); Netgear Inc. ("Netgear"); and Nintendo Co., Ltd. and Nintendo of America, Inc. ("Nintendo Defendants") (collectively, "Defendants"), upon personal knowledge as to its own actions and upon information and belief as to actions by others, hereby alleges as follows:

INTRODUCTION

1. This is an action for patent infringement brought before this Court pursuant to 28 U.S.C. §§ 1331 and 1338(a). Spansion seeks remedies for Defendants' infringement of one or more claims of U.S. Patent Nos. 6,369,416 ("the '416 Patent"); 6,459,625 ("the '625 Patent"); 6,731,536 ("the '536 Patent"); 6,900,124 ("the '124 Patent"); 7,018,922 ("the '922 Patent"); and 7,151,027 ("the '027 Patent") (collectively, the "Spansion Patents"). True and correct copies of the Spansion Patents are attached hereto as Exhibits A through F.

PARTIES

2. Spansion LLC is a wholly owned operating subsidiary company of Spansion, Inc. Spansion LLC is incorporated in Delaware and its headquarters are located at 915 DeGuigne Drive, Sunnyvale, CA 94085. Spansion LLC is the owner of the Spansion Patents.

3. Upon information and belief, Macronix International Co., Ltd.. is a corporation organized under the laws of Taiwan, having its principal place of business at No. 16, Li-Hsin Road, Science Park, Hsin-chu, Taiwan, Republic of China. Macronix International Co., Ltd. makes, uses, sells, offers to sell, and imports flash memory chips that infringe the Spansion Patents ("Macronix Chips") in this District.

4. Upon information and belief, Macronix America, Inc. is a corporation organized under the laws of the State of California, having its principal place of business at 680 North

McCarthy Blvd., Suite 200, Milpitas, CA 95035. Macronix America, Inc. uses, sells, offers to sell, and imports flash memory chips that infringe the Spansion Patents in this District.

5. Upon information and belief, Acer Inc. is a corporation organized under the laws of Taiwan and has its principal place of business at 8F, 88, Sec. 1, Xintai 5th Rod., Xizhi, New Taipei City 221, Taiwan, Republic of China. Acer Inc. sells its products, including those that contain Macronix Chips, in this District.

6. Upon information and belief, Acer America Corporation is a corporation organized under the laws of the State of California and has its principal place of business at 333 West San Carlos Street, Suite 1500, San Jose, CA 95110. Acer America Corporation sells its products, including those that contain Macronix Chips, in this District.

7. Upon information and belief, ASUSTek Computer Inc. is a corporation organized under the laws of Taiwan and has its principal place of business at No. 15, Li-Te Rd., Beitou District, Taipei 112, Taiwan, Republic of China. ASUSTek Computer Inc. sells its products, including those that contain Macronix chips, in this District.

8. Upon information and belief, Asus Computer International (America) is a corporation organized under the laws of the State of California and has its principal place of business at 800 Corporate Way, Fremont, CA 94539. Asus Computer International (America) sells its products, including those that contain Macronix chips, in this District.

9. Upon information and belief, Belkin is a corporation organized under the laws of the State of California and has its principal place of business at 12045 E. Waterfront Drive, Playa Vista, CA 90094. Belkin sells its products, including those that contain Macronix chips, in this District.

10. Upon information and belief, D-Link Corporation is a corporation organized under the laws of Taiwan and has its principal place of business at No. 289, Sinhu 3rd Road, Neihu District, Taipei City, 114 Taiwan, Republic of China. D-Link sells its products, including those that contain Macronix chips, in this District.

11. Upon information and belief, D-Link System, Inc. is a corporation organized under the laws of the State of California and has its principal place of business at 17595 Mt. Herrmann

Street, Fountain Valley, CA 92708. D-Link System, Inc. sells its products, including those that contain Macronix chips, in this District.

12. Upon information and belief, Netgear is a corporation organized under the laws of the State of Delaware and has its principal place of business at 350 East Plumeria Drive, San Jose, CA 95134. Netgear sells its products, including those that contain Macronix chips, in this District.

13. Upon information and belief, Nintendo Co., Ltd. is a corporation organized under the laws of Japan and has its principal place of business at 11-1 Kamitobo-hokotate-cho, Minami-ku, Kyoto, Japan. Nintendo Co., Ltd. sells its products, including those that contain Macronix chips, in this District.

14. Upon information and belief, Nintendo of America, Inc. is a corporation organized under the laws of the State of Washington and has its principal place of business at 4600 150th Avenue NE, Redmond, WA 98052. Nintendo sells its products, including those that contain Macronix chips, in this District.

JURISDICTION AND VENUE

15. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has exclusive subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

16. This Court has personal jurisdiction over Defendants for at least the following reasons: (i) on information and belief, Defendants have committed acts of patent infringement, and/or contributed to or induced acts of patent infringement by others, in this District and elsewhere in California and the United States; (ii) Defendants regularly do business, solicits business, engages in other persistent courses of conduct, and/or derives substantial revenue from products and/or services provided to individuals in this District and in this State; (iii) Defendants have purposefully established substantial, systematic, and continuous contacts with this District and expects or should reasonably expect to be sued here; (iv) and, for Defendants Macronix America, Inc., Acer America Corporation, Asus Computer International (America), Belkin, and Netgear, each has its principal place of business in the Northern District of California.

17. Venue is proper in this District under 28 U.S.C. §§ 1391(b) and (c) and 1400(b) because Defendants transact business in this District, is subject to personal jurisdiction in this District, and has committed acts of infringement in this District.

INTRADISTRICT ASSIGMENT

18. This is an Intellectual Property Action to be assigned on a district-wide basis pursuant to Civil Local Rule 3-2(c).

BACKGROUND

19. Sunnyvale-based Spansion is a leading provider of the flash memory technology at the heart of the world's electronics systems. It is one of the largest companies in the world dedicated to designing, developing, manufacturing, marketing, and selling flash memory solutions. It is also one of the last major manufacturers of flash memory remaining in the United States and has over $900 million in net sales each year.

20. Spansion designs, develops, manufactures, markets, licenses, and sells flash memory technology and solutions for retail, commercial, and institutional customers worldwide. Its flash memory products primarily store data and software code for microprocessors, controllers and other programmable semiconductors which run applications in a broad range of electronics systems. These electronic systems include, for example, computing and communications, automotive and industrial, consumer and gaming, wireless and machine-to-machine devices.

21. Spansion devotes substantial resources to its highly sophisticated research and development program in the United States, and as a result, is a leading innovator in the flash memory technology industry. For example, Spansion has developed a revolutionary charge trapping MirrorBit® flash memory technology, which is designed to provide better manufacturability and scalability than floating-gate technology. Charge trapping technology, including Spansion's MirrorBit® technology, is widely described as the next generation of flash memory. Spansion has also developed various technologies that make flash memory manufacturing more efficient and help increase the density and capacity of flash memory devices.

22. Spansion's ability to compete and its success as a company depend on its ability to innovate and to protect these innovations. To that end, Spansion spends significant sums on research and development each year relating to products protected by the Spansion Patents. Spansion has made significant investments in the manufacture of products covered by its patents here in this District.

23. Spansion's ability to compete also depends on protecting its inventions through patents. Spansion's long-term financial success depends, in significant part, on its ability to establish, maintain, and protect its proprietary technology through enforcement of its patent rights. That ability has been significantly compromised by the acts complained of in this Complaint.

ASSERTED PATENTS

24. Spansion is the owner by assignment of all rights, title, and interest in the Spansion Patents, including the right to bring this suit for injunctive relief and damages.

25. The '416 Patent, titled "Semiconductor Device with Contacts Having a Sloped Profile," was duly and legally issued by the United States Patent and Trademark Office on April 9, 2002.

26. The '124 Patent, titled "Patterning for Elliptical V_{ss} Contact on Flash Memory," was duly and legally issued by the United States Patent and Trademark Office on May 31, 2005.

27. The '922 Patent, titled "Patterning for Elongated V_{ss} Contact Flash Memory," was duly and legally issued by the United States Patent and Trademark Office on September 3, 2023.

28. The '625 Patent, titled "Three Metal Process for Optimizing Layout Density," was duly and legally issued by the United States Patent and Trademark Office on October 1, 2002.

29. The '027 Patent, titled "Method and Device for Reducing Interface Area of a Memory Device," was duly and legally issued by the United States Patent and Trademark Office on December 19, 2006.

30. The '536 Patent, titled "Password and Dynamic Protection of Flash Memory Data," was duly and legally issued by the United States Patent and Trademark Office on May 4, 2004.

RELATED PROCEEDINGS

31. This Complaint is being filed concurrently with a complaint under Section 337 of the Tariff Act of 1930, as amended 19 U.S.C. § 1337 ("Section 337") with the United States International Trade Commission.

COUNT I

(INFRINGEMENT OF THE '416 PATENT)

32. Plaintiff incorporates by reference paragraphs 1 through 27 above as if fully set forth herein.

Macronix

33. The Macronix Defendants have infringed, and continue to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '416 patent, including, but not limited to its XtraROM Family of Chips, its NOR Flash Generation F chips, its NOR Flash Generation E chips, its NOR Flash Generation D chips, and its NOR Flash Generation C chips.

34. The Macronix Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Acer

35. The Acer Defendants have infringed, and continue to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Acer Aspire V5 laptop computer.

36. The Acer Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is

entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Asus

37. The Asus Defendants have infringed, and continue to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Asus RT-AC66U, Asus RT-N56U, Asus RT-N16, and Asus RT-N12 routers.

38. The Asus Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Belkin

39. Defendant Belkin has infringed, and continues to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Belkin N600 DB router.

40. Belkin's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

D-Link

41. The D-Link Defendants have infringed, and continue to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the D-Link DIR-655 Xtreme N Gigabit Router.

42. The D-Link Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Netgear

43. Defendant Netgear has infringed, and continues to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Netgear WNR1000 router.

44. Netgear's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Nintendo

45. The Nintendo Defendants have infringed, and continue to infringe, the '416 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Nintendo Wii U, and Nintendo 3DS Game Cartridges.

46. The Nintendo Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT II

(INFRINGEMENT OF THE '124 PATENT)

47. Plaintiff incorporates by reference paragraphs 1 through 27 above as if fully set forth herein.

Macronix

48. The Macronix Defendants have infringed, and continue to infringe, the '124 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '124 patent, including, but not limited to its XtraROM Family of Chips.

49. The Macronix Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Nintendo

50. The Nintendo Defendants have infringed, and continue to infringe, the '124 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to Nintendo 3DS Game Cartridges.

51. The Nintendo Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT III

(INFRINGEMENT OF THE '922 PATENT)

52. Plaintiff incorporates by reference paragraphs 1 through 27 above as if fully set forth herein.

Macronix

53. The Macronix Defendants have infringed, and continue to infringe, the '922 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '922 patent, including, but not limited to its XtraROM Family of Chips.

54. The Macronix Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Nintendo

55. The Nintendo Defendants have infringed, and continue to infringe, the '922 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to Nintendo 3DS Game Cartridges.

56. Nintendo's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT IV

(INFRINGEMENT OF THE '625 PATENT)

57. Plaintiff incorporates by reference paragraphs 1 through 27 above as if fully set forth herein.

Macronix

58. The Macronix Defendants have infringed, and continue to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '625 patent, including, but not limited to its NOR Flash Generation F chips, its NOR Flash Generation E chips, its NOR Flash Generation D chips, and its NOR Flash Generation C chips.

59. The Macronix Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Acer

60. The Acer Defendants have infringed, and continue to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Acer Aspire V5 laptop computer.

61. The Acer Defendants' infringing activities infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Asus

62. The Asus Defendants have infringed, and continue to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Asus RT-AC66U, Asus RT-N56U, Asus RT-N16, and Asus RT-N12 routers.

63. The Asus Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Belkin

64. Defendant Belkin has infringed, and continues to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Belkin N600 DB router.

65. Belkin's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

D-Link

66. The D-Link Defendants have infringed, and continue to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the D-Link DIR-655 Xtreme N Gigabit Router.

67. The D-Link Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Netgear

68. Defendant Netgear has infringed, and continues to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the

United States, electronic devices that contain Macronix Chips, including, but not limited to the Netgear WNR1000 router.

69. Netgear's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Nintendo

70. The Nintendo Defendants have infringed, and continue to infringe, the '625 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Nintendo Wii U, and Nintendo 3DS Game Cartridges.

71. The Nintendo Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT V

(INFRINGEMENT OF THE '027 PATENT)

72. Plaintiff incorporates by reference paragraphs 1 through 27 above as if fully set forth herein.

Macronix

73. The Macronix Defendants have infringed, and continue to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '027 patent, including, but not limited to its NOR Flash Generation F chips, its NOR Flash Generation E chips, and its NOR Flash Generation D chips.

74. The Macronix Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Acer

75. The Acer Defendants have infringed, and continue to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Acer Aspire V5 laptop computer.

76. The Acer Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Asus

77. The Asus Defendants have infringed, and continue to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Asus RT-AC66U, Asus RT-N56U, Asus RT-N16, and Asus RT-N12 routers.

78. The Asus Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Belkin

79. Defendant Belkin has infringed, and continues to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Belkin N600 DB router.

80. Belkin's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

D-Link

81. The D-Link Defendants have infringed, and continue to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the D-Link DIR-655 Xtreme N Gigabit Router.

82. The D-Link Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Netgear

83. Defendant Netgear has infringed, and continues to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain Macronix Chips, including, but not limited to the Netgear WNR1000 router.

84. Netgear's infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for

which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Nintendo

85. The Nintendo Defendants have infringed, and continue to infringe, the '027 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Nintendo Wii U, and Nintendo 3DS Game Cartridges.

86. The Nintendo Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

COUNT VI

(INFRINGEMENT OF THE '536 PATENT)

87. Plaintiff incorporates by reference paragraphs 1 through 27 above as if fully set forth herein.

Macronix

88. The Macronix Defendants have infringed, and continue to infringe, the '536 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, products that practice the inventions claimed in the '536 patent, including, but not limited to its NOR Flash Generation F chips and its NOR Flash Generation E chips.

89. The Macronix Defendants have been, and continue to actively induce and encourage infringement the '536 Patent. With actual knowledge of the '536 Patent at least as of the date of this Complaint, Macronix actively induces and encourages its customers' direct infringement of the '536 Patent by selling or using its Macronix Chips, including those identified above and herein. Specifically, Macronix's datasheets teach others to use the Advanced Sector Protection features of their chips. In addition, Macronix's own product literature, marketing, sales and other materials

instruct customers to use its own chips instead of Spansion's chips that practice that Spansion Patents. For example, Macronix's website provides customers and potential customers with product specifications, technical papers, and "Application Notes" that describe how its chips perform identical functions as Spansion's chips, and instruct customers how to use a Macronix Chip instead of a Spansion Chip in a given application. Macronix does this with specific intent to induce and encourage such infringement, or at a minimum with willful blindness to the known risk of such infringement.

90. The Macronix Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

Asus

91. The Asus Defendants have infringed, and continue to infringe, the '536 Patent by making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips, including, but not limited to the Asus RT-N16 router.

92. The Asus Defendants' infringing activities have caused and will cause Spansion irreparable harm for which there is no adequate remedy at law and damages in an amount yet to be determined for which Spansion is entitled to relief. Under 35 U.S.C. §§ 283 and 284, Spansion is entitled to recover damages, as well as permanent injunctive relief against further infringing activity.

PRAYER FOR RELIEF

WHEREFORE, Spansion respectfully requests that:

A. Entry of a judgment that Defendants have infringed, directly and indirectly, one or more claims of the Spansion Patents;

B. A judgment and order permanently enjoining the Macronix Defendants, and the directors, officers, agents, servants and employees of each of the Macronix Defendants, and those acting in active concert or participation with the Macronix Defendants from infringing, directly, or indirectly, the Spansion Patents;

C. A judgment and order permanently enjoining the Defendants and each Defendant's parent corporations, subsidiaries, and affiliates from making, using, offering for sale, and selling within the United States, and/or importing into the United States, electronic devices that contain infringing Macronix Chips;

D. Damages to compensate Spansion for Defendants' infringement, including all compensatory damages incurred in this case, including all pre-judgment and post-judgment interest and enhanced damages;

E. An award of reasonable attorneys' fees under 35 U.S.C. § 285

F. Such other and further relief as this Court may deem just and proper.

DATED: August 1, 2013

SKADDEN, ARPS, SLATE, MEAGHER & FLOM, LLP

By: _____
Andrew Thomases

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DEMAND FOR JURY TRIAL

Plaintiff Spansion LLC demands a trial by jury pursuant to Rule 38(b) of the Federal Rules of Civil Procedure.

DATED: August 1, 2013

SKADDEN, ARPS, SLATE, MEAGHER & FLOM, LLP

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Attorneys for PLAINTIFF
SPANSION LLC

US006369416B1

(12) **United States Patent**
Hui et al.

(10) **Patent No.: US 6,369,416 B1**
(45) **Date of Patent: Apr. 9, 2002**

(54) **SEMICONDUCTOR DEVICE WITH CONTACTS HAVING A SLOPED PROFILE**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/404,394**

(22) Filed: **Sep. 23, 1999**

(51) **Int. Cl.**[7] **H01L 29/76**

(52) **U.S. Cl.** **257/288**; 257/296; 257/306; 257/315; 257/368; 257/390

(58) **Field of Search** 257/288, 368, 257/369, 296, 306, 307, 308, 309, 310, 390, 315

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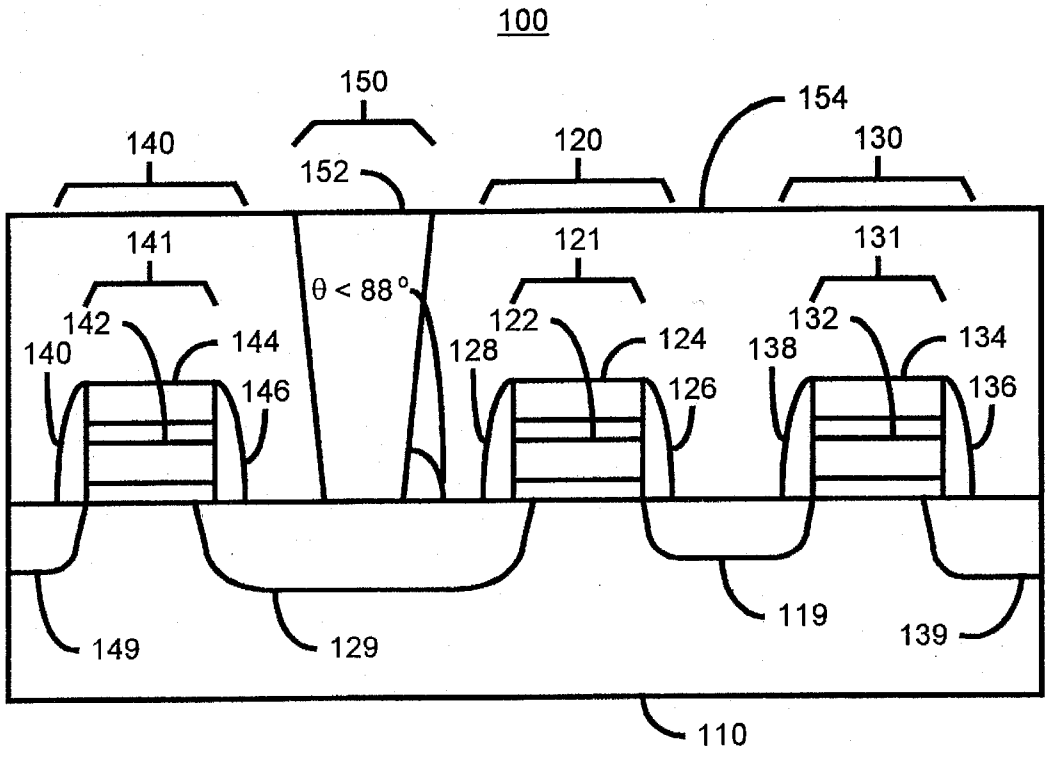
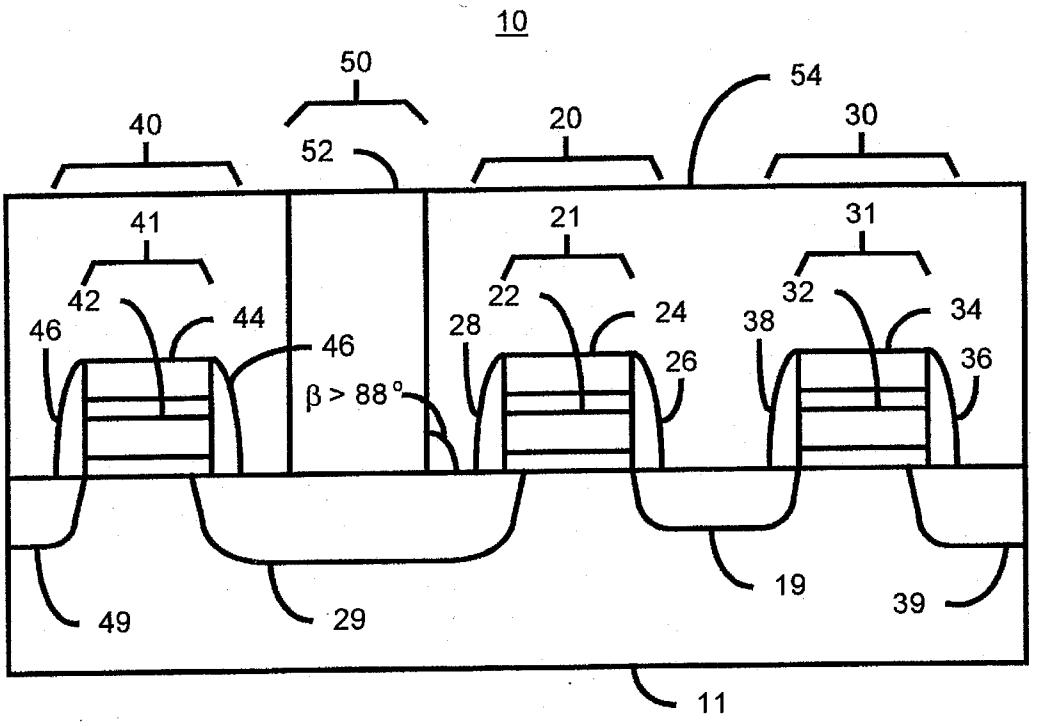
(57) **ABSTRACT**

A method and system for providing a contact in a semiconductor device including a plurality of gates is disclosed. The method and system include providing an insulating layer substantially surrounding at least a portion of the plurality of gates and providing at least one contact within the insulating layer. The contact has a side defining a sloped profile. The sloped profile includes an angle between the side of the contact and a surface of the substrate that is less than approximately eighty-eight degrees.

4 Claims, 4 Drawing Sheets





Prior Art

Figure 1

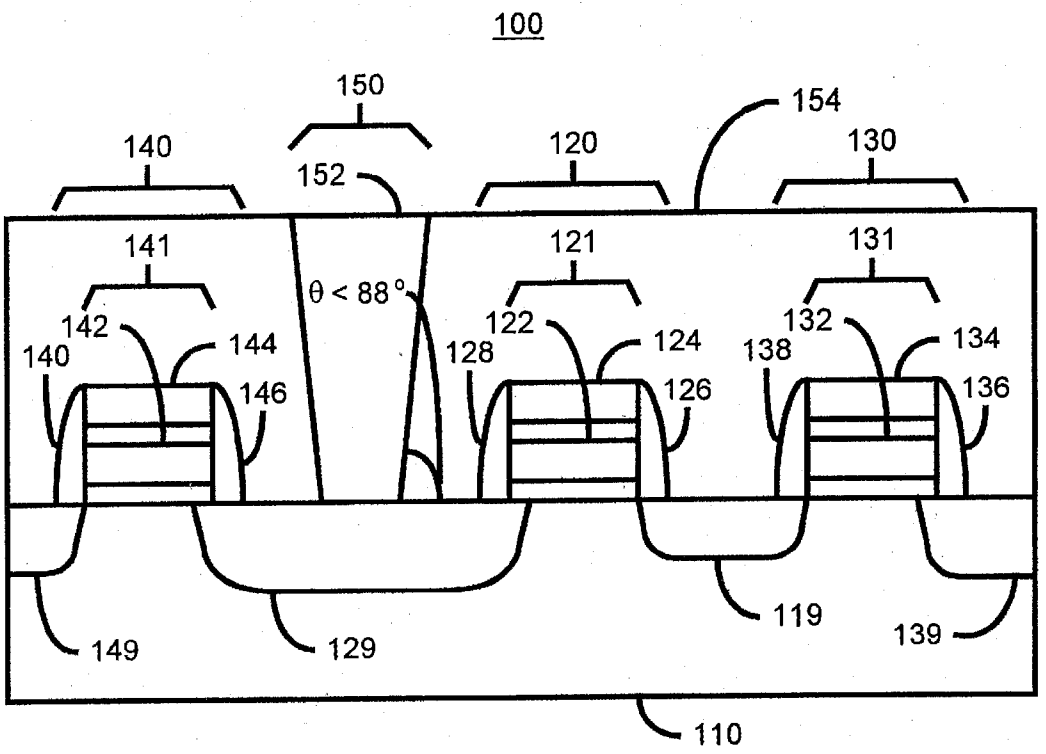

100
150
154
140
120
130
152
141
121
131
θ < 88°
142
122
132
144
124
134
140
128
138
146
126
136
119
149
129
139
110

Figure 2

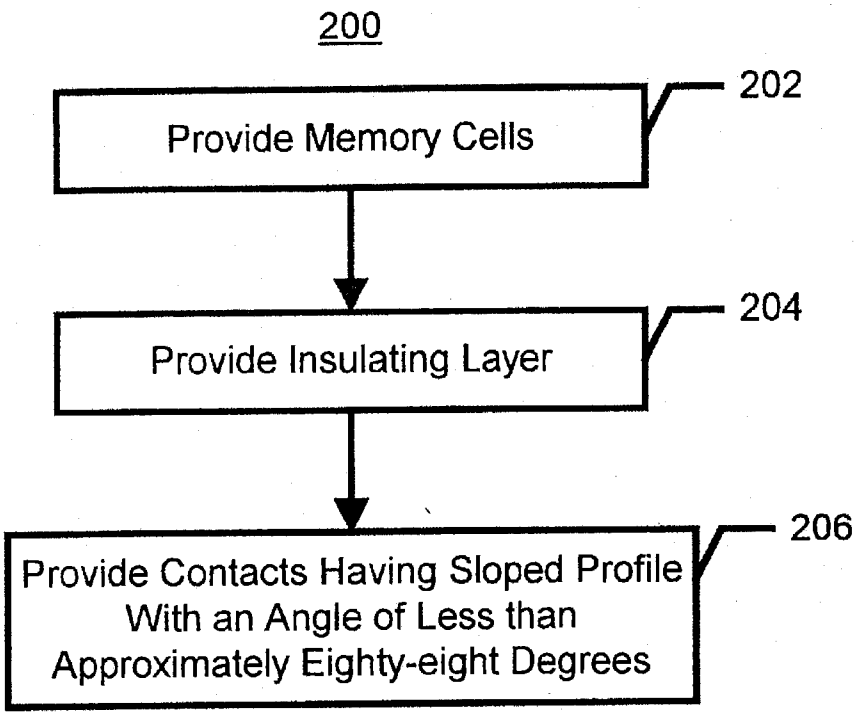


Figure 3A

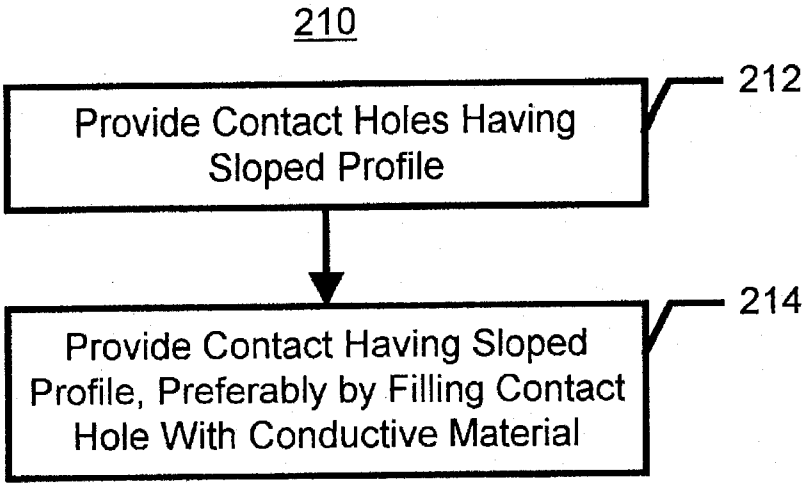


Figure 3B

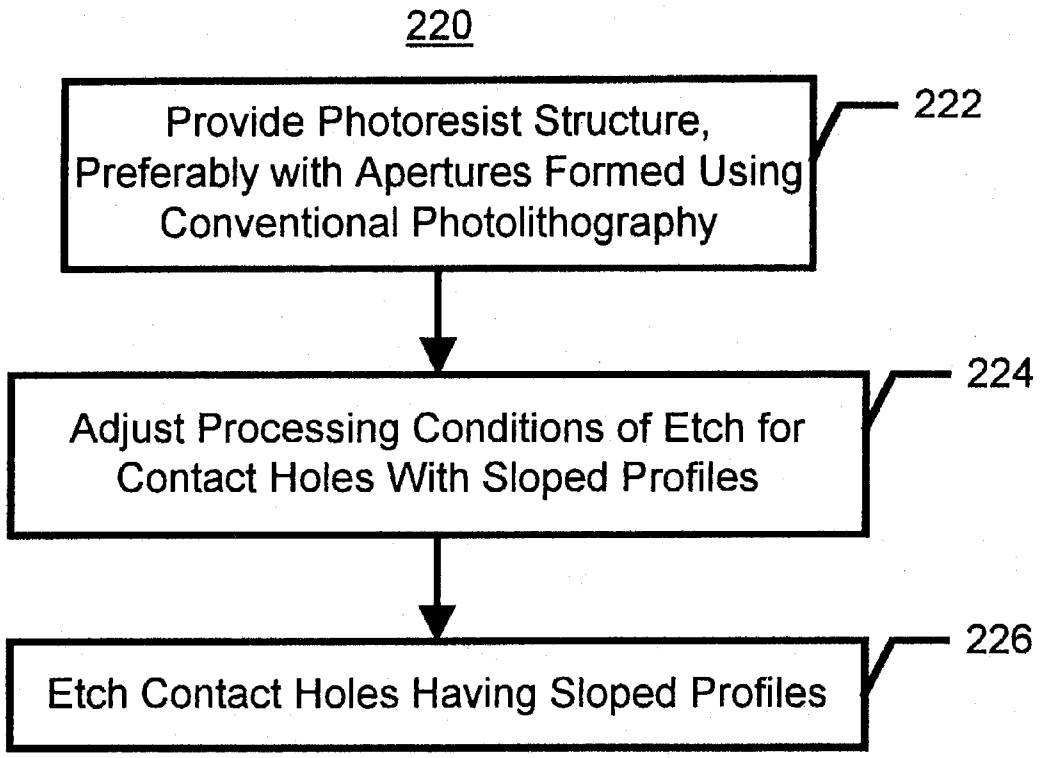

220
Provide Photoresist Structure, Preferably with Apertures Formed Using Conventional Photolithography
222
Adjust Processing Conditions of Etch for Contact Holes With Sloped Profiles
224
Etch Contact Holes Having Sloped Profiles
226

Figure 3C

SEMICONDUCTOR DEVICE WITH CONTACTS HAVING A SLOPED PROFILE

FIELD OF THE INVENTION

The present invention relates to semiconductor devices, more particularly to a method and system for reducing charge gain and charge loss due to contacts in semiconductor devices, such as a flash memory device.

BACKGROUND OF THE INVENTION

A conventional semiconductor device, such as a memory, includes a large number of cells, which are typically floating gate devices such as floating gate transistors. For example, FIG. **1** depicts a portion of a conventional semiconductor device **10**. The semiconductor device **10** includes cells **20**, **30**, and **40** formed on a substrate **11**. Each cell includes a gate stack **21**, **31** and **41**. Each gate stack **21**, **31** and **41** includes a floating gate **22**, **32** and **42**, respectively, and a control gate **24**, **34** and **44**, respectively. The cells **20**, **30** and **40** also include drains **29** and **39** and sources **19** and **49**. As depicted in FIG. **1**, the cells **20** and **40** share a common drain **29**, while the cells **20** and **30** share a common source **19**. Typically, each cell **20**, **30** and **40** also includes spacers **26** and **28**, **36** and **38**, and **46** and **48**, respectively.

In order to make electrical contact to one or more of the cells **20**, **30** and **40**, a conventional electrical contact **52** is provided. The conventional contact **52** is provided within a conventional contact hole **50**. The conventional contact hole **50** is provided in an insulating layer **54** which otherwise covers the cells **20**, **30** and **40**. The insulating layer **54** insulates the cells **20**, **30** and **40**. The conventional contact hole **50** is filled with a conductive material to form the conventional contact **52**.

Although the conventional semiconductor device **10** functions, one of ordinary skill in the art will readily realize that the conventional semiconductor device **10** is subject to unanticipated charge gain and charge loss because of the spacing of the contact **52** from a particular cell, such as the cell **20**. The current trend in semiconductor technology is toward higher densities. In order to reduce the space occupied by a given conventional semiconductor device **10**, the components of the semiconductor device are more densely packed and made smaller. Thus, the cells **20**, **30** and **40** and the conventional contact **52** are relatively close. The thickness of the spacers **26** and **28**, **36** and **38** and **46** and **48** is between approximately one thousand and two thousand Angstroms. The conventional contact **52** is approximately 0.2 to 0.4 μm wide. This distance is approximately the smallest that an aperture in a photoresist mask (not shown) can be made. The photoresist mask is used to form the conventional contact hole **50**. The sides of the conventional contact hole **50** and, therefore, the sides of the conventional contact **52** are also almost perpendicular to the surface of the substrate **11**. For example, the conventional contact hole **50** is typically formed so that the edges make an angle, β, of greater than eighty-eight degrees. Thus, the top of the contact **52** is approximately directly above the bottom of the contact **52**. The conventional contact **52** is also closely spaced to neighboring cells **20**, **30** and **40**. In particular, the distance between the base of the conventional contact **52** and the edge of a nearest gate in a gate stack, such as the gate stack **21**, is very small.

The small spacing between the conventional contact **52** and the gate stack of a particular cell, such as the cell **20**, causes unanticipated charge gain and charge loss from the cell **20**. Because the conventional contact **52** is typically

separated from the edge of the gate stack **21** by such a small distance, the portion of the insulating layer **54** between the conventional contact **52** and the gate stack **21** is very thin. The combination of the spacer **28** and the insulating layer **54** may not provide sufficient insulation to prevent the gate stack **32** from being electrically coupled to the conventional contact **52** through the spacer **28** and insulating layer **54**. For example, charge on the conventional contact **52** may travel to the gate stack **21** when a user does not desire the floating gate **22** to store charge. Similarly, a charge stored on the floating gate **22** may travel to the conventional contact **52**. Thus, a charge intentionally stored on the floating gate **22** may bleed away. Consequently, the cell **20** is subject to unanticipated charge gain and charge loss. As a result, the cell **20** may not function as desired.

Accordingly, what is needed is a system and method for providing contacts in a semiconductor device which has reduced charge gain and charge loss. The present invention addresses such a need.

SUMMARY OF THE INVENTION

The present invention provides a method and system for providing a contact in a semiconductor device including a plurality of gates. The method and system comprise providing an insulating layer substantially surrounding at least a portion of the plurality of gates and providing at least one contact in the insulating layer. The at least one contact has a side defining a sloped profile. The sloped profile includes an angle between the side of the contact and a surface of the substrate that is less than approximately eighty-eight degrees.

According to the system and method disclosed herein, the present invention provides a greater spacing between the contact and the closest gate stack without increasing the spacing between gate stacks or between the center of the contact and the gate stack. Consequently, a higher density of devices can be achieved while reducing the charge gain and charge loss through the contact.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram of a conventional semiconductor device

FIG. **2** is a diagram of a one embodiment of a semiconductor device including a contact in accordance with the present invention.

FIG. **3A** is a flow chart depicting one embodiment of a method for providing a contact for a semiconductor device in accordance with the present invention.

FIG. **3B** is a flow chart depicting one embodiment of a method for providing the contact in accordance with the present invention.

FIG. **3C** is a flow chart depicting one embodiment of a method for providing the contact hole in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to an improvement in semiconductor processing. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is

not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features described herein.

A conventional semiconductor device, such as a flash memory, includes a large number of cells, which are typically floating gate devices such as floating gate transistors. The cells also include sources and drains. Typically, each cell also includes spacers. In order to make electrical contact to the source or drain of one or more of the cells, a conventional contact hole is filled with a conductive material to provide a conventional contact. The conventional contact hole is provided in a conventional insulating layer that may otherwise cover and insulate the cells.

Although the conventional semiconductor device functions, one of ordinary skill in the art will readily realize that the conventional semiconductor device is subject to unanticipated charge gain and charge loss because of the spacing of the contact and a nearest cell. The cells and contacts of a conventional semiconductor device are relatively close. In particular, the distance between the base of the conventional contact and the edge of nearest gates of a gate stack is very small. The small spacing between the conventional contact and the gate stack causes undesirable charge gain and charge loss from the cell. Because the conventional contact is typically separated from the edge of the nearest gate stack by such a small distance, the portion of the insulating layer and any spacer between the conventional contact may allow charge stored on the cell to travel to the contact, thereby bleeding away. For similar reasons, a charge on the contact may travel to the nearest cell. Consequently, the cell is subject to unanticipated charge gain and charge loss. As a result, the semiconductor device may malfunction, which is undesirable.

The present invention provides a method and system for providing a contact in a semiconductor device including a plurality of gates. The method and system comprise providing an insulating layer substantially surrounding at least a portion of the plurality of gates and providing at least one contact within the insulating layer. The at least one contact has a side defining a sloped profile. The sloped profile includes an angle between the side of the contact and a surface of the substrate that is less than approximately eighty-eight degrees.

The present invention will be described in terms of a particular device having certain components and particular techniques, such as a plasma etch, for performing certain steps. However, one of ordinary skill in the art will readily recognize that this method and system will operate effectively for other devices having other components and other techniques. Furthermore, the present invention will be described in terms of a particular semiconductor memory device. However, nothing prevents the method and system from being utilized with another semiconductor device.

To more particularly illustrate the method and system in accordance with the present invention, refer now to FIG. **2**, depicting one embodiment of a semiconductor device **100**, such as a memory, for providing a semiconductor device including a contact in accordance with the present invention. The semiconductor device **100** includes a number of cells **120**, **130** and **140**, which are typically floating gate devices such as floating gate transistors. Each cell **120**, **130** and **140** includes a gate stack **121**, **131** and **141**. Each gate stack **121**, **131** and **141** includes a floating gate **122**, **132** and **142**, respectively, and a control gate **124**, **134** and **144**, respectively. The cells **120**, **130** and **140** also include drains **129** and **139** and sources **119** and **149**. The cells **120** and **140** are depicted as sharing a common drain **129**, while the cells **120** and **130** are depicted as sharing a common source **119**. Typically, each cell **120**, **130** and **140** also includes spacers **126** and **128**, **136** and **138**, and **146** and **148**, respectively. Preferably, the spacers **126**, **128**, **136**, **138**, **146** and **148** are approximately one thousand to two thousand Angstroms thick.

In order to make electrical contact to one or more of the cells **120**, **130** and **140**, an electrical contact **152** in accordance with the present invention is used. The electrical contact **152** is provided within a contact hole **150** in accordance with the present invention. The contact hole **150** is provided in an insulating layer **154** which otherwise covers the cells **120**, **130** and **140**. The insulating layer **154** insulates the cells **120**, **130** and **140**. The contact hole **150** is filled with a conductive material to form the contact **152**.

The contact hole **150** and, therefore, the contact **152** have sides having a sloped profile. Thus, the base of the contact hole **150** and the contact **152** is smaller than the top of the contact hole **150** and the contact **152**, respectively. Thus, the contact **152** is a tapered contact. In a preferred embodiment, the angle, θ, between the surface of the substrate **110** underlying the contact **152** and the sides of the contact hole **150** and contact **152** is between eighty-two and eighty eight degrees. Thus, the distance between the base of the contact hole and the nearest gate stack, such as the gate stack **121** is increased. However, the top of the contact hole **150** and, therefore, the top of the contact **152** may still be approximately 0.2–0.4 μm wide. As a result, a conventional photoresist structure (not shown) may be used to provide the contact hole **150**. However, the bottom of the contact hole **150** and the bottom of the contact **150** are smaller than 0.2–0.4 μm wide. Thus, the top edge of the contact hole **150** may be a smaller horizontal distance from the closest edge of the nearest gate stack **121** than the bottom edge of the contact hole **150**. Similarly, the top edge of the contact **152** may be a smaller horizontal distance from the closest edge of the nearest gate stack **121** than the base of the contact **152**. In a preferred embodiment, the top side of the contact hole **150** or contact **152** is approximately the same distance from the closest edge of the gate stack **121**, measured horizontally, as the conventional contact hole **50** or contact **52** depicted in FIG. **1**. Referring back to FIG. **2**, as discussed above, even if the top of the contact hole **150** or contact **152** is no farther from the gate stack **121**, the bottom of the contact hole **150** or contact **152** is farther from the gate stack **121**. Note, however, that nothing prevents the top edge of the contact hole **150** or contact **152** from being another distance from the closest edge of the gate stack **121**.

Because the profile of the sides of the contact **152** are sloped, the edge of the contact **152** is separated from the edge of the nearest gate stack **121** by a greater distance. Because the edge of the contact **150** is a greater distance from the edge of the gate stack **121**, there is more of the insulating layer **154** between the contact **152** and the edge of the gate stack **121**. As a result, the insulating layer **154** is better able to electrically insulate the contact **152** from the edge of the gate stack **121**. In a preferred embodiment, there is sufficient insulation to electrically insulate the contact **152** from the gate stack **121**. Consequently, charge intentionally stored by the memory cell **120**, for example on the floating gate **122**, is much less likely to travel through the insulating layer **154** to the contact **152**. Similarly, charge on the contact **152** is much less likely to travel through the insulating layer to the gate stack **121**. As a result, unwanted charge gain and charge loss may be reduced or eliminated in a semiconductor device which has components relatively densely packed.

FIG. 3A depicts one embodiment of a method **200** for providing a semiconductor device in accordance with the present invention. The memory cells **120**, **130** and **140** are provided, via step **202**. In a preferred embodiment, step **202** includes at least providing the gate stacks **121**, **131**, and **141**. Step **202** may also include providing the spacers **126**, **128**, **136**, **138**, **146**, and **148**. The insulating layer **154** is then provided on the gate stacks, via step **204**. The contact **152** having a sloped profile is then provided, via step **206**. The sloped profile has an angle with the underlying substrate of less than eighty-eight degrees.

FIG. 3B depicts a flow chart of one embodiment of a method **210** in accordance with the present invention for performing step **206**, providing the contact **152**. One or more contact holes, such as the contact hole **150**, are provided, via step **212**. Thus, step **206** includes providing contact holes **150** which have a sloped profile. The contact **152** is provided by filling the contact hole **150** with a conductive material, via step **214**. Thus, the contact **152** having a sloped profile is formed.

FIG. 3C depicts one embodiment of a method **220** for performing the step **212** of providing the contact hole(s). A resist structure having apertures above the desired positions of the contact holes is provided, via step **222**. In a preferred embodiment, the apertures in the resist structure are approximately the same size as the desired size of the top of the contact hole **150**. The processing conditions are then adjusted to ensure that the contact hole **150** has a sloped profile, via step **224**. In a preferred embodiment, step **224** is performed by ensuring that the etch of the insulating layer has a more polymerizing chemistry. Preferably, step **224** includes increasing the ratios of CH_3F gas to CF_4 gas or CHF_3 gas to CF_4 gas. The etch for the contact hole **150** is then performed, via step **226**. The etch performed in step **226** is preferably a plasma etch.

In the method **220**, the etch itself insures that the contact **152** will be tapered, having a sloped profile. As a result, a conventional resist structure may be provided in step **222**. The photolithography used in step **222** to form the resist structure may thus be relatively simple to carry out. Furthermore, the etch conditions may be relatively easily controlled once the appropriate ratios of CH_3F gas to CF_4 gas or CHF_3 gas to CF_4 gas are determined. Consequently, the contact **152**, and contact hole **150**, may be relatively easy to provide. At the same time, a greater distance separates the contact **150** from a nearest gate stack **121**. Thus, the charge gain and charge loss issues of the conventional semiconductor device of FIG. **1** may be reduced or eliminated without significantly complicating processing of the semiconductor device **100**, depicted in FIG. **2**.

A method and system has been disclosed for providing a contact having a sloped profile. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a plurality of gate stacks;

an insulating layer substantially surrounding at least a portion of the plurality of gates; and

at least one contact disposed within the insulating layer, the at least one contact having a side defining a sloped profile including an angle between the side of the at least on contact and a surface of a substrate, the angle being less than approximately eighty-eight degrees.

2. The semiconductor device of claim **1** further comprising:

at least one contact hole within the insulating layer, the at least one contact hole having a second side defining a sloped profile including a second angle between the second side of the contact and the surface of a substrate, the second angle being substantially the same as the first angle; and

wherein the at least one contact further includes a conductive material filling the at least one contact hole to form at least one contact.

3. The semiconductor device of claim **2** wherein the angle is between eighty-two and eighty eight-degrees.

4. The semiconductor device of claim **2** wherein the at least one contact includes a bottom edge and a top edge and wherein a first distance between the bottom of the at least one contact and a nearest gate of the plurality of gates is greater than a second distance between the top edge of the at least one contact and the at least one contact.

* * * * *

US006459625B1

(12) **United States Patent**
Bill et al.

(10) **Patent No.: US 6,459,625 B1**
(45) **Date of Patent: Oct. 1, 2002**

(54) **THREE METAL PROCESS FOR OPTIMIZING LAYOUT DENSITY**

(75) Inventors: **Colin S. Bill**, Cupertino; **Jonathan S. Su**, Gabriel; **Ravi P. Gutala**, San Jose, all of CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/767,341**

(22) Filed: **Jan. 23, 2001**

Related U.S. Application Data

(60) Provisional application No. 60/185,149, filed on Feb. 25, 2000.

(51) **Int. Cl.**[7] **G11C 16/04**; G11C 5/02

(52) **U.S. Cl.** **365/185.33**; 365/63; 365/52

(58) **Field of Search** 365/185.05, 161, 365/164, 185.01, 185.33, 63, 52

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6,034,882 A * 3/2000 Johnson et al. 365/103

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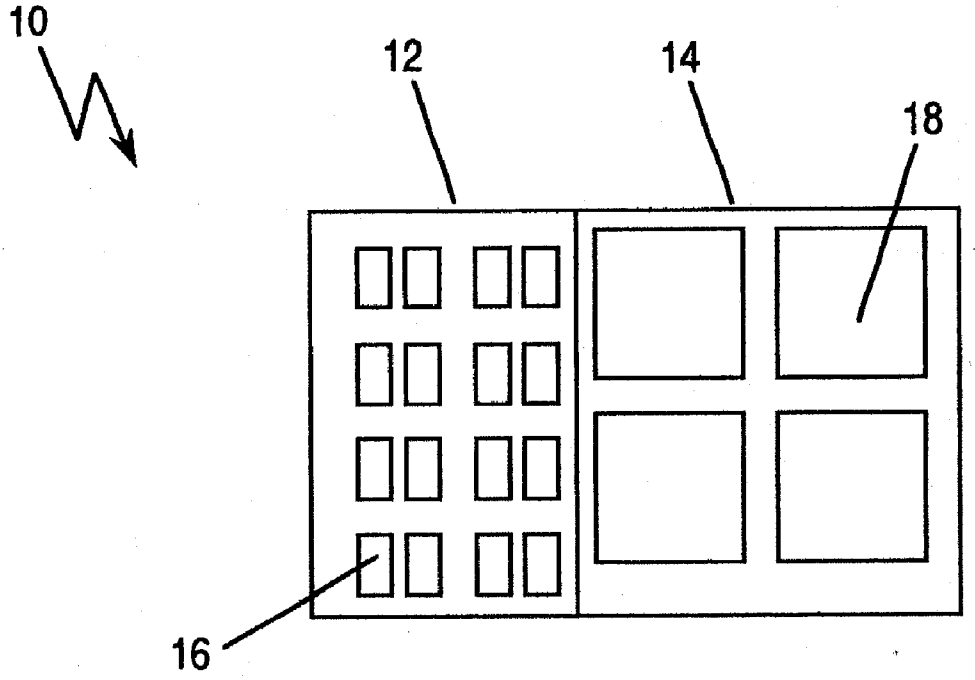
Primary Examiner—David Nelms
Assistant Examiner—Thong Le

(57) **ABSTRACT**

The present invention discloses a method and system to optimize electrical interconnection of electrical components in a periphery area of a memory device thereby minimizing the periphery area. The periphery area is divided into a plurality of sub-circuits formed by selectively electrically connecting the electrical components. Electrical interconnection of the electrical components to form the sub-circuits is accomplished using a first metal layer and a second metal layer. The first metal layer is formed to create a plurality of first metal layer lines that are oriented to extend in substantially one direction on the memory device. The second metal layer is formed to create a plurality of second metal layer lines that are oriented to extend substantially perpendicular to the first metal layer lines. The plurality of sub-circuits are electrically interconnected using a third metal layer that is formed to create a plurality of third metal layer lines that are oriented to extend substantially parallel to the first metal layer lines.

14 Claims, 4 Drawing Sheets



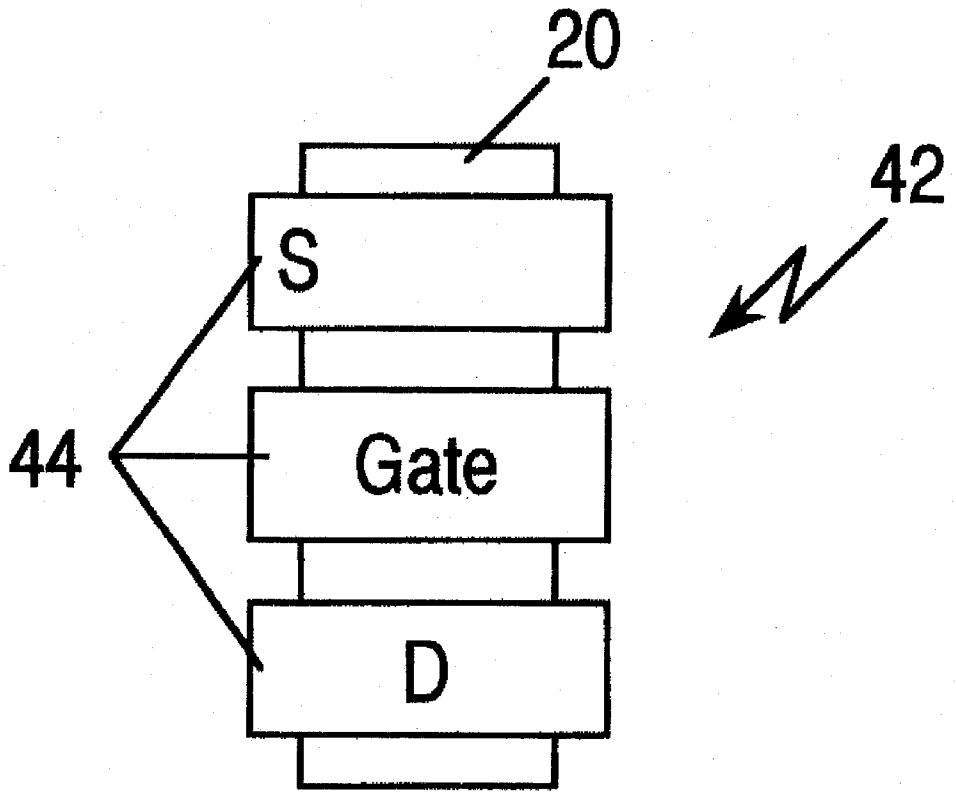


Fig. 4

US006459625B1

(12) **United States Patent**
Bill et al.

(10) **Patent No.: US 6,459,625 B1**
(45) **Date of Patent: Oct. 1, 2002**

(54) **THREE METAL PROCESS FOR OPTIMIZING LAYOUT DENSITY**

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(52) **U.S. Cl.** **365/185.33**; 365/63; 365/52

(58) **Field of Search** 365/185.05, 161, 365/164, 185.01, 185.33, 63, 52

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* cited by examiner

Primary Examiner—David Nelms
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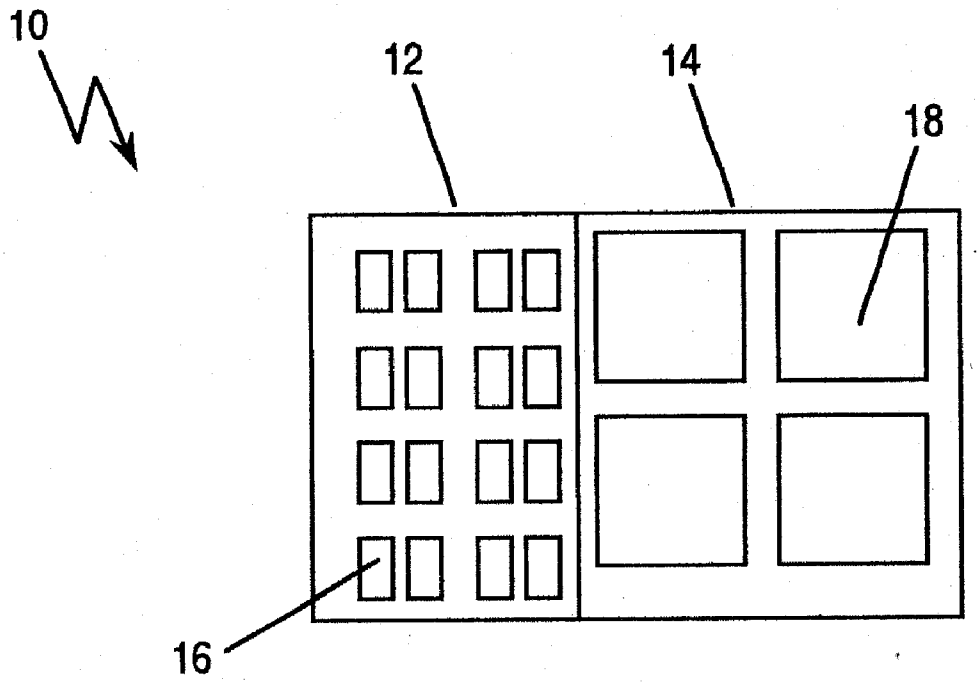
(57) **ABSTRACT**

The present invention discloses a method and system to optimize electrical interconnection of electrical components in a periphery area of a memory device thereby minimizing the periphery area. The periphery area is divided into a plurality of sub-circuits formed by selectively electrically connecting the electrical components. Electrical interconnection of the electrical components to form the sub-circuits is accomplished using a first metal layer and a second metal layer. The first metal layer is formed to create a plurality of first metal layer lines that are oriented to extend in substantially one direction on the memory device. The second metal layer is formed to create a plurality of second metal layer lines that are oriented to extend substantially perpendicular to the first metal layer lines. The plurality of sub-circuits are electrically interconnected using a third metal layer that is formed to create a plurality of third metal layer lines that are oriented to extend substantially parallel to the first metal layer lines.

14 Claims, 4 Drawing Sheets



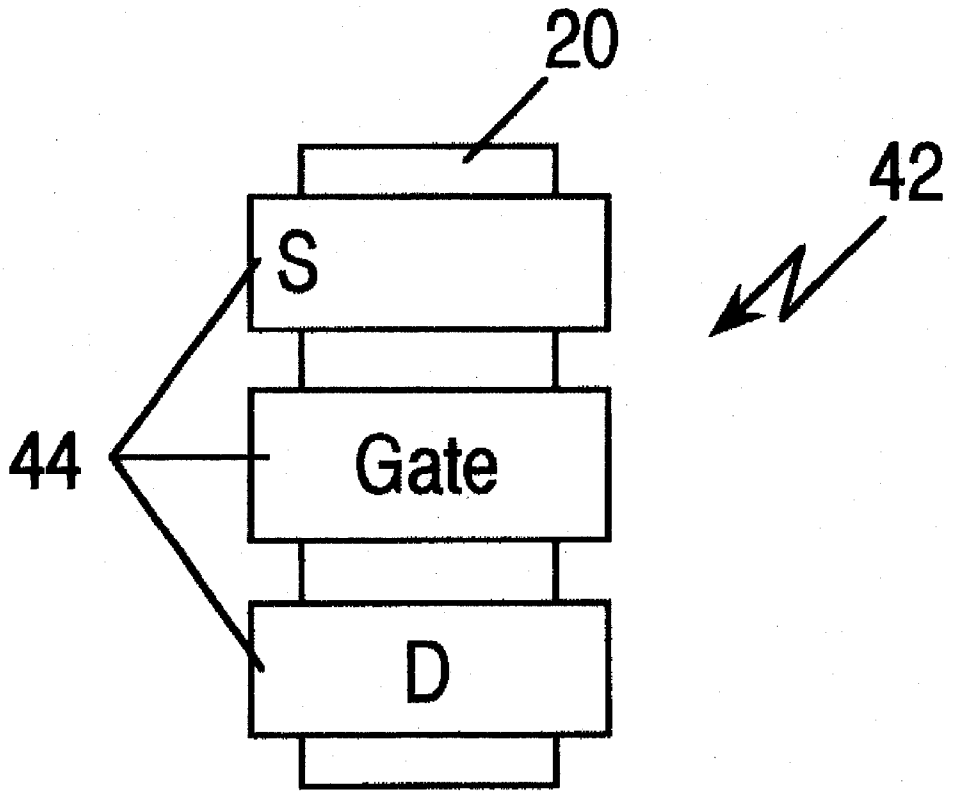


Fig. 4

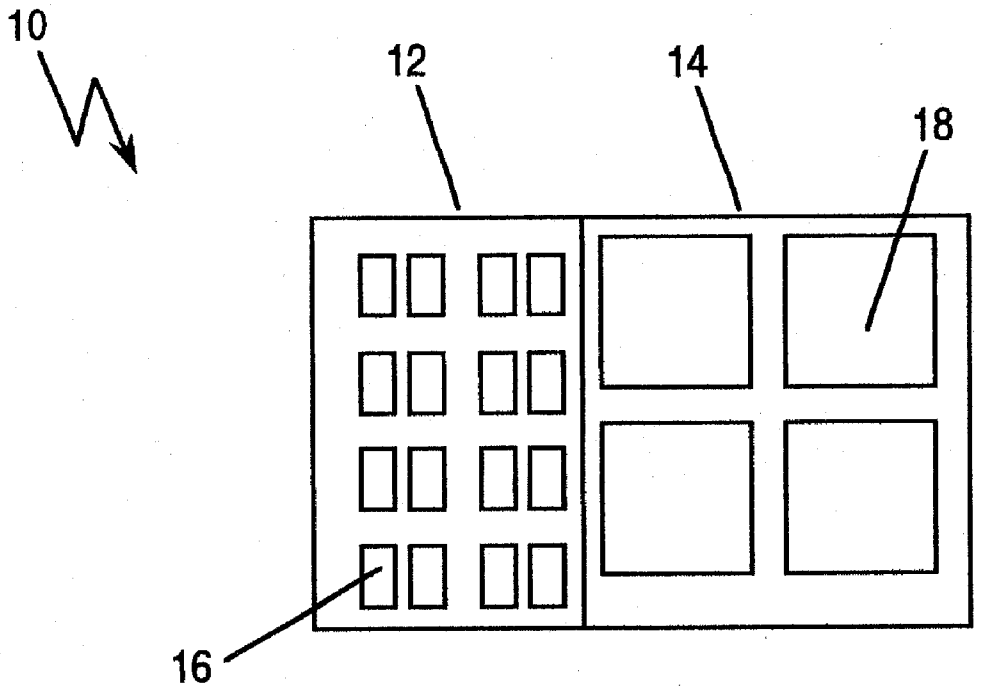


Fig. 1

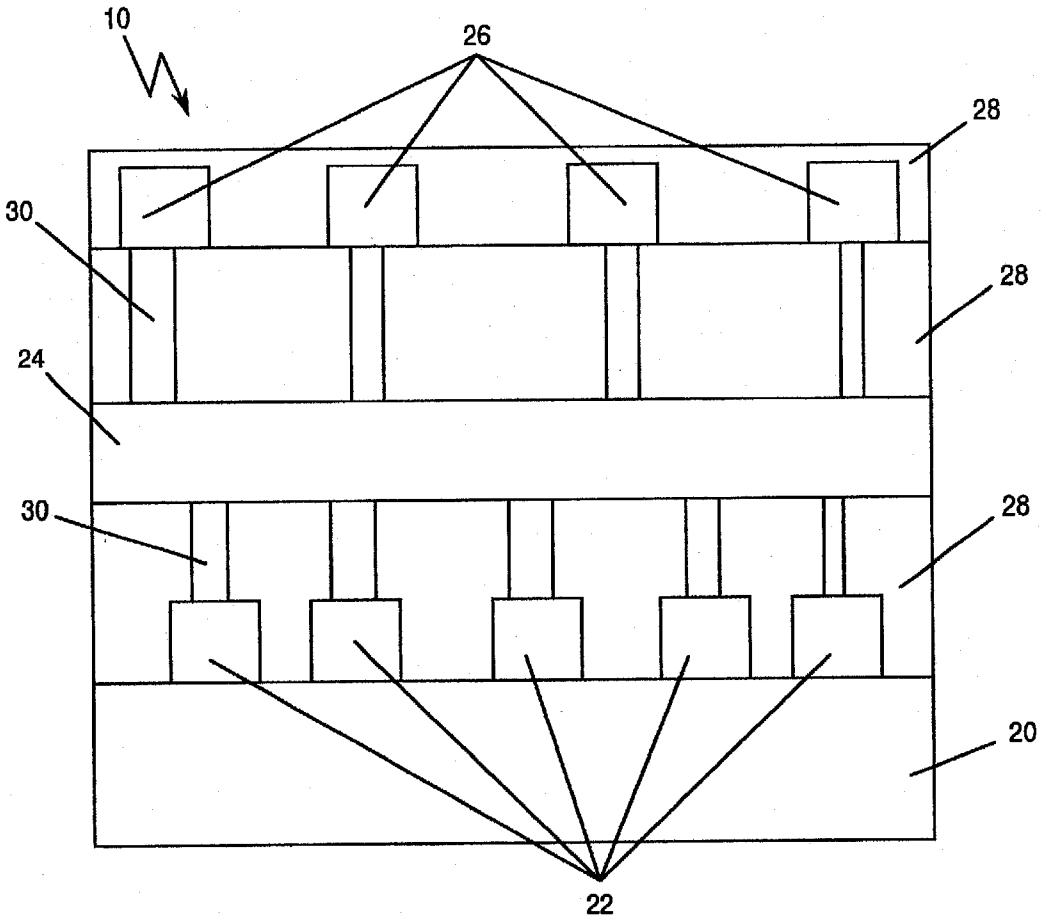


Fig. 2

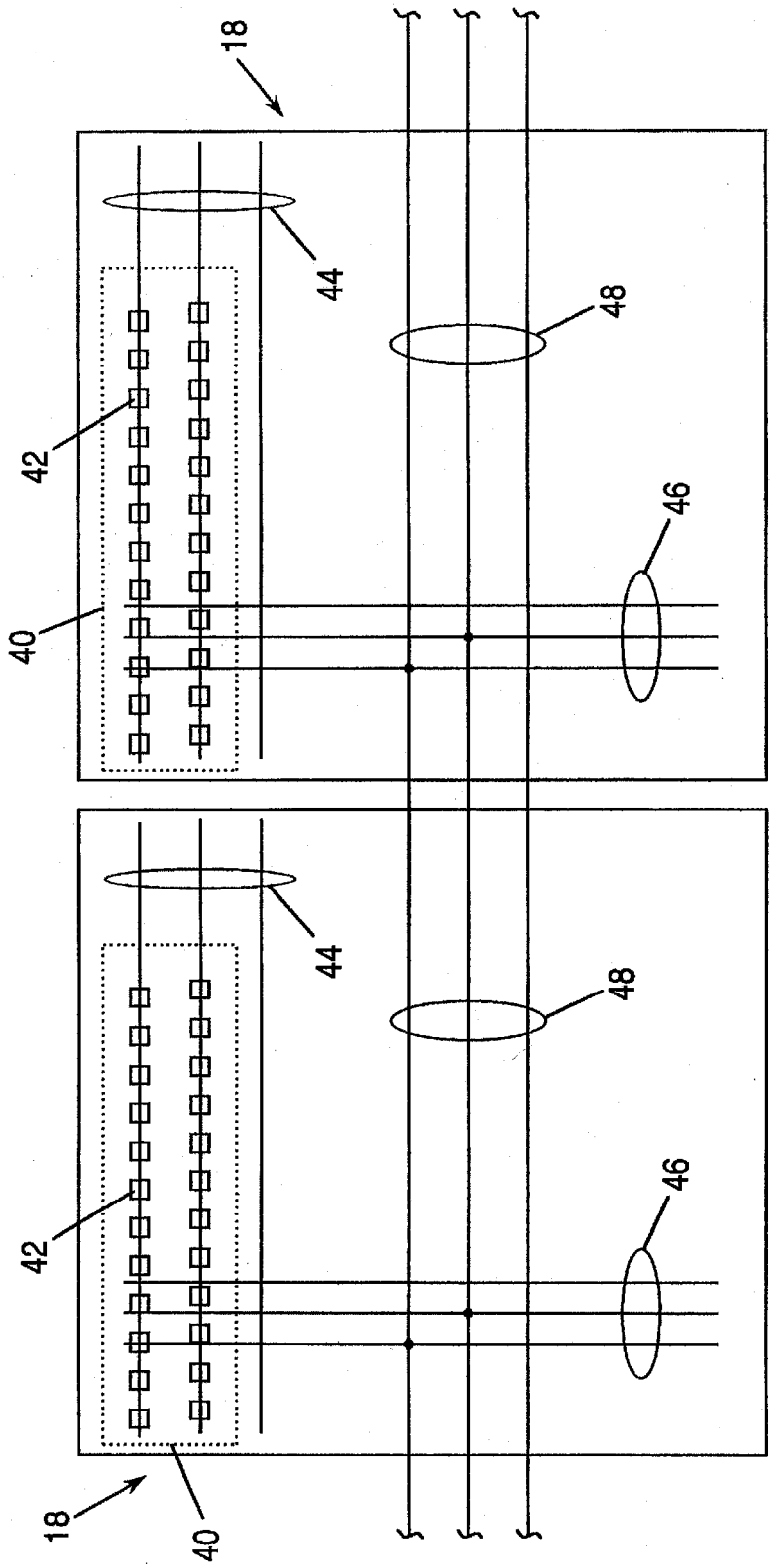


Fig. 3

THREE METAL PROCESS FOR OPTIMIZING LAYOUT DENSITY

This application claims the benefit under 35 U.S.C. §119(e) of Provisional U.S. patent application Ser. No. 60/185,149, filed Feb. 25, 2000.

FIELD OF INVENTION

The present invention relates generally to non-volatile memory devices and, more particularly, to methods and systems for optimization of layout density in a periphery area using a three-metal interconnection process in flash electrically erasable programmable read-only memory (EEPROM) devices.

BACKGROUND OF THE INVENTION

Flash memories are popular memory storage devices because they store information in the absence of continuous power and are capable of being constructed in a very compact form. Flash memory is typically constructed by fabricating a plurality of electrical components in a silicon substrate. It is desirable to place as many of the electrical components as possible in the available area on the silicon substrate to optimize functionality and economical manufacture. The density or layout area of the electrical components depends on the physical size of the electrical components and the electrical connections between components. As the size of the electrical components decreases due to technological advances, more components can be placed in the available area on the flash memory. However, more electrical components require more electrical connections that can offset the layout area gained by the smaller component size.

Flash memory devices include two functional areas, a core cell area to perform memory functions and a periphery area to perform logic functions. As known in the art, the core cell area includes rows and columns of electrical components that are floating-gate transistors formed in the silicon substrate during fabrication. The floating-gate transistors located in the core cell area of the flash memory are typically referred to as core memory cells. The rows of core memory cells within the core cell area are typically electrically connected to form wordlines and the columns of core memory cells within the core cell area are typically electrically connected to form bitlines. As known in the art, the wordlines and bitlines are used to provide predetermined operational voltages to erase, read and write the core memory cells within the core cell area.

In addition to the core cell area, the flash memory also has a periphery area that includes a plurality of electrical components such as transistors, resistors, capacitors and diodes formed in the silicon substrate during fabrication. As known in the art, the resistors, capacitors and diodes may be formed during fabrication to create electrical components such as bipolar and field-effect transistors. The electrical components are electrically connected to form integrated circuits that perform logic functions within the flash memory to support operations such as the read, write and erase of the core memory cells. Part of the formation of the electrical connections of the electrical components occurs during a fabrication process known in the art as metallization.

Generally, metallization involves depositing a thin film of conductive metal on the flash memory such that the electrical components are formed and electrically connected with the conductive metal. In addition to forming portions of the electrical components, the conductive metal electrically connects the electrical components in a predetermined configuration, thereby "wiring" the electrical components to create the integrated circuits. The conductive metal that electrically connects the electrical components is routed on the flash memory and contributes to the layout area consumed.

Known prior art flash memory uses a two-metal layer metallization process to electrically connect the electrical components in the periphery area of the flash memory. A first layer of metal is typically used to form portions of the electrical components and to electrically connect the electrical components to form a plurality of sub-circuits that perform predetermined logic functions during operation. A second layer of metal is typically used to electrically connect one sub-circuit with another and to electrically connect the sub-circuits with the core memory cells in the core area such that operations can be performed within the flash memory.

A known problem with this method and system of electrical connection is layout area consumed by routing channels of the first and second layer of metal between the sub-circuits in the periphery area. In addition, layout area is consumed for routing channels that are used to route the first and second metal layers between the electrical components that form the sub-circuits. The layout area for the routing channels required by existing electrical connection systems and methods increases the size of the periphery area on the flash memory. The area on the flash memory that is not consumed by the periphery area can be reserved for the core cell area, allowing more core memory cells to be fabricated on the flash memory. It is therefore desirable to minimize the amount of periphery area consumed, thereby increasing the amount of information stored in the flash memory. That is, the ratio of the core area to the periphery area can be maximized.

To that end, a need exists for flash memory with an improved method and system of interconnection of electrical components to minimize the area consumed in the periphery area of the flash memory.

SUMMARY OF THE INVENTION

The present invention discloses a method and system of optimizing layout area consumed in a periphery area of a flash memory. The flash memory includes a core cell area and the periphery area. Within the core cell area, the flash memory includes a plurality of core memory cells; and, within the periphery area, the flash memory includes a plurality of sub-circuits. Generally, the core cell area provides memory-related functions in the flash memory and the periphery area supports the memory-related functions by providing logic-related functions in the flash memory.

The core cell area and the periphery area share the available area on the flash memory. As such, a smaller periphery area is desirable, thereby increasing the area available for the core cell area. In the preferred embodiment, selectively placing and electrically connecting a plurality of electrical components to form the sub-circuits and selectively electrically connecting the sub-circuits with the core memory cells mininimizes the layout area of the sub-circuits in the periphery area.

The preferred sub-circuits include the electrical components such as transistors, resistors, capacitors and diodes that are electrically connected with a first metal layer, a second metal layer and a third metal layer. The electrical components are electrically connected to form the sub-circuits by the first metal layer and the second metal layer. The sub-circuits are electrically interconnected with each other and

with the core memory cells in the core cell area by the third metal layer. Those skilled in the art would understand that, typically, the majority of electrical components in the periphery area used to create the integrated circuits are transistors; however, other electrical components such as diodes and resistors could also be utilized.

The circuit layout of the sub-circuits is such that the transistors are oriented to form a plurality of rows of transistors wherein each transistor has a drain and a source oriented along an axis parallel with the rows of transistors. In another preferred embodiment of the present invention, the drain and the source of the transistors are not oriented along an axis parallel with the rows of transistors.

The first metal layer is applied to the periphery area of the flash memory during fabrication to form and partially interconnect the electrical components in a predetermined circuit configuration. The first metal layer comprises a plurality of first metal lines that provide interconnecting surface "wiring" for the predetermined circuit configuration. The layout in the periphery area of the first metal lines is oriented to extend along an axis substantially parallel to the rows of transistors. The second metal layer also provides surface "wiring" of the electrical components to complete the predetermined circuit configuration and form the sub-circuits. The second metal layer is also applied to the periphery area of the flash memory during fabrication. The layout of the second metal layer on the flash memory is deposited to form a plurality of second metal lines that are oriented to extend along an axis substantially perpendicular to the first metal lines.

The sub-circuits are selectively electrically interconnected and electrically connected with the core memory cells in the core cell area by the third metal layer. The third metal layer is also applied to the periphery area of the flash memory during the fabrication process and is adapted to form a plurality of third metal lines. The third metal lines provide surface "wiring" to electrically connect the sub-circuits with the core memory cells and are oriented to extend along an axis substantially parallel to the first metal lines.

During the fabrication process, the periphery area consumed by the transistors, the first metal layer, the second metal layer and the third metal layer is optimized in the preferred embodiment. The orientation of the transistors uniformly in rows allows the spacing between the transistors in the rows to be minimized without causing short circuits or undesirable leakage currents while still allowing electrical connection of the transistors. In addition, the combination of the first metal layer and the second metal layer to form and electrically connect the electrical components to create the sub-circuits also minimizes the periphery area consumed.

The electrical connections with the transistors are typically located directly below the first metal lines of the first metal layer. Since the first metal lines are substantially straight, additional spacing between the rows of transistors to allow for electrical connection of the transistors to the first metal layer is minimized. The second metal lines of the second metal layer provide additional electrical connections to complete the sub-circuits, thereby minimizing bends in the first metal lines and repositioning of the electrical components under the first metal lines. The second metal lines are also substantially straight and orthogonally pass over the first metal lines, thereby minimizing noise and allowing efficient electrical connections that further minimize consumption of the periphery area. The third metal layer provides electrical connection of the first metal layer and the second metal layer with the core memory cells. As such, the third metal lines can be substantially straight and be routed on top of the sub-circuits such that consumption of the periphery area is minimized.

These and other features and advantages of the invention will become apparent upon consideration of the following detailed description of the presently preferred embodiments of the invention, viewed in conjunction with the appended drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** represents a block diagram of a portion of a preferred flash memory incorporating an embodiment of the present invention.

FIG. **2** generally illustrates a cross-sectional view of a portion of the preferred flash memory.

FIG. **3** illustrates a top view of two sub-circuits of the preferred flash memory.

FIG. **4** illustrates the preferred source/drain orientation in relation to the first metal layer lines.

DETAILED DESCRIPTION OF THE INVENTION

The exemplary embodiments of the invention are set forth below with reference to specific configurations, and those skilled in the art would recognize that various changes and modifications can be made on the specific configurations while remaining within the scope of the claims. The invention may be used with any type of memory device; however, the preferred embodiment of the invention is designed for a flash memory.

FIG. **1** illustrates a general block diagram of a preferred flash memory **10** incorporating an embodiment of the present invention. The flash memory **10** includes a core cell area **12** and a periphery area **14**. As known in the art, within the core cell area **12**, the flash memory **10** includes a plurality of core memory cells **16**. Within the periphery area **14**, the flash memory **10** includes a plurality of sub-circuits **18** that are made up of various types of circuit components such as transistors, capacitors and resistors. Generally, the core cell area **12** performs memory-related functions in the flash memory **10**, and the periphery area **14** supports the memory-related functions by performing logic-related functions in the flash memory **10**. Although not illustrated in FIG. **1**, the periphery area **14** typically includes electronic circuits such as decoder circuits, state machine circuitry, voltage regulator circuits and addressing circuits as known in the art.

In order to understand the method and system of optimizing the layout in the periphery area **14**, an understanding of the operation and configuration of the periphery area **14** is helpful. Generally, during operation of the preferred flash memory **10**, the sub-circuits **18** within the periphery area **14** execute a plurality of functions to assist in performing memory operations such as read, write and erase. The sub-circuits **18** are integrated electric circuits that occupy different physical areas in the periphery area **14** of the flash memory **10**, and are identified based on the function the particular sub-circuit **18** performs. Those skilled in the art would recognize that the sub-circuits **18** in the periphery area **14** of the flash memory **10**, as briefly set forth above, can contain many types of logic circuits and control circuits that perform a variety of functions in the flash memory **10**. The present invention relates to methods of optimally placing and electrically interconnecting transistors that are used

in the sub-circuits **18** to the other respective sub-circuits **18**, as well as interconnecting the various electrical components used in a particular sub-circuit **18** with one another.

The physical size of the periphery area **14** occupied by the sub-circuits **18** is a predetermined area based on the physical size of the particular sub-circuits **18**, which is determined on a circuit-by-circuit basis during the design phase of the flash memory **10**. The design phase occurs prior to fabrication of the flash memory **10** and involves circuit design, dimensioning and circuit layout of the sub-circuits **18** on the surface of the flash memory **10**. The circuit layout area of a particular sub-circuit **18** is preferentially designed using just enough area for the physical dimensions of the electrical components and interconnections as well as providing enough spacing between components and the interconnections to avoid electrical short circuits and problems with leakage current. For the best layout efficiency of the layout of transistors used in the sub-circuits **18**, the transistors should have their source/drain geometries spaced apart by their minimum source/drain spacing rule. In addition, in the preferred embodiment, all of the transistors in the sub-circuits **18** are placed in rows while obeying the minimum source/drain spacing rules of the particular transistors.

FIG. **2** generally illustrates a cross-sectional view of a portion of a preferred flash memory **10**. As known in the art, the preferred flash memory **10** includes a substrate **20** where the electrical components of the flash memory **10** are formed during fabrication. In addition, the preferred flash memory **10** includes a first metal interconnect layer (M1) **22**, a second metal interconnect layer (M2) **24** and a third metal interconnect layer (M3) **26**, which are separated and encapsulated by a plurality of dielectric layers **28**. The dielectric layers **28**, which can be made using any dielectric material commonly used in the art such as oxide, silicon nitride or a polyamide film, provides an insulating layer between the first metal interconnect layer (M1) **22** and the second metal interconnect layer (M2) **24** in the preferred embodiment. In addition, the dielectric layer **28** is also used to provide an insulating layer between wiring lines formed in the respective first (M1), second (M2) and third (M3) metal interconnect layers **22**, **24**, **26** as set forth in detail below. One dielectric layer **28** is also deposited over the third metal interconnect layer (M3) **26** to protect the third metal interconnect layer (M3) **26**.

A plurality of contact holes **30**, which are also referred to in the art as vias, are created during fabrication to penetrate the dielectric layers **28** in predetermined locations of the flash memory **10**. The contact holes **30** provide electrical interconnections between the first metal interconnect layer (M1) **22**, the second metal interconnect layer (M2) **24** and the third interconnect layer **26** at the predetermined locations of the flash memory **10**. As known in the art, once the contact holes **30** are formed, the contact holes **30** are filled with a conductive material such as copper, tungsten or any other suitable conductive material. To that end, a conductive path is created between the respective metal interconnect layers **22**, **24**, **26** with the contact holes **30** at predetermined locations in the preferred flash memory **10**.

FIG. **3** generally represents the top view of two sub-circuits **18** within the periphery area **14** of the flash memory **10**. As previously set forth, the sub-circuits **18** include a plurality of electrical circuits **40**, which generally include a plurality of transistors **42** and a plurality of other circuit components (not shown). Although not illustrated, those skilled in the art would recognize that other circuit components, such as resistors, capacitors and diodes may also be used in the electrical circuits **40**. However, since a majority of the circuit components used in the preferred flash memory **10** are transistors **42**, the present invention is directed to methods and systems that provide optimal transistor **42** layout and interconnection.

In the preferred embodiment, the individual components of the electrical circuits **40** in each sub-circuit **18** are electrically interconnected with one another in a predetermined manner to form the sub-circuits **18** by the first metal interconnect layer (M1) **22** and the second metal interconnect layer (M2) **24**. The circuit component layout of the sub-circuits **18** is preferentially designed such that the transistors **42** of the electrical circuits **40** are positioned to form rows of transistors **42**, wherein each transistor **42** is positioned such that its drain and source are oriented along a common horizontal axis with wiring lines formed by the first metal interconnect layer (M1) **22** as set forth in detail below.

The first metal interconnect layer (M1) **22** is deposited on the periphery area **14** of the flash memory **10** during fabrication to partially interconnect the individual circuit components of each respective electrical circuit **40** in predetermined circuit configurations. Referring to FIGS. **2** and **3**, the first metal interconnect layer (M1) **22** is fabricated to form a plurality of first metal layer lines **44** that provide interconnecting surface "wiring" of the components of the electrical circuits **40**. In the preferred embodiment, the first metal layer lines **44** are formed to extend along an axis substantially parallel to the rows of transistors **42** in the electrical circuits **40**. Those skilled in the art would recognize that occasional deviation from the axis parallel with the rows of transistors **42** will occur to perform necessary electrical connections but, preferentially, the first metal layer lines **44** are formed parallel with the rows of transistors **42**. The electrical circuits **40** are partially electrically interconnected once the first metal interconnect layer (M1) **22** is deposited during fabrication to form the first metal layer lines **44**. As set forth below, the remaining electrical interconnection of the electrical circuits **40** in the sub-circuits **18** is accomplished using the second metal interconnect layer (M2) **24**.

The second metal interconnect layer (M2) **24** also provides surface "wiring" of the electrical circuits **40** to complete the predetermined circuit configuration and formation of the sub-circuits **18**. The second metal interconnect layer (M2) **24** is fabricated on the periphery area **14** of the flash memory **10** during fabrication in a predetermined configuration. Referring to FIGS. **2** and **3**, the second metal interconnect layer (M2) **24** is fabricated to form a plurality of second metal layer lines **46** that are oriented substantially perpendicular to the first metal layer lines **44**. Those skilled in the art would again recognize that occasional deviation from the axis perpendicular with the first metal layer lines **44** will occur to facilitate efficient electrical connections but, preferentially, the second metal layer lines **46** are formed to run perpendicular to the orientation of the first metal layer lines **44**.

As set forth above, the electrical circuits **40** of the sub-circuits **18** are electrically interconnected with the first metal layer lines **44** and the second metal layer lines **46**. As such, each circuit component and transistor **42** in the electrical circuits **40** are interconnected in a predetermined configuration using the first metal layer lines **44** and the second metal layer lines **46**. The contact holes **30** are used to electrically connect the second metal layer lines **46** to respective first metal layer lines **44** and circuit components and transistors **42** on the substrate **20**. Utilizing both the first metal interconnect layer (M1) **22** and the second metal

interconnect layer (M2) **24** within the boundary of the sub-circuits **18** provides the greatest opportunity to place transistors **42** at their minimum spacing and yet have the metal interconnect consuming no extra area than that needed by the transistors **42**. As such, this layout scheme optimizes the area consumed by the transistors **42**.

The third metal interconnect layer (M3) **26** is used to electrically interconnect one respective sub-circuit **18** to another respective sub-circuit **18** in the preferred flash memory **10**. The third metal interconnect layer (M3) **26** is fabricated to form a plurality of third metal layer lines **48** that electrically interconnect the respective sub-circuit **18** to each other. The third layer metal lines **48** are formed perpendicular to the second metal layer lines **46** in the preferred flash memory **10**. Those skilled in the art would recognize that occasional deviation from the axis perpendicular to the second metal layer lines **46** will occur to facilitate electrical connection but, preferentially, the third metal layer lines **48** are formed perpendicular to the second metal layer lines **46**.

Although not illustrated, in the preferred embodiment, the sub-circuits **18** are also electrically interconnected with the core memory cells **16** in the core cell area **12** by the third metal layer lines **48**. The third metal layer lines **48** therefore provide the surface "wiring" that electrically connect the sub-circuits **18** with the core memory cells **16** and are generally oriented to extend along an axis parallel to the first metal layer lines **44**. As illustrated in FIG. **2**, the third metal layer lines **50** are connected with the first and second metal layer lines **44**, **46** using contact holes **30** to reach the other layers. Although not illustrated, in the preferred embodiment of the present invention, those skilled in the art should recognize that the contact holes **30** can travel through more than one metal interconnect layer.

During the fabrication process, the periphery area **14** consumed by the electrical circuits **40** is optimized by using the preferred embodiment of the present invention. As previously set forth, the electrical circuits **40** include uniformly oriented rows of transistors **42** and are oriented such that the drain of a respective transistor **42** is adjacent to the source of the next transistor **42** in the rows of transistors **42**. When the transistors **42** of the electrical circuits **40** are oriented in rows, the layout area between respective electrical circuits **40** is minimized without causing short circuits or undesirable leakage currents while still providing electrical interconnection of the electrical circuits **40**. Referring to FIG. **4**, which is an enlarged view of one of the transistors **42** illustrated in FIG. **3**, the source, gate and drain of the transistors **42** used in the electrical circuits **40** are oriented substantially parallel with the first metal layer lines **44**.

Using the first metal layer lines **44** that are formed by the first metal interconnect layer (M1) **22** and the second metal layer lines **46** that are formed by the second metal interconnect layer (M2) **24** to electrically interconnect the electrical circuits **40** to form the sub-circuits **18** minimizes the periphery area **14** consumed in the preferred flash memory **10**. As previously set forth, the first metal layer lines **44** are oriented to extend substantially parallel with the rows of transistors **42** in the periphery area **14**. In addition, the electrical connections with the drains, sources and control gates of the transistors **42** in the electrical circuits **40** are located directly below the first metal layer lines **44**. Since the first metal layer lines **44** are formed substantially parallel with the transistors **42**, additional layout area between the rows of transistors **42** is further minimized.

The second metal layer lines **46** formed by the second metal interconnect layer **34** provide additional electrical interconnections to complete the sub-circuits **18**, thereby minimizing bends required in the first metal layer lines **44** and repositioning of the electrical components under the first metal layer lines **44**. Prior art electrical interconnection connection of the sub-circuits was completed using the first metal interconnect layer, thereby requiring several bends in the first metal layer lines formed by the first metal interconnect layer or increasing the spacing between the electrical components used in the periphery area. The second metal layer lines **46** formed by the second metal interconnect layer (M2) **24** are also substantially straight and oriented substantially perpendicular to the first metal layer lines **44** in the preferred embodiment. As such, the second metal layer lines **46** uniformly pass over the first metal layer lines **44**, thereby minimizing noise created by parasitic capacitance and allowing efficient electrical connections that further minimize consumption of the space available in the periphery area **14**.

The electrical interconnection of the sub-circuits **18** and the core memory cells **16** by the third metal interconnect layer (M3) **26** is also optimized in the preferred embodiment. The third metal interconnect layer (M3) **26** provides electrical interconnection of the first metal interconnect layer **22**, the second metal interconnection layer **24** and therefore connecting the sub-circuits **18** with the core memory cells **16**. As such, the third metal layer lines **48** that are formed by the third metal interconnect layer (M3) **26** are substantially straight and routed on top of the sub-circuits **18** such that consumption of the periphery area **14** is minimized. In addition, the third metal layer lines **48** are sufficiently separated from the first metal layer lines **44** and perpendicularly pass over the second metal layer lines **46** such that noise created by parasitic capacitance is minimized.

In the prior art, the second metal interconnect layer is used to electrically connect the first metal interconnect layer with the core memory cells by routing the second metal lines of the second metal interconnect layer in routing channels between the sub-circuits. The routing of the second metal lines of the second metal interconnect layer between the sub-circuits consumes layout area between the sub-circuits, thereby enlarging the periphery area. In the present invention, no additional layout area is required between the sub-circuits **18** for the third metal interconnect layer (M3) **26** and consumption of the periphery area **14** is further minimized.

While the invention has been described in its currently best known modes of operation and embodiments, other modes and embodiments of the invention will be apparent to those skilled in the art and it is the following claims, including all equivalents, that are intended to define the spirit and scope of the invention.

What is claimed is:

1. A method of electrically interconnecting a periphery area in a flash memory, comprising:

providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein each sub-circuit includes at least one electrical circuit having a plurality of circuit components;

partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction;

completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of

second metal layer lines that are oriented substantially perpendicular to said first metal layer lines; and

electrically interconnecting each respective sub-circuit with a predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines.

2. The method of claim **1**, further comprising the step of depositing a dielectric layer between said first, second and third metal interconnect layers.

3. The method of claim **1**, wherein a plurality of contact holes are used to electrically interconnect said first metal interconnect layer, said second metal interconnect layer and said third metal interconnect layer at predetermined locations.

4. The method of claim **1**, wherein said circuit components include a plurality of transistors that are arranged in rows substantially parallel with said first metal layer lines.

5. The method of claim **4**, wherein said transistors are at least spaced apart from each other by at least the minimum source/drain spacing rule of said transistors.

6. A method of optimizing circuit layout in a flash memory, comprising:

forming a plurality of sub-circuits in a periphery area of a silicon substrate, wherein each sub-circuit includes at least one electric circuit having a row of transistors;

depositing a first metal interconnect layer on said substrate to partially electrically interconnect the transistors of the sub-circuits, wherein said first metal interconnect layer forms a plurality of first metal layer lines that are oriented to extend substantially in the same direction as said row of transistors;

depositing a second metal interconnect layer above said first metal interconnect layer to complete the electrical interconnection of said respective transistors within said sub-circuits, wherein said second metal interconnect layer forms a plurality of second metal lines oriented to extend substantially perpendicular to said first metal layer lines; and

depositing a third metal interconnect layer above said second metal interconnect layer to electrically interconnect the respective sub-circuits, wherein said third metal layer forms a plurality of metal layer lines oriented to extend substantially parallel to said first metal layer lines.

7. The method of claim **6**, further comprising the step of depositing a dielectric layer between said first, second and third metal interconnect layers.

8. The method of claim **6**, wherein a plurality of contact holes are used to electrically interconnect said first metal interconnect layer, said second metal interconnect layer and said third metal interconnect layer at predetermined locations.

9. The method of claim **6**, wherein said transistors are at least spaced apart from each other by at least the minimum source/drain spacing rule of said transistors.

10. An electrical interconnection system to optimize layout of a periphery area in a memory device, comprising:

a plurality of sub-circuits in a periphery area of a silicon substrate, wherein each of said sub-circuits includes at least one electric circuit with a plurality of circuit components;

a first metal interconnect layer comprising a plurality of first metal layer lines that partially electrically connect the circuit components of said electric circuits, wherein said first metal layer lines are fabricated to be oriented to extend substantially in one direction;

a second metal interconnect layer comprising a plurality of second metal layer lines that complete the electrical connection of said circuit components of said electric circuits, wherein said second metal layer lines are fabricated to be oriented to extend substantially perpendicular to said first metal layer lines; and

a third metal interconnect layer comprising a plurality of third metal layer lines that electrically interconnect said plurality of sub-circuits, wherein said third metal layer lines are fabricated to be oriented to extend substantially parallel to said first metal layer lines.

11. The electrical interconnection system of claim **10**, wherein said plurality of electrical components comprise a plurality of transistors, a plurality of diodes and a plurality of resistors.

12. The electrical interconnection system of claim **11**, wherein said plurality of transistors are oriented to form a plurality of rows of transistors that run substantially parallel with said plurality of first metal layer lines.

13. The electrical interconnection system of claim **11**, wherein each of said plurality of transistors within said plurality of rows of transistors are positioned such that a drain and a source of each of said plurality of transistors is similarly oriented along an axis substantially parallel with said plurality of first metal lines.

14. The electrical interconnection system of claim **11**, wherein said transistors are spaced apart by at least the minimum source/drain spacing rule of said transistors.

* * * * *

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(12) **United States Patent**
McClain et al.

(10) **Patent No.: US 6,731,536 B1**
(45) **Date of Patent: May 4, 2004**

(54) **PASSWORD AND DYNAMIC PROTECTION OF FLASH MEMORY DATA**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 121 days.

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Related U.S. Application Data

(60) Provisional application No. 60/273,615, filed on Mar. 5, 2001.

(51) **Int. Cl.**[7] **G11C 7/00**

(52) **U.S. Cl.** **365/185.04**; 365/185.29; 365/189.01; 365/218

(58) **Field of Search** 365/185.04, 185.29, 365/189.01, 218

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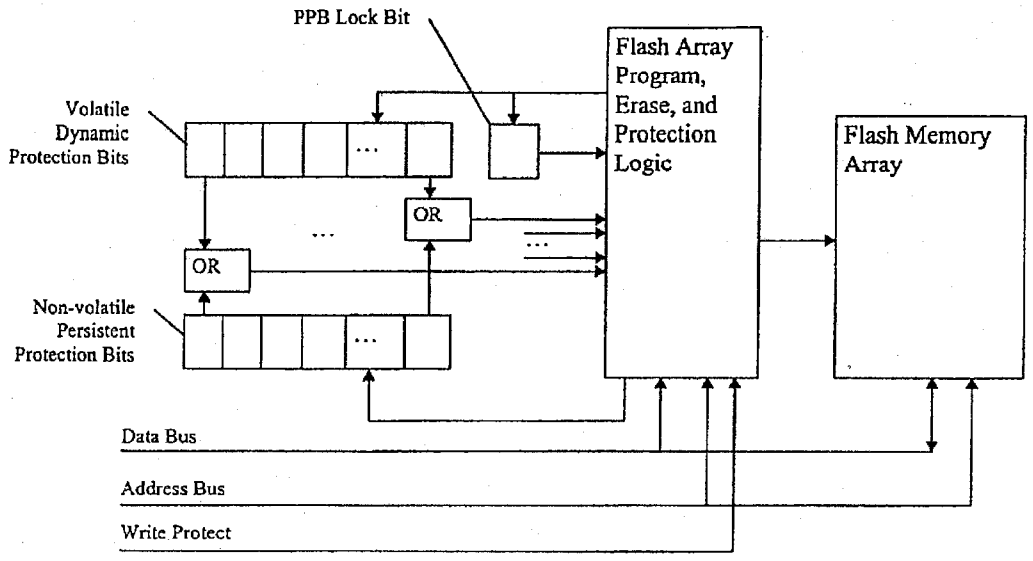
Primary Examiner—Viet Q. Nguyen

(57) **ABSTRACT**

In protecting Flash memory data, a flexible system and method provides for different levels of protection. It offers the ability to dynamically lock a sector of memory using a dynamic protection bit in volatile memory. It offers persistent locking of a sector using a non-volatile bit in memory and locking this status using a lock bit in volatile memory. It offers yet further protection by including a password mode which requires a password to clear the lock bit. The password is located in an unreadable, one time programmable area of the memory. The memory also includes areas, whose protection state is controlled by an input signal, for storing boot code in a protected manner.

28 Claims, 1 Drawing Sheet



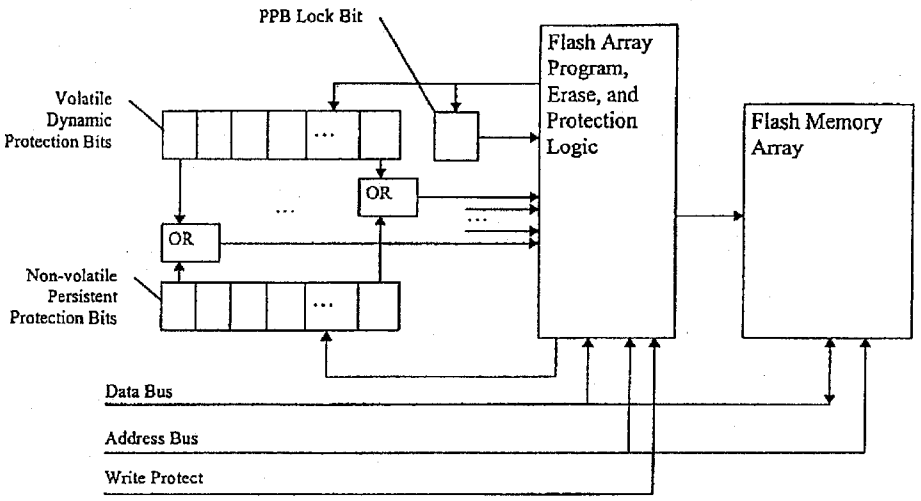

PPB Lock Bit
Volatile
Dynamic
Protection Bits
Non-volatile
Persistent
Protection Bits
OR
OR
Flash Array
Program,
Erase, and
Protection
Logic
Flash Memory
Array
Data Bus
Address Bus
Write Protect

Figure 1

PASSWORD AND DYNAMIC PROTECTION OF FLASH MEMORY DATA

This application claims the benefit of U.S. Provisional application Ser. No. 60/273,615 filed Mar. 5, 2001.

FIELD OF THE INVENTION

This invention relates to a method and means for protecting Flash memory data.

BACKGROUND OF THE INVENTION

As virtually every sector of technology moves toward microprocessor controlled functionality, the need for effective protection of code controlling the microprocessor becomes increasingly important. Flash memory devices are common prey for hackers wishing to circumvent or control the code by making changes thereto or by replacing the Flash memory. Protection systems, therefore, have been devised to prevent the code from being erased or altered. Flash memory is also susceptible to damage caused by unintentional and intentional signals received by the memory. Some methods of protecting data stored in Flash memories are designed to prevent unintended changes due to electrical noise, or software program errors. These methods rely on electrical noise filters or complex sequences of software commands, that are an unlikely result of random or unintended electrical or software activity. Some protection methods even prevent intentional software controlled changes such as an attack by a virus program intended to damage stored data.

One commonly used method to prevent changes to the code on the Flash is to require a high voltage signal, e.g., 12 V to be applied to a pin on the Flash memory. Such a method assumes a lack of physical access to the flash device that would allow changing the electrical signals connected to the Flash memory. One or more signal inputs of the Flash are required to be at certain voltage levels in order to enable changes to the Flash data Without a physical change to the signal connections, the required voltage is not available. However, if physical access is possible, the appropriate voltage can be applied and any protection overridden. Furthermore, such hardware controlled methods of preventing unauthorized changes of information stored in a Flash memory have the drawback that there is no way to control, by means of software, the signal inputs of the Flash which enable changes to the data protection circuit. Furthermore, while this protection method provides protection against hackers who have no physical access to the chip, it does not help in situations where the unauthorized person has physical access to the chips. For example, in the automotive industry the motor vehicle speed regulator chips are physically available to the owner. Thus, performance control parameters can readily be altered, thereby exposing the vehicle, the vehicle engine, and the driver to speeds and forces not contemplated or intended by the motor vehicle manufacturer. Illegal car tuning is something that is a serious concern in the automotive industry. Tuners typically charge in the vicinity of $1,000 for modifications that cost them no more than $5.00 to implement. The damage that is caused by these illegal changes is, however, very high, resulting in anything from blown engines, destroyed gear boxes, to killed people.

The prior art approach has further drawbacks insofar as 12 V signals are often not available in a system. It, therefore, makes it difficult to perform authorized changes to the chip.

Another traditional method of indicating which portions or sectors of data within the Flash memory are to be protected, makes use of non-volatile memory bits. These may only be programmed and erased a limited number of times, typically 100 to a few hundred cycles. Thus, the protection state of sectors must remain fairly static, software cannot simply turn protection on and off on a frequent basis during system operation in order to have residual benefit of added protection from unintended changes along with ease of access when changes are needed.

Another traditional protection method is to use boot code that verifies an expected check sum of the data in the Flash in order to detect any illegal alterations of parameters. This software managed protection may require one or more password codes to be presented in order to change the Flash. However, since this protection is all implemented in software, and the algorithm is placed in the Flash, the code can be read. Thus, the algorithm and the passwords can be determined.

The present invention seeks to address some of the drawbacks in the prior art solutions.

SUMMARY OF THE INVENTION

The invention provides two levels of protection for each sector of data, a persistent level, and a dynamic level. The persistent level of protection uses traditional non-volatile control memory bits in conjunction with the optional requirement for a password in order to change the state of the persistent protection bits. The dynamic level, on the other hand, is implemented with logic flip-flops that define register bits, which can be changed an unlimited number of times. This allows the software to turn on and off data protection as frequently as desired for those sectors that do not require persistent non-volatile protection.

According to the invention, there is provided a method of protecting Flash memory against alterations, comprising providing different degrees of protection including persistently locking a sector for preventing modification of the sector, and dynamically locking a sector which prevents modification of the sector without first resetting a protection bit.

A sector may also be left in an unlocked state, which allows the contents to be changed at will.

In order to persistently lock a sector, a persistent protection bit (PPB) is assigned in non-volatile.

In order to dynamically lock a sector, a dynamic protection bit (DPB) is assigned in a volatile memory. This volatile memory may take the form of flip-flops. Thus, the DPBs are individually modifiable through a write command. Also, after a power-up or a hardware reset all DPBs are reset.

A further level of protection can be applied to the persistent locking of the sectors, by making use of a PPB lock bit in volatile memory, which, when set, prevents the states of the PPBs being changed. Thus, changing the PPBs can only be achieved once the PPB lock bit is cleared.

Another level of protection can be achieved by holding a write protect pin low. This prevents certain sectors, e.g., the two outermost 8 kbyte sectors being changed. Thus, by maintaining boot code in these outermost sectors and holding the write protect (WP) pin low, boot code cannot be modified to interfere with the persistent sector protection settings defined at system initialization.

Yet a further level of protection is provided by including a password mode, requiring that a password, e.g., a 64-bit password, be entered in order to clear the PPB lock bit. The password may be fixed or may change from time to time. For example, a cyclic redundancy check (CRC), pseudo random

number generator, or hamming code could be adopted to define a dynamic password algorithm to produce the next valid password. When password mode is selected, the PPB lock bit is preferably in the active state when the device is first powered on or comes out of a reset cycle so that the persistent protection bits may only be changed after a valid password is provided. If the password is fixed, it is stored in a one time programmable or permanently lockable region of the Flash memory.

In order to select password mode, a password mode locking bit is assigned which permanently sets the Flash memory in password mode. Similarly a non-password mode locking bit is assigned which, once set, permanently prevents password mode being entered. Typically, both mode locking bits are in a cleared state, ready for setting by the OEM or end-user when the device is shipped from the manufacturer.

Once the password mode is locked the ability to change or read the password is disabled. In order to obstruct attempts at deriving the password by writing a program to sequentially try every permutation of the password, a time delay may be introduced, e.g., 2 microseconds between each attempt to clear the PPB lock bit. Instead, only a limited number of successive PPB lock bit clear commands may be permitted. Yet another alternative is to require a new power cycle between each PPB lock bit clear command.

Preferably the password is related to an electronic serial number (ESN) stored in the flash device, since the password is unreadable after the password mode is enabled. The ESN makes it possible to identify the specific memory device and retrieve its password from a database when the password is needed.

Further, according to the invention, there is provided a Flash memory having multiple degrees of protection, comprising a non-volatile storage area defining at least one persistent protection bit (PPB) which has to be cleared in order to change the contents of the memory, and a volatile storage area defining at least one dynamic protection bit (DPB), which has to be cleared in order to change the contents of the memory.

The volatile storage area further defines at least one PPB lock bit which, when set prevents the at least one PPB from being cleared. Typically each PPB lock bit can be cleared only by means of a power-up reset or provision of a password.

Preferably there is one PPB and one DPB per sector of the Flash memory, and one or more PPB lock bits each related to one or more sectors. If there are multiple PPB lock bits, each may be cleard by a different password.

Preferably the Flash memory includes a password or password generating mechanism in the non-volatile storage area in an area that is read and write protected. Preferably the Flash includes at least one mode selection bit for selecting password mode or non-password mode. The at least one mode selection bit is preferably located in a one time programmable portion of memory to permanently lock the memory into one or the other mode.

The Flash memory may further include a write protect pin to prevent programing or erasing of part of the Flash memory. The pin may be further protected by putting it under potting material. Alternatively, the boot sectors can be preprogrammed at the wafer level and the write protect pin not bonded out. In yet another alternative, the write protect could have an internal pull down and have the write protect pin not routed or not routed to an obvious place.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a Flash memory of the invention.

DETAILED DESCRIPTION OF THE INVENTION

A Flash memory device is shown in FIG. **1**, and includes a non-volatile memory region 10 and a volatile memory region 12. The bulk of the storage area in flash is non-volatile in nature, however, the present invention defines certain protection bits that may be volatile or non-volatile in nature and serve to prevent the contents of the flash being changed. For greater versatility, the present invention defines varying degrees of protection based on four considerations:

A. Whether the protection bit is defined in volatile or non-volatile memory;

B. Whether the protection bit itself may be prevented from changing state based on the state of a lock bit;

C. Whether a password is required to unlock the lock bit, and

D. Whether an external signal input is used to prevent changes being made to some sectors, independent of all other protection methods.

If the protection bit is defined in volatile memory, referred to as a Dynamic Protection Bit (DPB), it can be changed at will using software, and thus defines either a dynamic locked or unlocked state. In a preferred embodiment, one DPB is defined for each sector of the Flash memory. If the protection bit is in the non-volatile memory, referred to as a Persistent Protection Bit (PPB), it defines a persistently locked state when set. In a preferred embodiment, one PPB is defined for each sector. In a preferred embodiment, a PPB lock bit is provided in volatile memory to prevent PPBs from being altered. In one embodiment, only a single PPB lock bit is provided for the Flash memory, to lock or unlock all of the PPBs. It will, however, be appreciated that more than one PPB lock bit can be provided, e.g., one for each PPB.

The protection state for each sector is determined by the logical OR of the PPB and DPB related to that sector. Thus, for the sectors that have the PPBs cleared, the DPBs control whether or not the sector is protected or unprotected. By issuing a DPB write command sequence, the DPBs will be set or cleared, thus placing the corresponding sector in the protected or unprotected state. These may be referred to as dynamic locked or unlocked states, since it is easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. Since the DPBs are located in volatile memory, they may be set or cleared as often as is needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles since they are implemented in non-volatile memory. Thus, while individual PPBs may be set with a command, they must all be cleared as a group through a complex sequence of programs and erasing commands. Also, the PPBs are limited to approximately 100 erase cycles, due to the non-volatile nature of the bits.

The PPB lock bit, which is implemented in volatile memory, adds an additional level of protection. Once all PPBs are programmed to the desired setting, the PPB lock bit may be set to 1. Setting the PPB lock bit disables all program and erase commands to the non-volatile PPBs. In effect, the PPB lock bit locks the PPBs into their current state. The only way to clear the PPB lock is to go through a power cycle. System boot code can determine if any changes to the PPBs are needed, e.g., to allow a new system code to be downloaded. If no changes are needed, the boot

code can set the PPB lock to disable any further changes to the PPBs during system operation.

The write protect pin (WP#) adds a further level of hardware protection to the outermost 8 kbyte sectors. When this pin is low, it is not possible to change the contents of these two sectors. The sectors generally hold system boot code which includes the protection settings chosen for the Flash memory. Thus, the write protect pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are initially all unprotected. If there is a need to protect some of them, a simple DPB write command sequence is all that is necessary. The DPB write command for the dynamic sectors switches the DPBs to signify protected or unprotected state. In contrast, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB lock bit must be disabled which, in this embodiment, is done by either putting the device through a power cycle or hardware reset. In another embodiment, this can also be achieved using a software reset. As discussed below, the PPBs can then be changed to reflect the designed settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Table A is a table containing all possible combinations of the DPBs, PPBs, and PPB lock bit relating to the status of a sector. The protection state of a particular sector is the logical OR of the related DPBs and PPBs. If the PPB is set, and the PPB lock is set, the sector is protected and the protection cannot be removed until the next power cycle clears the PPB lock bit. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DPB then controls whether or not the sector is protected or unprotected.

TABLE A

DPB	PPB	PPB Lock	Sector State
0	0	0	Unprotected PPB and DPB are changeable
1	0	0	Protected - PPB and DPB are changeable
0	1	0	Protected - PPB and DPB are changeable
1	1	0	Protected - PPB and DPB are changeable
0	0	1	Unprotected - PPB not changeable, DPB is changeable
1	0	1	Protected - PPB not changeable, DPB is changeable
0	1	1	Protected - PPB not changeable, DPB is changeable
1	1	1	Protected - PPB not changeable, DPB is changeable

In a preferred embodiment, the Flash memory includes a non-password protection mode and a password protection mode. The former simply makes use of the DPBs, PPBs and one or more PPB lock bits to define the unlocked, dynamically locked or persistently locked states. When the device is first powered on, prior to any PPBs being set, the DPBs power up in a predetermined state, either set or cleared, such that all sectors are either protected or unprotected by the DPBs following the application of power or system reset. Unlike prior art protection solutions, non-password protection mode requires no unusual voltage levels and is therefore also referred to herein as Advanced Vcc-level protection mode.

The password protection mode allows a higher level of security than the advanced Vcc-level protection mode. It provides two added features, namely, when the device is first powered on or comes out of a reset cycle, the PPB lock bit is set to the locked state, rather than being cleared to the unlocked state, and furthermore, the only means of clearing the PPB lock bit is by writing a unique 64-bit password to the device. Otherwise, the password protection mode is identical to the non-password protection mode. The password is stored in a 1-time programmable region of the Flash memory. The password is used to clear the PPB lock bit. The password unlock command must be written to the Flash, along with a password. The Flash device internally compares the given password with the pre-programmed password. If they match, the PPB lock bit is cleared, and the PPBs can be altered. If they do not match, the Flash device does nothing. It will be appreciated that the password could instead be tied to erasing or writing to the PPB's, instead of to the clearing of the PPB lock bit. There is a built-in 2 to 4 μs delay for each password check. This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password. Once a password mode locking bit is set, the password is permanently set with no means to read, program or erase it.

In order to define which mode the Flash memory is to be operated in, a non-password protection mode locking bit and a password mode locking bit are defined in one-time programmable memory.

These bits permanently set the protection mode, thereby ensuring that the protection mode can no longer be changed. This guarantees that a malitious programmer can not later put the device into the alternative protection mode.

In order to select the password protection scheme, the customer must first program the password. The password is located in its own memory space and is accessible through the use of password program and verifying commands. A customer may perform password verification operations after programming the password. Once the desired password is programmed, the customer must set the password mode locking bit to permanently set the device into password protection mode and to disable all further commands to the password region. All program and read operations to the password region are thereafter ignored. Accordingly, there is no means of verifying the password once the password mode locking bit has been set. Preferably the password is somehow correlated to an electronic serial number (ESN) stored in the particular flash device. The ESN may be different for every Flash device. The ESN provides a means to identify which password should be used with a particular memory device after the password is made unreadable by entering the password protection mode. The password mode locking bit is not erasable and has the effect of disabling the non-password protection mode.

Instead of a fixed password, another embodiment uses the first programmed password as the initial value (seed) of a dynamic password that changes after each use according to some algorithm. It will be appreciated by those skilled in the art, that any one of a number of approaches can be adopted including a Linear Feedback Shift Register (LFSR), Cyclic Redundancy Check (CRC) generator, pseudo random number generator, or hamming code. Each time the password is used, it is logged into a particular area of memory. The internal password algorithm then reads the logged password and runs it through the dynamic password algorithm to produce the next valid password. In a preferred embodiment, the password algorithm has a seed value that can set a different starting point in the password generating algorithm for each memory. The seed value can also be a hidden number thereby providing the triple protection of a hidden starting point, an undisclosed algorithm, and a dynamic password. In one embodiment, an LFSR (simply some shift registers and exclusive OR feedback gates to the input of the

shift registers) is loaded with the initial password. The randomizing element involves a combination of selecting which feedback gates are used, and the number of shifts to take place to produce the dynamic password.

In order to avoid the password being found by writing a simple program to check all permutations of the password, a preferred embodiment disables password checking, after one password is supplied, until a power cycle has been completed, thereby requiring a power cycle each time a password check is made.

In another embodiment, each password check would require a significant time delay before an additional password check would be allowed. The delay would make trying all password combination take so long that it would not be a viable means to discover the password.

Typically, the Flash device is programmed by the system manufacturer or end user. The device initially operates in the non-password mode. The system manufacturer then may set the non-password protection mode locking bit, thereby disabling the password protection mode. Or, the system manufacturer may program the password and set the password mode locking bit, thereby disabling the non-password protection mode.

A preferred embodiment of the invention, further includes a hardware protection method. This involves the setting of a write protect pin which has the effect of protecting certain sectors, typically the sectors containing boot code. Even if the write protect pin is cleared, this does not circumvent the non-password or password protection features.

What is claimed is:

1. A method of protecting Flash memory against alterations, comprising

providing different degrees of protection including

persistently locking a sector for preventing modification of the sector, and

dynamically locking a sector which prevents modification of the sector without first resetting a protection bit.

2. A method of claim 1, wherein persistently locking a sector, includes assigning a persistent protection bit (PPB) in non-volatile memory.

3. A method of claim 1, wherein dynamically locking a sector, includes assigning a dynamic protection bit (DPB) in a volatile memory. This volatile memory may take the form of flip-flops.

4. A method of claim 3, wherein the DPBs are individually modifiable through a write command.

5. A method of claim 3, wherein after a power-up or a hardware reset all DPBs are either set or reset, depending on the desired default state.

6. A method of claim 2, further comprising a further level of protection applying to the persistent locking of the sectors, by making use of a PPB lock bit in volatile memory, which, when set, prevents the states of the PPBs being changed.

7. A method of claim 1, further comprising holding a write protect pin low to prevent certain sectors being changed.

8. A method of claim 7, further comprising maintaining boot code in said certain sectors.

9. A method of claim 6, further comprising including a password mode requiring that a password be entered in order to clear the PPB lock bit.

10. A method of claim 9, wherein the password is a fixed password.

11. A method of claim 9, wherein the password is variable and is produced by a dynamic password algorithm.

12. A method of claim 9, wherein when password mode is selected, the PPB lock bit is in a set state when the device is first powered on or comes out of a reset cycle.

13. A method of claim 10, wherein the password is stored in a one time programmable region of the Flash memory.

14. A method of claim 9, wherein a password mode locking bit is assigned which permanently sets the Flash memory in password mode.

15. A method of claim 9, wherein a non-password mode locking bit is assigned which, once set, permanently prevents entering the password mode.

16. A method of claim 9, wherein a time delay is introduced between each attempt to clear the PPB lock bit.

17. A method of claim 9, wherein only a limited number of successive attempts at clearing the PPB lock bit are permitted.

18. A method of claim 9, wherein a new power cycle is required between attempts to clear the PPB lock bit.

19. A method of claim 9, wherein the password is related to an electronic serial number (ESN) of the Flash memory.

20. A Flash memory having multiple degrees of protection, comprising

a non-volatile storage area defining at least one Persistent Protection Bit (PPB) which has to be cleared in order to change the contents of the memory, and

a volatile storage area defining at least one Dynamic Protection Bit (DPB), which has to be cleared in order to change the contents of the memory.

21. A method of claim 20, wherein the volatile storage area further defines at least one PPB lock bit which, when set prevents the at least one PPB from being cleared.

22. A method of claim 21, wherein each DPB and each PPB lock bit can be cleared only by means of a power-up or hardware reset.

23. A method of claim 21, wherein there is one PPB and one DPB per sector of the Flash memory, and a single global PPB lock bit for all sectors.

24. A Flash memory includes a password or password generating code in the non-volatile storage area in an area that is read and write protected.

25. A method of claim 24, wherein the password in the non-volatile storage area or generated by the code defines a password that has to be entered to clear the PPB lock bit.

26. A method of claim 25, wherein the Flash memory includes at least one mode selection bit for selecting password mode or non-password mode.

27. A method of claim 26, wherein the at least one mode selection bit is located in a one time programmable portion of the memory to permanently lock the memory into one or the other-mode.

28. A method of claim 20, wherein further including a write protect pin to prevent programming or erasing of part of the Flash memory.

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US006900124B1

(12) **United States Patent**
Kim et al.

(10) **Patent No.: US 6,900,124 B1**
(45) **Date of Patent: May 31, 2005**

(54) **PATTERNING FOR ELLIPTICAL V_{SS} CONTACT ON FLASH MEMORY**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 98 days.

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(22) Filed: **Sep. 3, 2003**

(51) **Int. Cl.**[7] **H01L 21/4763**

(52) **U.S. Cl.** **438/637**; 438/672; 438/638; 257/390; 257/316; 257/371

(58) **Field of Search** 438/637–638; 257/316–317, 390

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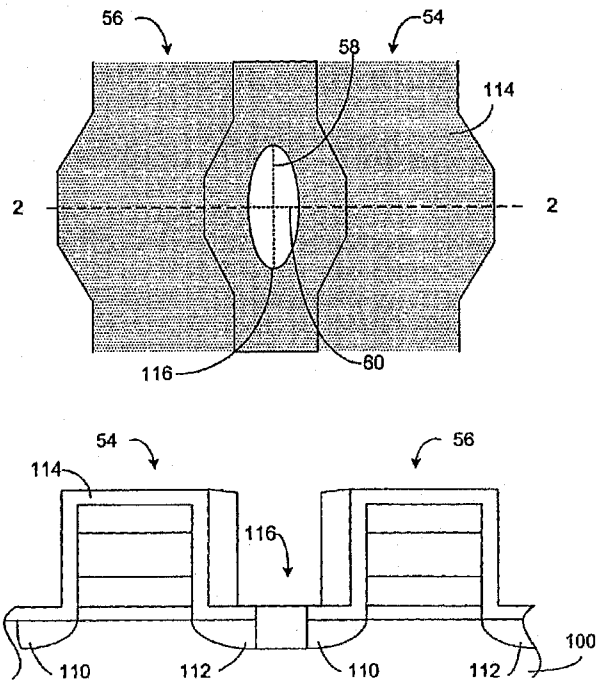
Primary Examiner—Dung A. Le
(74) *Attorney, Agent, or Firm*—Renner, Otto, Boisselle & Sklar, LLP

(57) **ABSTRACT**

A method of forming a contact in a flash memory device is disclosed. The method increases the depth of focus margin and the overlay margin between the contact and the stacked gate layers. A plurality of stacked gate layers are formed on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers. An interlayer insulating layer is deposited over the plurality of stacked gate layers, and a contact hole is patterned between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers. The contact hole is formed in an elongated shape, wherein a major axis of the contact hole is substantially parallel to the stacked gate layers. A conductive layer is deposited in the contact hole and excess conductive material is removed.

10 Claims, 5 Drawing Sheets



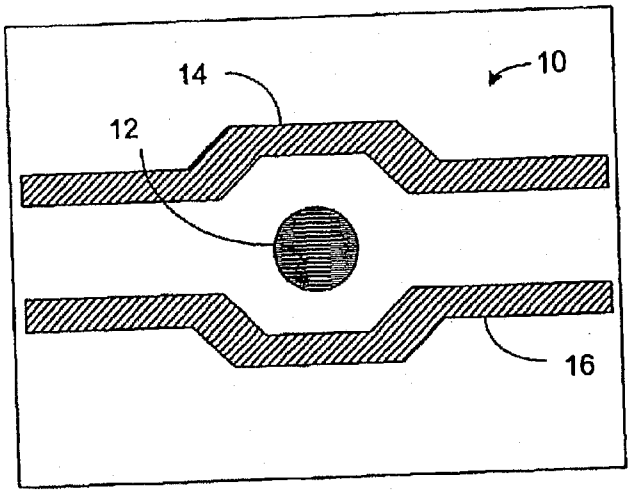


FIG. 1
(Prior Art)

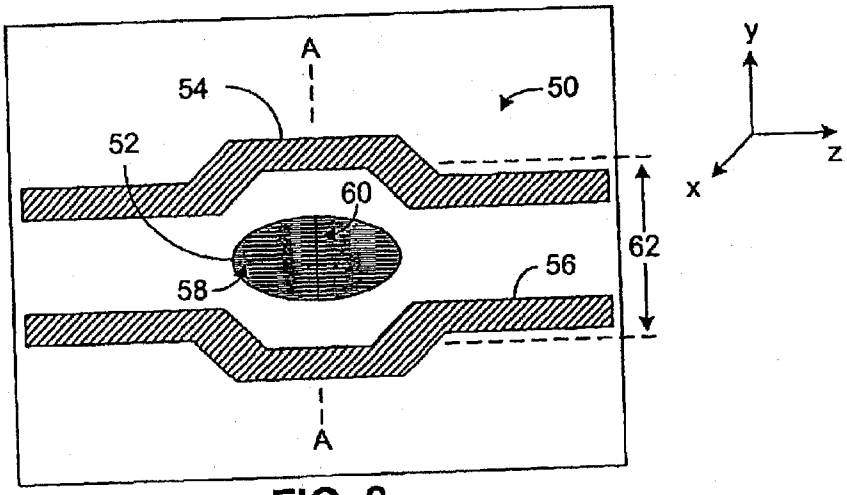


FIG. 2

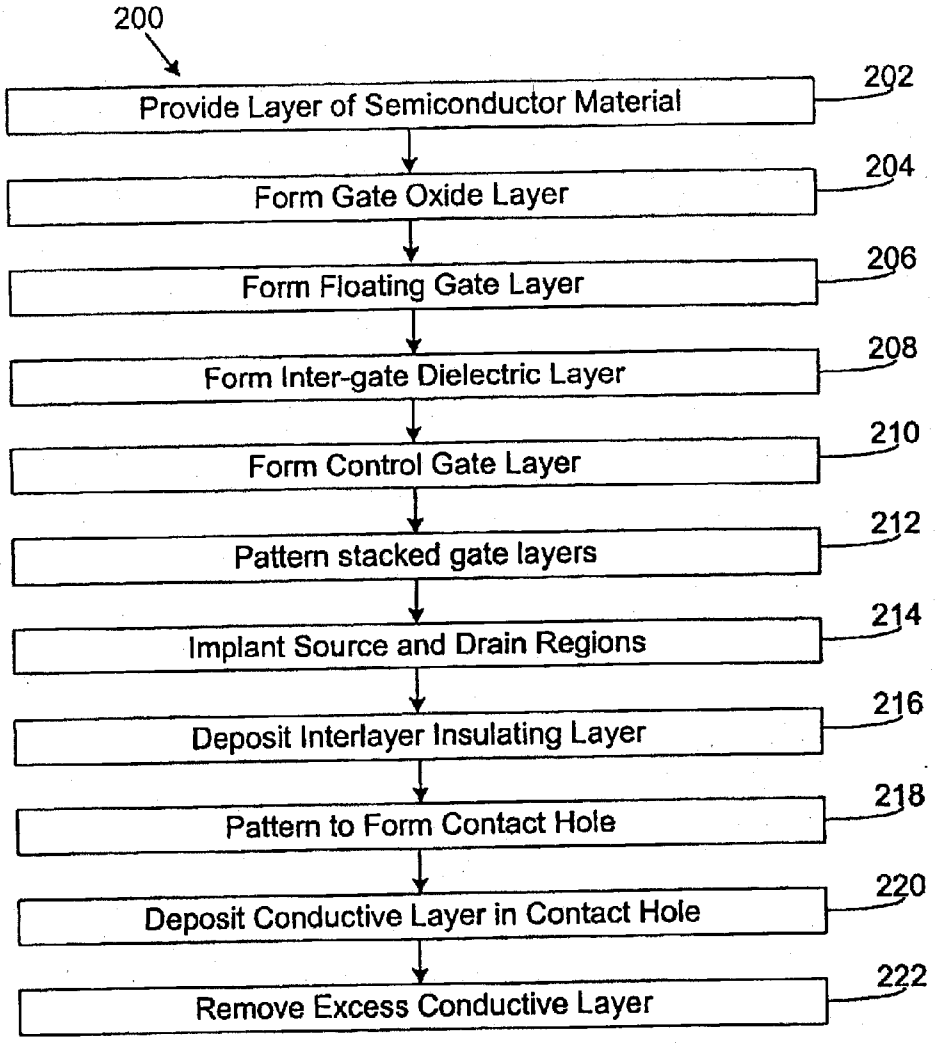

200
Provide Layer of Semiconductor Material
202
Form Gate Oxide Layer
204
Form Floating Gate Layer
206
Form Inter-gate Dielectric Layer
208
Form Control Gate Layer
210
Pattern stacked gate layers
212
Implant Source and Drain Regions
214
Deposit Interlayer Insulating Layer
216
Pattern to Form Contact Hole
218
Deposit Conductive Layer in Contact Hole
220
Remove Excess Conductive Layer
222

FIG. 3

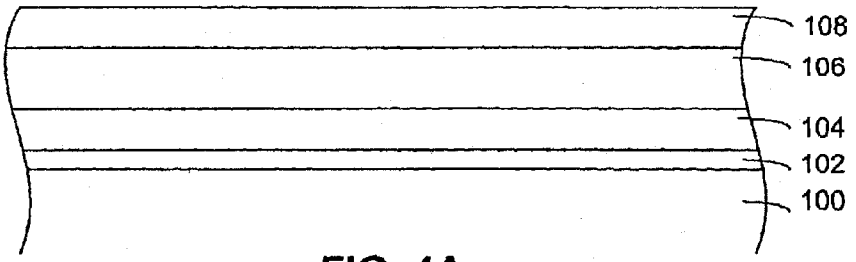


FIG. 4A

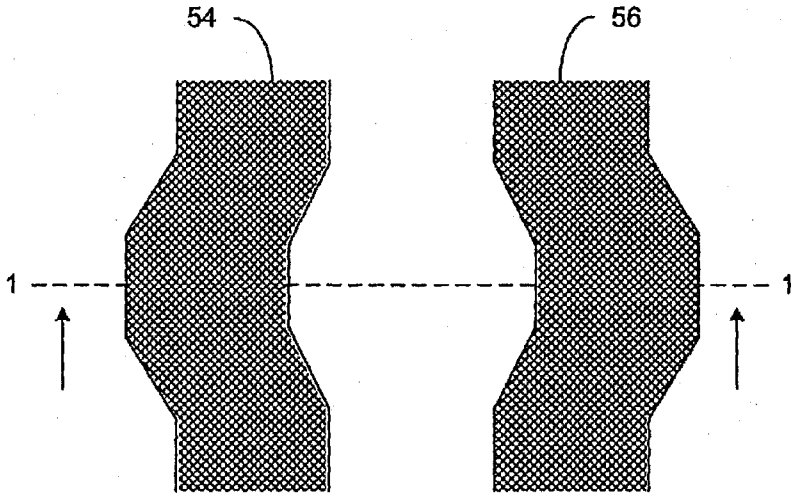


FIG. 4B

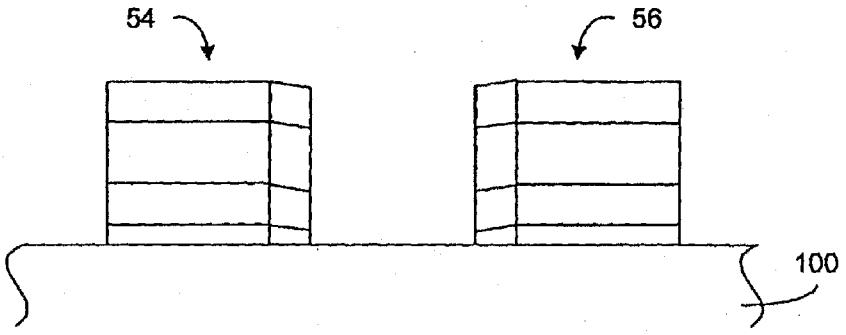


FIG. 4C

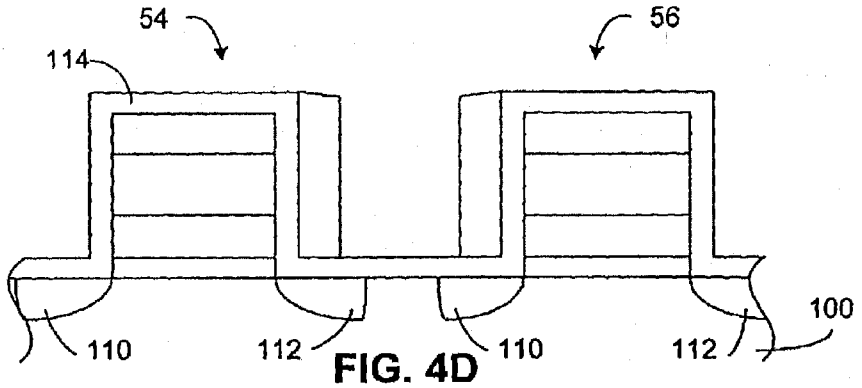


FIG. 4D

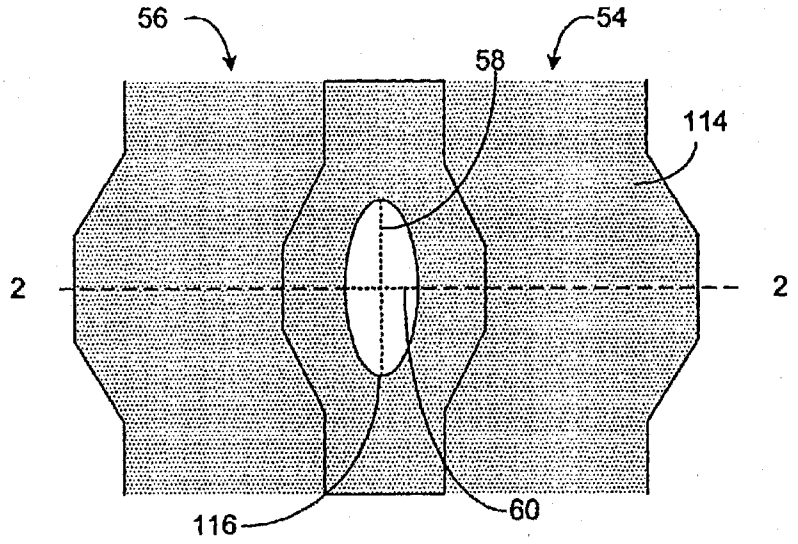


FIG. 4E

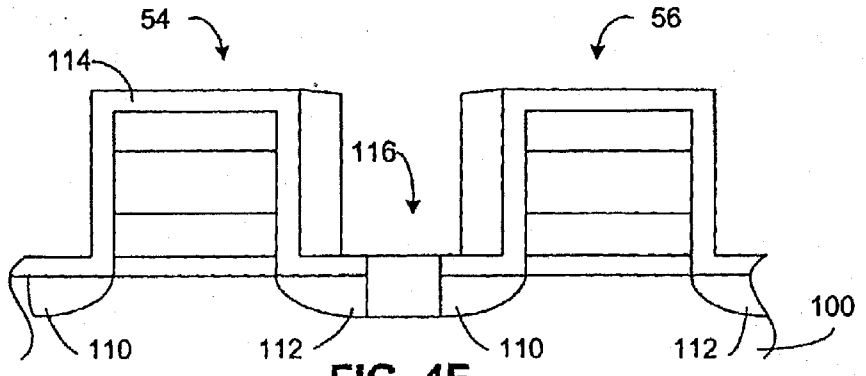


FIG. 4F

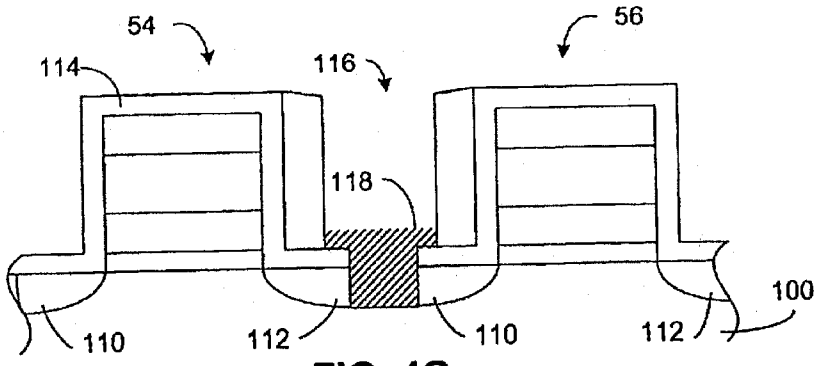


FIG. 4G

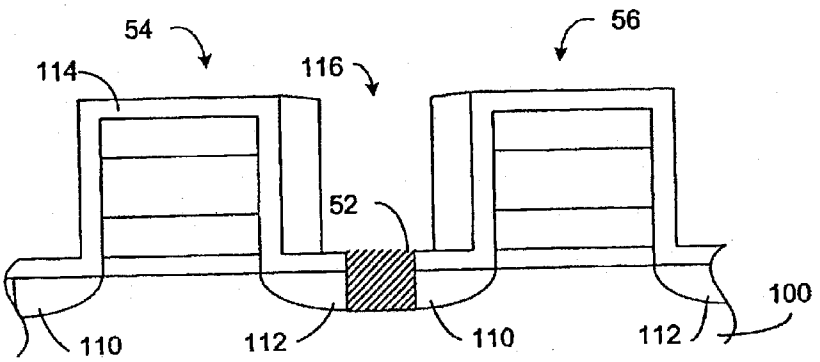


FIG. 4H

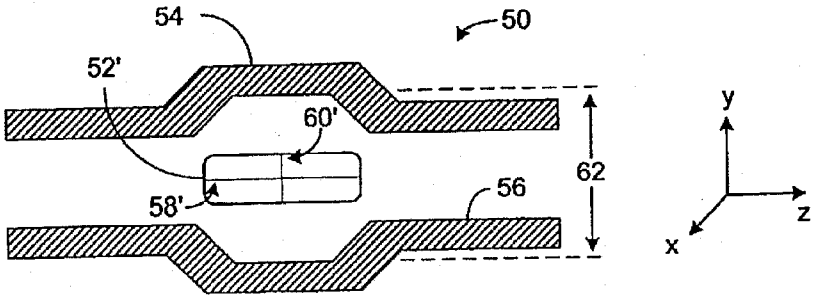


FIG. 5

PATTERNING FOR ELLIPTICAL V_{SS} CONTACT ON FLASH MEMORY

TECHNICAL FIELD

The present invention relates generally to the field of integrated circuit manufacture and, more particularly, to a method of improving the depth of focus and overlay margin within the stacked gate layer of a flash memory device.

BACKGROUND

Flash memory is a type of electronic memory media which can be rewritten and hold its content without power. Unlike dynamic random access memory (DRAM) and static random access memory (SRAM) memory chips, in which a single byte can be erased, flash memory is typically erased and written in fixed multi-bit blocks or sectors. Evolving out of electrically erasable read only memory (EEPROM) chip technology, which can be erased in place, flash memory is less expensive and more dense. This new category of EEPROMs has emerged as an important non-volatile memory which combines the advantages of EPROM density with EEPROM electrical erasability.

Conventional flash memories are constructed in a cell structure wherein a single bit of information is stored in each cell. In such single bit memory architectures, each cell typically includes a metal oxide semiconductor (MOS) transistor structure having a source, a drain, and a channel in a substrate or P-well, as well as a stacked gate structure overlying the channel. The stacked gate may further include a thin gate dielectric layer (sometimes referred to as a tunnel oxide) formed on the surface of the P-well. The stacked gate also includes a polysilicon floating gate overlying the tunnel oxide and an interpoly dielectric layer overlying the floating gate. The interpoly dielectric layer often is a multilayer insulator such as an oxide-nitride-oxide (ONO) layer having a nitride layer sandwiched between two oxide layers. Lastly, a polysilicon control gate overlies the interpoly dielectric layer.

Flash memory devices require a common source line, for example, to provide a connection to ground voltage (e.g., a V_{ss} contact) during a read operation. Generally, the V_{ss} contact is formed between stacked gate layers of the flash memory device. As is known in the art, contacts are among the most difficult features to pattern in semiconductor manufacturing. Not only are they smaller than any other circuit structure (except gates), but their images are intrinsically 3-dimensional, with the same contact having minimum feature size in both x and y direction and the laws of diffraction reducing the range of focus along the z-direction.

In a conventional method of forming the V_{ss} contact in a flash memory device, a gate oxide layer, a floating gate polysilicon layer, an inter-gate insulating layer and a control gate polysilicon layer are sequentially formed on a semiconductor substrate. Through photolithographic processes, the stacked layers are patterned to form a stacked gate pattern, e.g., a series of stacked gate layers. Impurities are implanted into the substrate using the stacked gate pattern as an implanting mask to form source/drain regions outside of the stacked gate pattern, and an interlayer insulating layer is deposited on the resulting structure. Using a photoetching process, the interlayer insulating layer is patterned between stacked gate layers to form a circular contact hole, exposing a predetermined region of the semiconductor substrate. A conductive layer is then deposited in the contact hole and on the interlayer insulating layer. A planarization process such as an etch-back or a chemical mechanical polish is carried out to leave the conductive layer in the contact hole and remove the portion of the conductive layer that is outside of the contact hole, thereby forming the V_{ss} contact.

Referring to FIG. **1**, a stacked gate pattern **10** of a prior art flash memory device is illustrated. A V_{ss} contact **12** is patterned between a first stacked gate layer **14** and a second stacked gate layer **16**. As stated previously, the V_{ss} contact **12** typically is circular in shape.

A pervasive trend in modern integrated circuit manufacture is to produce semiconductor devices, such as flash memory devices, that are as small as possible. The reduction in size of flash memory devices requires high resolution technology and a sufficient depth of focus (DOF), particularly in the formation of contact holes. DOF is the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate. As flash memory devices are reduced in size, each stacked gate layer **14, 16** of the stacked gate pattern **10** is formed closer to adjacent stacked gate layers, thus requiring a smaller V_{ss} contact **12**. As the V_{ss} contact **12** is reduced in size, DOF margin becomes an issue in patterning the V_{ss} contact. In present integrated circuit fabrication, DOF is becoming so small that it is a concern as to whether optical wafer steppers are capable of maintaining the image in focus. This problem is evident in forming components having small feature size, such as contact holes.

Another concern in integrated circuit manufacture is the lateral positioning between layers comprising the integrated circuit, which is known as overlay. As feature sizes shrink, the overlay tolerances must become smaller in order to minimize the creation of defective devices. The reduction in size of the flash memory device requires the V_{ss} contact **12** and adjacent stacked gate layers **14, 16** to be in closer proximity to one another, thus creating overlay margin issues.

As a result, there exists a need in the art for a method of patterning a V_{ss} contact in a flash memory device that improves the DOF margin and the overlay margin within the stacked gate layer.

SUMMARY OF THE INVENTION

According to one aspect of the invention, the invention is directed to a method of processing an integrated circuit wafer to form a contact in a flash memory device. The method can include forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; depositing an interlayer insulating layer over the plurality of stacked gate layers; patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elongated shape; and depositing a conductive layer in the contact hole.

Another aspect of the invention relates to flash memory device, including a plurality of stacked gate layers, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; and a contact formed between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact is formed in an elongated shape.

Other aspects, features, and advantages of the invention will become apparent from the following detailed description. It should be understood, however, that the detailed

description and specific examples, while indicating several embodiments of the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the present invention.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a schematic top view of a prior art V_{ss} contact formed between stacked gate layers of a flash memory device.

FIG. **2** is a schematic top view of a V_{ss} contact formed between stacked gate layers of a flash memory device in accordance with an embodiment of the present invention.

FIG. **3** is a flow diagram illustrating an exemplary embodiment of a method of processing a wafer in accordance with the present invention.

FIG. **4A** is a sectional view of a semiconductor wafer at a certain point during processing of the wafer using the method in accordance with an embodiment of the present invention.

FIG. **4B** is a top view of the semiconductor wafer of FIG. **4A** during another point of the wafer processing.

FIG. **4C** is a cross-section taken along the line **1**—**1** of FIG. **4B**.

FIG. **4D** is a sectional view of the semiconductor wafer during another point of the wafer processing.

FIG. **4E** is a top view of the semiconductor wafer of FIG. **4A** during yet another point of the wafer processing.

FIG. **4F** is a cross-section taken along the line **2**—**2** of FIG. **4E**.

FIG. **4G** is a sectional view of the semiconductor wafer during yet another point of the wafer processing.

FIG. **4H** is a sectional view of the semiconductor wafer during yet another point of the wafer processing.

FIG. **5** is a schematic top view of a V_{ss} contact formed between stacked gate layers of a flash memory device in accordance with another embodiment of the present invention.

DISCLOSURE OF INVENTION

In the detailed description that follows, corresponding components have been given the same reference numerals, regardless of whether they are shown in different embodiments of the present invention or at difference times during a wafer processing method. To illustrate the present invention in a clear and concise manner, the drawings may not necessarily be to scale.

Referring to FIG. **2**, a stacked gate pattern **50** of a flash memory device in accordance with an embodiment of the invention is illustrated. The stacked gate pattern **50** includes a plurality of stacked gate layers **54**, **56**. As can bee seen in FIG. **2**, the stacked gates layers **54**, **56** of the stacked gate pattern **50** form a series of rows, and the rows are substantially parallel to each other.

To assist in describing the invention, the stacked gates layers **54**, **56** can be described with respect to a 3 dimensional Cartesian coordinate system. With respect to FIG. **2**, for example, the z-axis is represented as the horizontal component (e.g., left to right), the y-axis is represented as the vertical component (e.g., bottom to top), and the x-axis is represented as the depth component (e.g., coming out of the page). Thus, the "rows" of stacked gate layers lie in the z-axis, e.g., they form a line that extends along the z-axis, while the width and height components of each stacked gate layer lie in the y-axis and the x-axis respectively.

A V_{ss} contact **52** is formed between the first stacked gate layer **54** and the second stacked gate layer **56**. The V_{ss} contact is formed in an elongated shape, such as an ellipse, for example, wherein a major axis **58** of the ellipse (i.e., the axis that passes through the foci of the ellipse) is substantially parallel to the stacked gate layers **54**, **56**, and the minor axis **60** of the ellipse (i.e. the axis perpendicular to the major axis at the midpoint between the foci) is substantially perpendicular to the stacked gate layers **54**, **56**.

Since the major axis **58** of the ellipse is substantially parallel to the rows of stacked gate layers **54**, **56** and the rows of stacked gate layers lie in the z-axis, it follows that the major axis **58** of the ellipse also lies in the z-axis. In light of the above and with reference to FIG. **2**, it follows that the minor axis **60** of the ellipse lies in the y-axis. As will be explained in more detail below, the elongated shape provides a contact pattern that minimizes DOF and overlay issues during the fabrication of a flash memory device.

Eccentricity is a numerical value that determines the shape of an ellipse and is defined as the ratio of the distance between the foci to the length of the major axis. Eccentricity is always less than 1, and is expressed by the equation

$$\frac{\sqrt{(a^2 - b^2)}}{a} \qquad \text{Eq. 1}$$

where "a" is one half the length of the ellipse's major axis, and "b" is one half the length of the ellipse's minor axis. A perfectly circular ellipse has an eccentricity of 0, while an extremely long and narrow ellipse has an eccentricity that approaches 1. Thus, an elliptical contact having an eccentricity greater than zero, by definition, is not a perfect circle. Such an elliptical contact has a long or wide portion (the major axis) and a narrow or thin portion (the minor axis).

As packing densities of flash memory devices increase, the separation **62** between stacked gate layers is reduced. By forming an elliptical V_{ss} contact between stacked gate layers with its minor axis **60** substantially perpendicular to the stacked gate layers **54**, **56**, the length "b" of the minor axis **60** is constrained by one half of the separation **62** between stacked gate layers, plus any required overlay margin. This same constraint is imposed on prior art circular V_{ss} contacts, wherein a radius "r", of the circular contact must fit within the same limitations.

Thus, as the distance of separation **62** between stacked gate layers **54**, **56** is reduced, the radius "r" of the circular V_{ss} contact and the minor axis "b" of the elliptical V_{ss} contact also must be reduced. A reduction in the radius of the circular V_{ss} contact has the effect of reducing the size of the circular V_{ss} contact in all directions since, by definition, a circle is composed of all points having a distance "r" from a center point. As the radius is reduced, the entire circle is reduced.

The elliptical V_{ss} contact **52**, on the other hand, only is reduced along the minor axis **60**. The major axis **58** is not affected by the reduction in separation between stacked gate layers **54**, **56**. Therefore, the elliptical V_{ss} contact **52** formed between stacked gate layers **54**, **56** can occupy a larger area than a circular V_{ss} contact formed between the same stacked gate layers. Moreover, the elliptical V_{ss} contact can be dimensioned along its major axis **58** so as to maintain feature size above a threshold value, and thus minimize DOF issues. For example, the length of the major axis **58** can be increased as the length of the minor axis **60** is decreased, thereby maintaining the contact area above a threshold value.

Furthermore, since the elliptical V_{ss} contact **52** can overcome DOF issues by maintaining feature size above a threshold value (e.g., by increasing the major axis **58**), the minor axis **60** can be reduced to a greater extent than can the radius "r" of a circular contact. This provides an increase in overlay margin between the V_{ss} contact **52** and the stacked gate layers **54, 56** when compared to a circular V_{ss} contact. In one embodiment, the ratio of the minor axis length "b" relative to the major axis length "a" (e.g., a/b) is about 1.1 to 1.4, or in other words, the length of the minor axis is about 71 percent to about 90 percent of the length of the major axis.

Referring to the flowchart **200** of FIG. **3** in conjunction with the diagrams of FIG. 4A–FIG. 4H, exemplary processing steps for fabricating the V_{ss} contact **52** between stacked gate layers **54, 56** of a flash memory device are shown.

The process begins with a layer of semiconductor material **100** as shown in step **202**. In step **204**, a gate oxide layer **102** is deposited or grown on a semiconductor substrate **100**. Deposition or growth may be performed through various well known processes, such as chemical vapor deposition (CVD) or dry oxidation in an oxygen and nitrogen ambient atmosphere, for example. Following the formation of the gate oxide layer **102**, a floating gate layer **104** is deposited over the gate oxide layer in step **206**, and in step **208** an inter-gate dielectric layer **106** is deposited over the floating gate layer **104**. The inter-gate dielectric layer **106** typically is an oxide-nitride-oxide (ONO) composition and is formed using conventional techniques. For example, the ONO layer can be formed in a three-stage process, which includes forming a first film of silicon dioxide, depositing a film of silicon nitride on the silicon dioxide, and then depositing a second film of silicon dioxide on the silicon nitride film.

At step **210**, a control gate layer **108** is formed over the intergate dielectric layer **106**. Formation of the control gate layer **108** includes, for example, depositing a layer of polysilicon material on the surface of the inter-gate dielectric layer **106** using low pressure chemical vapor deposition as is known by those skilled in the art. Using conventional photolithographic processes, the stacked gate layer is patterned at step **212** to form a stacked gate pattern, e.g., stacked gate layers **54, 56**, as shown in FIG. **4B** and FIG. **4C**.

Next at step **214**, impurities are implanted into the substrate **100** using the stacked gate pattern as an implanting mask to form source **110** and drain **112** regions outside the stacked gate pattern, as is conventional. At step **216**, an interlayer insulating layer **114** is deposited on the resulting structure, as shown in FIG. **4D**. The interlayer insulating layer **114**, for example, can be formed by depositing a silicon oxide film on the stacked gate pattern by means of sputtering or CVD and subsequently polishing the silicon oxide film by chemical mechanical polish (CMP). Alternatively, the interlayer insulating layer **114** may be a multilayer film such as a silicon nitride film, an SOG (spin on glass) film or a BPSG (boron phosphor silicate lass) film.

Moving to step **218**, a V_{ss} contact hole **116** is patterned in the interlayer insulating layer **114** between stacked gate layers **54, 56** using conventional photolithographic techniques, as shown in FIG. **4E** and FIG. **4F**. As disclosed previously, the V_{ss} contact hole **116** is patterned in an elliptical shape, wherein the minor axis **60** of the ellipse is substantially perpendicular to the stacked gate layers **54, 56** and the major axis **58** of the ellipse is substantially parallel to the stacked gate layers **54, 56**.

At step **220**, the contact hole **116** is filled with a suitable conductive material (e.g., a metal, a metal containing compound or a semiconductor). For example, a conductive layer **118** such as a doped polysilicon layer or a metal polycide layer is deposited in the contact hole **116** and on the interlayer insulating layer **114** as shown in FIG. **4G**. Moving to step **222**, a planarization process such as an etch-back or a chemical mechanical polish is carried out to leave the conductive layer in the contact hole and remove the portion of the conductive layer that is outside of the contact hole, thereby forming the V_{ss} contact **52** as shown in FIG. **4H**.

As one skilled in the art will appreciate, the exemplary method described herein can be modified. For example, certain steps can be omitted, certain steps can be carried out concurrently, and other steps can be added.

Referring now to FIG. **5**, a stacked gate pattern **50'** of a flash memory device in accordance with another embodiment of the invention is illustrated. The stacked gate pattern **50'** includes a plurality of stacked gate layers **54, 56**. A V_{ss} contact **52'** is formed between the first stacked gate layer **54** and the second stacked gate layer **56**. The V_{ss} contact is formed in the shape of a rectangle, wherein a first pair of sides **300** are longer than a second pair of sides **302**. The first pair of sides **300** lie in the z-axis and are substantially parallel to the stacked gate layers **54, 56**. The second pair of sides **302** lie in the y-axis and are substantially perpendicular to the stacked gate layers **54, 56**. With respect to the rectangular V_{ss} contact **52'**, a major axis **58'** is defined as an axis parallel to the first pair of sides **300** and intersecting a midpoint of the second pair of sides **302**, and a minor axis **60'** is defined as an axis parallel to the second pair of sides **302** and intersecting a midpoint of the first pair of sides **300**.

As was described previously with respect to the elliptical V_{ss} contact **52**, the rectangular V_{ss} contact **52'** formed between stacked gate layers **54, 56** can occupy a larger area than a circular V_{ss} contact formed between the same stacked gate layers. Additionally, the rectangular V_{ss} contact **52'** can be dimensioned along the z-axis so as to maintain feature size above a threshold value, and thus minimize DOF issues. For example, the length of the first pair of sides **300** can be increased as the length of the second pair of sides **302** are decreased, thereby maintaining the contact area above a threshold value.

Furthermore, since the first pair of sides **300** of the rectangular V_{ss} contact **52'** can be increased to maintain feature size above a threshold value, the length of the second pair of sides **302** can be reduced to a greater extent than can the radius "r" of a circular contact. This provides an increase in overlay-Margin between the V_{ss} contact **62'** and the stacked gate layers **54, 56** when compared to a circular V^{ss} contact. In one embodiment, the ratio of the second pair of sides **302** relative to the first pair of sides **300** (first pair/second pair) is about 1.1 to 1.4, or in other words, the length of the second pair of sides **302** are about 71 percent to about 90 percent of the length of the first pair of sides **300**.

Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto. For example, while the exemplary embodiment has been illustrated using a floating gate memory cell, it will be appreciated by those skilled in the art that the invention also may be applied to a flash memory device employing a silicon-oxide-nitride-oxide-silicon (SONOS) memory cell.

What is claimed is:

1. A method of forming a contact in a flash memory device that improves the depth of focus (DOF) margin and the overlay margin between a plurality of stacked gate layers and the respective contact, comprising the steps of:

forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers;

depositing an interlayer insulating layer over the plurality of stacked gate layers;

patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elliptical shape having a major axis and a minor axis, and the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit; and

depositing a conductive layer in the contact hole.

2. The method of claim **1**, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes aligning the major axis of the contact hole substantially parallel to the predefined direction of the stacked gate layers.

3. The method of claim **1**, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes aligning the minor axis of the contact hole substantially perpendicular to the predefined direction of the stacked gate layers.

4. The method of claim **1**, further comprising the step of:

removing a portion of the conductive layer that is outside the contact hole to leave the conductive layer in the contact hole.

5. The method of claim **1**, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes forming the minor axis of the contact hole to be about 71 percent to about 90 percent of a major axis of the contact hole.

6. A flash memory device, comprising:

a plurality of stacked gate layers, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; and

a contact formed between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact is formed in an elliptical shape.

7. The flash memory device of claim **6**, wherein the contact includes a major axis, and the major axis is substantially parallel to the predefined direction of the stacked gate layers.

8. The flash memory device of claim **6**, wherein the contact includes a minor axis, and the minor axis is substantially perpendicular to the predefined direction of the stacked gate layers.

9. The flash memory device of claim **6**, wherein the contact is a V_{ss} contact.

10. The flash memory device claim **6**, wherein a minor axis of the contact is about 71 percent to about 90 percent of a major axis of the contact.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

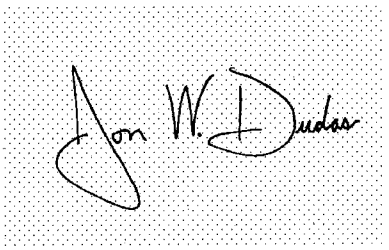
PATENT NO. : 6,900,124 B1
DATED : May 31, 2005
INVENTOR(S) : Kim et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6,
Line 46, replace "contact 62'" with -- contact 52' --

Signed and Sealed this

Ninth Day of August, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office

US007018922B1

(12) **United States Patent**
Kim et al.

(10) **Patent No.: US 7,018,922 B1**
(45) **Date of Patent: *Mar. 28, 2006**

(54) **PATTERNING FOR ELONGATED V_{SS} CONTACT FLASH MEMORY**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/968,713**

(22) Filed: **Oct. 19, 2004**

Related U.S. Application Data

(63) Continuation of application No. 10/654,739, filed on Sep. 3, 2003, now Pat. No. 6,900,124.

(51) **Int. Cl.**
H01L 21/4763 (2006.01)

(52) **U.S. Cl.** **438/637**; 438/638; 438/673; 257/316; 257/317

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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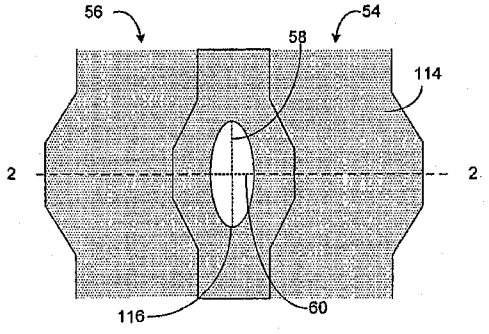
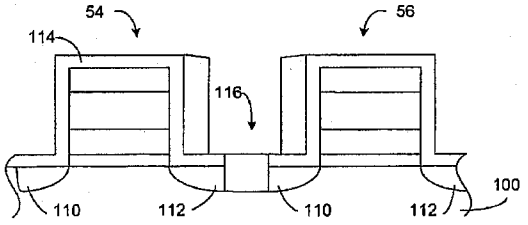
Primary Examiner—Dung A. Le
(74) *Attorney, Agent, or Firm*—Renner, Otto, Boisselle & Sklar, LLP

(57) **ABSTRACT**

A method of forming a contact in a flash memory device is disclosed. The method increases the depth of focus margin and the overlay margin between the contact and the stacked gate layers. A plurality of stacked gate layers are formed on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers. An interlayer insulating layer is deposited over the plurality of stacked gate layers, and a contact hole is patterned between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers. The contact hole is formed in an elongated shape, wherein a major axis of the contact hole is substantially parallel to the stacked gate layers. A conductive layer is deposited in the contact hole and excess conductive material is removed.

7 Claims, 5 Drawing Sheets





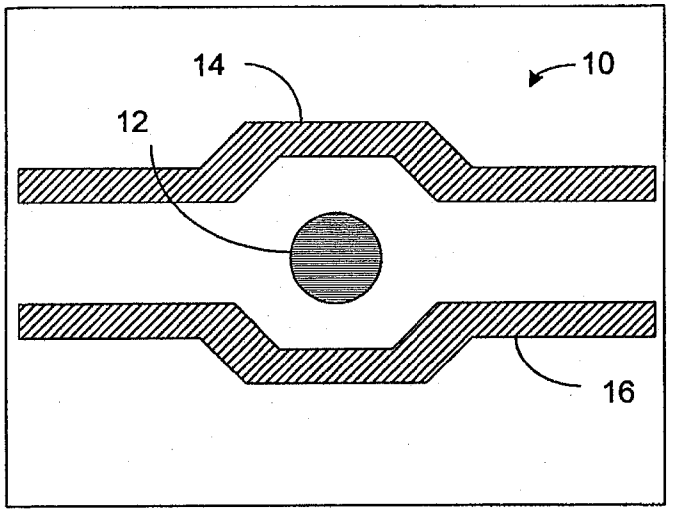


FIG. 1
(Prior Art)

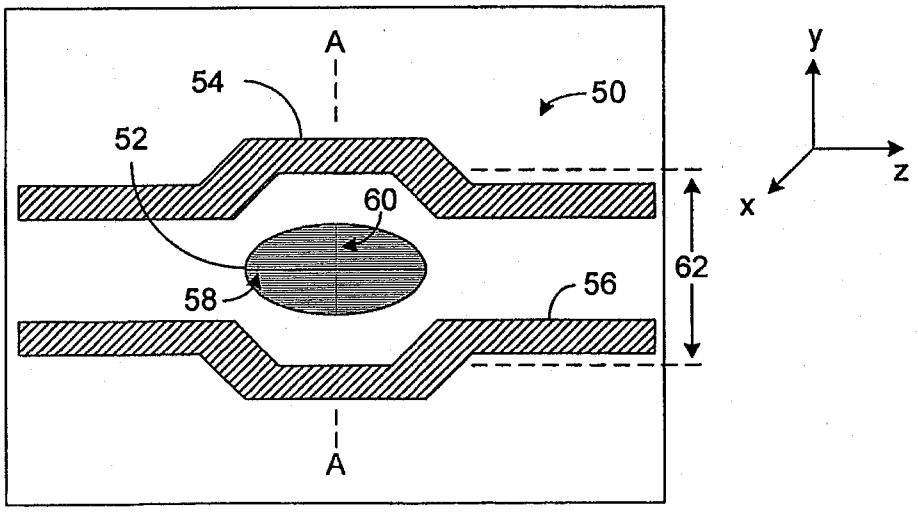


FIG. 2

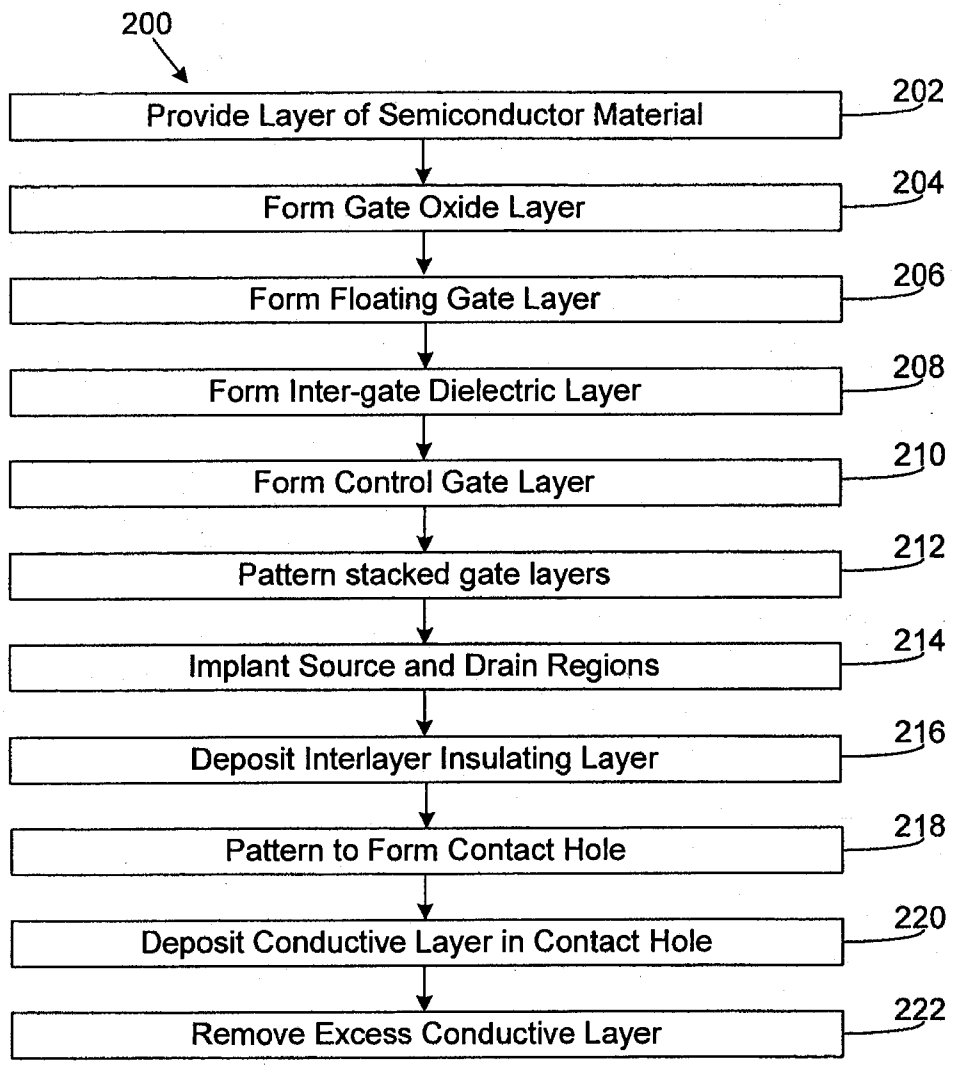

200
Provide Layer of Semiconductor Material
202
Form Gate Oxide Layer
204
Form Floating Gate Layer
206
Form Inter-gate Dielectric Layer
208
Form Control Gate Layer
210
Pattern stacked gate layers
212
Implant Source and Drain Regions
214
Deposit Interlayer Insulating Layer
216
Pattern to Form Contact Hole
218
Deposit Conductive Layer in Contact Hole
220
Remove Excess Conductive Layer
222

FIG. 3

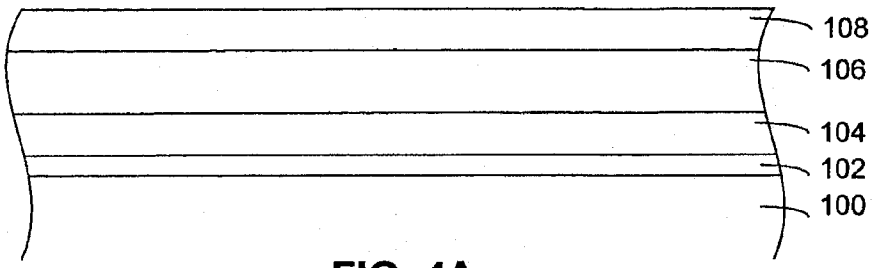


FIG. 4A

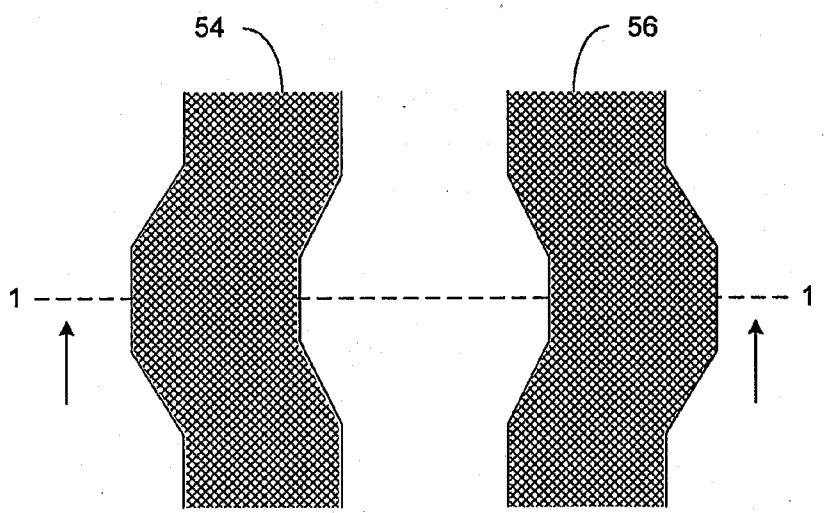


FIG. 4B

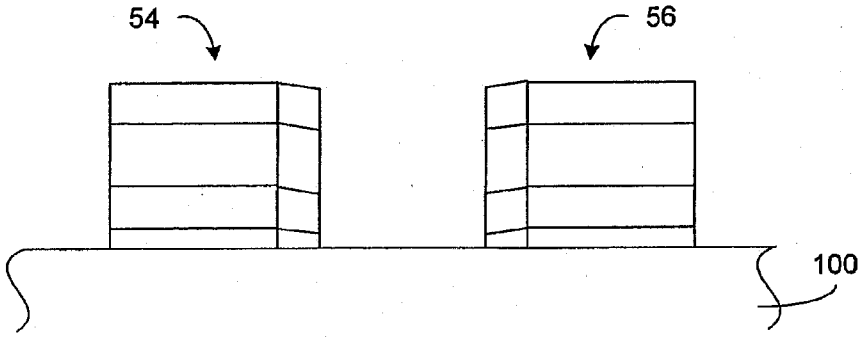


FIG. 4C

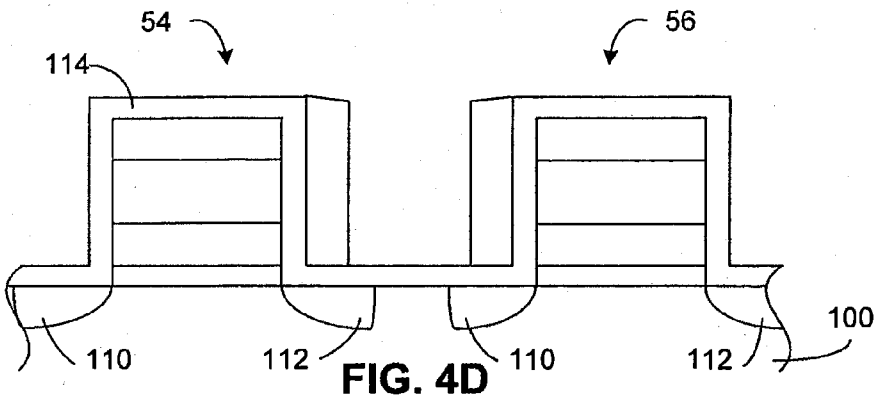


FIG. 4D

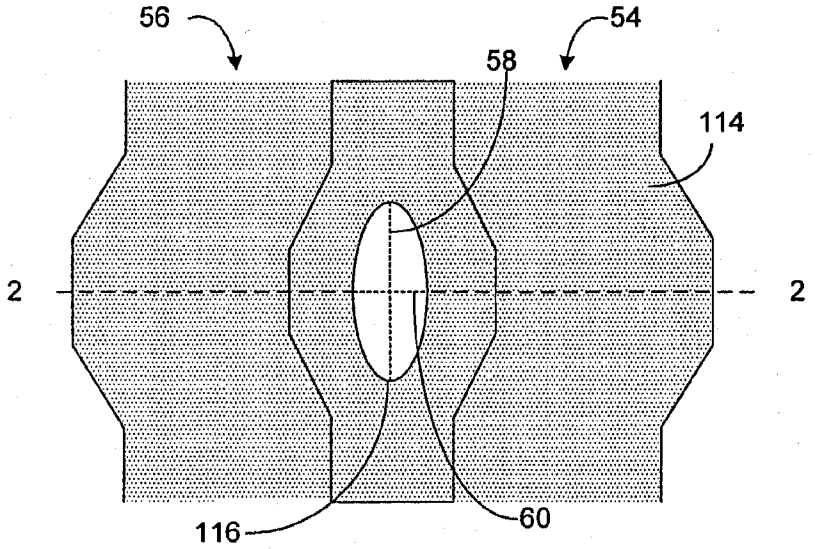


FIG. 4E

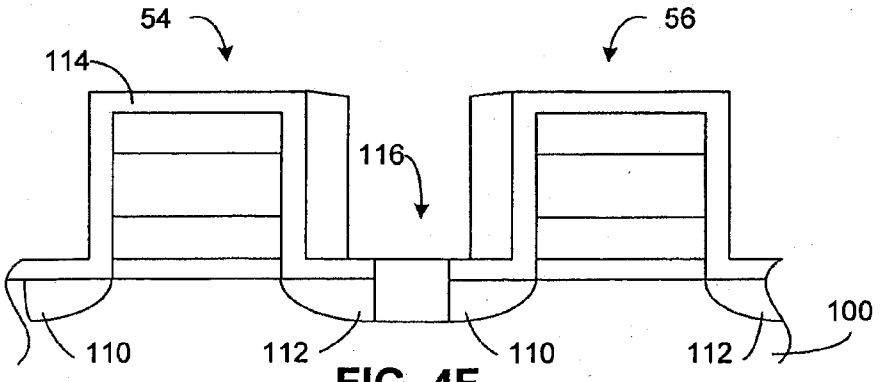


FIG. 4F

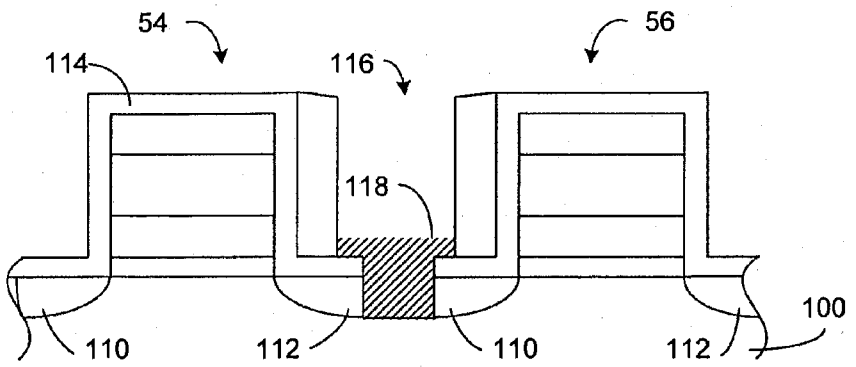


FIG. 4G

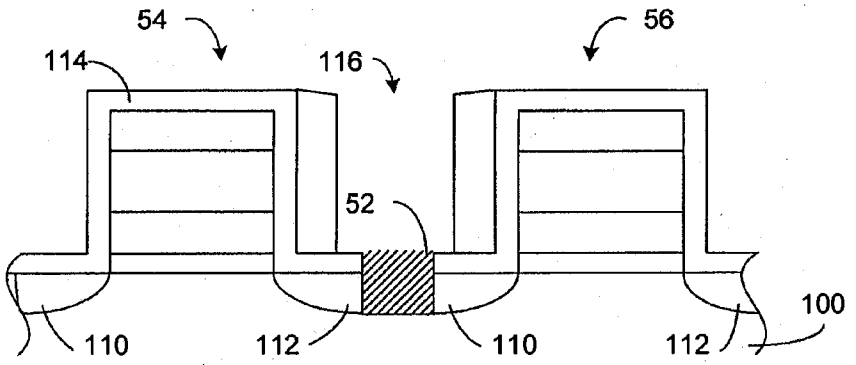


FIG. 4H

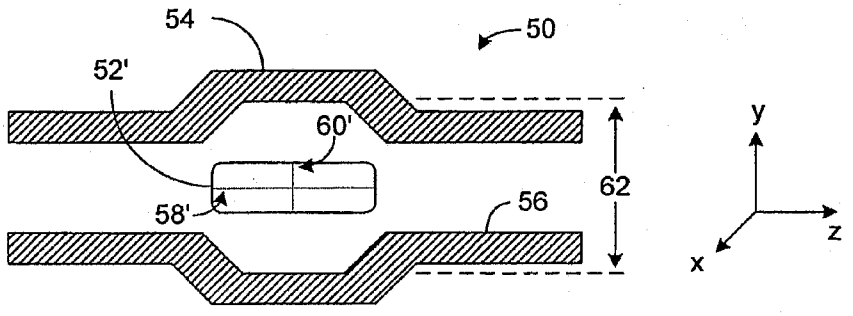


FIG. 5

PATTERNING FOR ELONGATED V_{SS} CONTACT FLASH MEMORY

This application is a continuation of U.S. patent application Ser. No. 10/654,379 filed on Sep. 3, 2003 now U.S. Pat. No. 6,900,124, which is hereby incorporated herein by reference in its entirety.

TECHNICAL FIELD

The present invention relates generally to the field of integrated circuit manufacture and, more particularly, to a method of improving the depth of focus and overlay margin within the stacked gate layer of a flash memory device.

BACKGROUND

Flash memory is a type of electronic memory media which can be rewritten and hold its content without power. Unlike dynamic random access memory (DRAM) and static random access memory (SRAM) memory chips, in which a single byte can be erased, flash memory is typically erased and written in fixed multi-bit blocks or sectors. Evolving out of electrically erasable read only memory (EEPROM) chip technology, which can be erased in place, flash memory is less expensive and more dense. This new category of EEPROMs has emerged as an important non-volatile memory which combines the advantages of EPROM density with EEPROM electrical erasability.

Conventional flash memories are constructed in a cell structure wherein a single bit of information is stored in each cell. In such single bit memory architectures, each cell typically includes a metal oxide semiconductor (MOS) transistor structure having a source, a drain, and a channel in a substrate or P-well, as well as a stacked gate structure overlying the channel. The stacked gate may further include a thin gate dielectric layer (sometimes referred to as a tunnel oxide) formed on the surface of the P-well. The stacked gate also includes a polysilicon floating gate overlying the tunnel oxide and an interpoly dielectric layer overlying the floating gate. The interpoly dielectric layer often is a multilayer insulator such as an oxide-nitride-oxide (ONO) layer having a nitride layer sandwiched between two oxide layers. Lastly, a polysilicon control gate overlies the interpoly dielectric layer.

Flash memory devices require a common source line, for example, to provide a connection to ground voltage (e.g., a V_{SS} contact) during a read operation. Generally, the V_{SS} contact is formed between stacked gate layers of the flash memory device. As is known in the art, contacts are among the most difficult features to pattern in semiconductor manufacturing. Not only are they smaller than any other circuit structure (except gates), but their images are intrinsically 3-dimensional, with the same contact having minimum feature size in both x and y direction and the laws of diffraction reducing the range of focus along the z-direction.

In a conventional method of forming the V_{SS} contact in a flash memory device, a gate oxide layer, a floating gate polysilicon layer, an inter-gate insulating layer and a control gate polysilicon layer are sequentially formed on a semiconductor substrate. Through photolithographic processes, the stacked layers are patterned to form a stacked gate pattern, e.g., a series of stacked gate layers. Impurities are implanted into the substrate using the stacked gate pattern as an implanting mask to form source/drain regions outside of the stacked gate pattern, and an interlayer insulating layer is deposited on the resulting structure. Using a photoetching process, the interlayer insulating layer is patterned between stacked gate layers to form a circular contact hole, exposing a predetermined region of the semiconductor substrate. A conductive layer is then deposited in the contact hole and on the interlayer insulating layer. A planarization process such as an etch-back or a chemical mechanical polish is carried out to leave the conductive layer in the contact hole and remove the portion of the conductive layer that is outside of the contact hole, thereby forming the V_{SS} contact.

Referring to FIG. **1**, a stacked gate pattern **10** of a prior art flash memory device is illustrated. A V_{SS} contact **12** is patterned between a first stacked gate layer **14** and a second stacked gate layer **16**. As stated previously, the V_{SS} contact **12** typically is circular in shape.

A pervasive trend in modern integrated circuit manufacture is to produce semiconductor devices, such as flash memory devices, that are as small as possible. The reduction in size of flash memory devices requires high resolution technology and a sufficient depth of focus (DOF), particularly in the formation of contact holes. DOF is the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate. As flash memory devices are reduced in size, each stacked gate layer **14**, **16** of the stacked gate pattern **10** is formed closer to adjacent stacked gate layers, thus requiring a smaller V_{SS} contact **12**. As the V_{SS} contact **12** is reduced in size, DOF margin becomes an issue in patterning the V_{SS} contact. In present integrated circuit fabrication, DOF is becoming so small that it is a concern as to whether optical wafer steppers are capable of maintaining the image in focus. This problem is evident in forming components having small feature size, such as contact holes.

Another concern in integrated circuit manufacture is the lateral positioning between layers comprising the integrated circuit, which is known as overlay. As feature sizes shrink, the overlay tolerances must become smaller in order to minimize the creation of defective devices. The reduction in size of the flash memory device requires the V_{SS} contact **12** and adjacent stacked gate layers **14**, **16** to be in closer proximity to one another, thus creating overlay margin issues.

As a result, there exists a need in the art for a method of patterning a V_{SS} contact in a flash memory device that improves the DOF margin and the overlay margin within the stacked gate layer.

SUMMARY OF THE INVENTION

According to one aspect of the invention, the invention is directed to a method of processing an integrated circuit wafer to form a contact in a flash memory device. The method can include forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; depositing an interlayer insulating layer over the plurality of stacked gate layers; patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elongated shape; and depositing a conductive layer in the contact hole.

Another aspect of the invention relates to flash memory device, including a plurality of stacked gate layers, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; and a contact formed between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate

layer of the plurality of stacked gate layers, wherein the contact is formed in an elongated shape.

Other aspects, features, and advantages of the invention will become apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating several embodiments of the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the present invention.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a schematic top view of a prior art V_{SS} contact formed between stacked gate layers of a flash memory device.

FIG. **2** is a schematic top view of a V_{SS} contact formed between stacked gate layers of a flash memory device in accordance with an embodiment of the present invention.

FIG. **3** is a flow diagram illustrating an exemplary embodiment of a method of processing a wafer in accordance with the present invention.

FIG. **4**A is a sectional view of a semiconductor wafer at a certain point during processing of the wafer using the method in accordance with an embodiment of the present invention.

FIG. **4**B is a top view of the semiconductor wafer of FIG. **4**A during another point of the wafer processing.

FIG. **4**C is a cross-section taken along the line **1**—**1** of FIG. **4**B.

FIG. **4**D is a sectional view of the semiconductor wafer during another point of the wafer processing.

FIG. **4**E is a top view of the semiconductor wafer of FIG. **4**A during yet another point of the wafer processing.

FIG. **4**F is a cross-section taken along the line **2**—**2** of FIG. **4**E.

FIG. **4**G is a sectional view of the semiconductor wafer during yet another point of the wafer processing.

FIG. **4**H is a sectional view of the semiconductor wafer during yet another point of the wafer processing.

FIG. **5** is a schematic top view of a V_{SS} contact formed between stacked gate layers of a flash memory device in accordance with another embodiment of the present invention.

DISCLOSURE OF INVENTION

In the detailed description that follows, corresponding components have been given the same reference numerals, regardless of whether they are shown in different embodiments of the present invention or at difference times during a wafer processing method. To illustrate the present invention in a clear and concise manner, the drawings may not necessarily be to scale.

Referring to FIG. **2**, a stacked gate pattern **50** of a flash memory device in accordance with an embodiment of the invention is illustrated. The stacked gate pattern **50** includes a plurality of stacked gate layers **54**, **56**. As can bee seen in FIG. **2**, the stacked gates layers **54**, **56** of the stacked gate pattern **50** form a series of rows, and the rows are substantially parallel to each other.

To assist in describing the invention, the stacked gates layers **54**, **56** can be described with respect to a 3-dimensional Cartesian coordinate system. With respect to FIG. **2**, for example, the z-axis is represented as the horizontal component (e.g., left to right), the y-axis is represented as the vertical component (e.g., bottom to top), and the x-axis is represented as the depth component (e.g., coming out of the page). Thus, the "rows" of stacked gate layers lie in the z-axis, e.g., they form a line that extends along the z-axis, while the width and height components of each stacked gate layer lie in the y-axis and the x-axis respectively.

A V_{SS} contact **52** is formed between the first stacked gate layer **54** and the second stacked gate layer **56**. The V_{SS} contact is formed in an elongated shape having a major axis and a minor axis, such as an ellipse, for example, wherein a major axis **58** of the elongated shape (e.g., the axis that passes through the foci of the ellipse) is substantially parallel to the stacked gate layers **54**, **56**, and the minor axis **60** of the elongated shape (e.g. the axis of the ellipse perpendicular to the major axis at the midpoint between the foci) is substantially perpendicular to the stacked gate layers **54**, **56**.

Since the major axis **58** of the ellipse is substantially parallel to the rows of stacked gate layers **54**, **56** and the rows of stacked gate layers lie in the z-axis, it follows that the major axis **58** of the ellipse also lies in the z-axis. In light of the above and with reference to FIG. **2**, it follows that the minor axis **60** of the ellipse lies in the y-axis. As will be explained in more detail below, the elongated shape provides a contact pattern that minimizes DOF and overlay issues during the fabrication of a flash memory device.

Eccentricity is a numerical value that determines the shape of an ellipse and is defined as the ratio of the distance between the foci to the length of the major axis. Eccentricity is always less than 1, and is expressed by the equation

$$\frac{\sqrt{(a^2-b^2)}}{a} \qquad \text{Eq. 1}$$

where "a" is one half the length of the ellipse's major axis, and "b" is one half the length of the ellipse's minor axis. A perfectly circular ellipse has an eccentricity of 0, while an extremely long and narrow ellipse has an eccentricity that approaches 1. Thus, an elliptical contact having an eccentricity greater than zero, by definition, is not a perfect circle. Such an elliptical contact has a long or wide portion (the major axis) and a narrow or thin portion (the minor axis).

As packing densities of flash memory devices increase, the separation **62** between stacked gate layers is reduced. By forming an elliptical V_{SS} contact between stacked gate layers with its minor axis **60** substantially perpendicular to the stacked gate layers **54**, **56**, the length "b" of the minor axis **60** is constrained by one half of the separation **62** between stacked gate layers, plus any required overlay margin. This same constraint is imposed on prior art circular V_{SS} contacts, wherein a radius "r" of the circular contact must fit within the same limitations.

Thus, as the distance of separation **62** between stacked gate layers **54**, **56** is reduced, the radius "r" of the circular V_{SS} contact and the minor axis "b" of the elliptical V_{SS} contact also must be reduced. A reduction in the radius of the circular V_{SS} contact has the effect of reducing the size of the circular V_{SS} contact in all directions since, by definition, a circle is composed of all points having a distance "r" from a center point. As the radius is reduced, the entire circle is reduced.

The elliptical V_{SS} contact **52**, on the other hand, only is reduced along the minor axis **60**. The major axis **58** is not affected by the reduction in separation between stacked gate layers **54**, **56**. Therefore, the elliptical V_{SS} contact **52** formed between stacked gate layers **54**, **56** can occupy a larger area than a circular V_{SS} contact formed between the same stacked

gate layers. Moreover, the elliptical V_{SS} contact can be dimensioned along its major axis **58** so as to maintain feature size above a threshold value, and thus minimize DOF issues. For example, the length of the major axis **58** can be increased as the length of the minor axis **60** is decreased, thereby maintaining the contact area above a threshold value.

Furthermore, since the elliptical V_{SS} contact **52** can overcome DOF issues by maintaining feature size above a threshold value (e.g., by increasing the major axis **58**), the minor axis **60** can be reduced to a greater extent than can the radius "r" of a circular contact. This provides an increase in overlay margin between the V_{SS} contact **52** and the stacked gate layers **54, 56** when compared to a circular V_{SS} contact. In one embodiment, the ratio of the minor axis length "b" relative to the major axis length "a" (e.g., a/b) is about 1.1 to 1.4, or in other words, the length of the minor axis is about 71 percent to about 90 percent of the length of the major axis.

Referring to the flowchart **200** of FIG. **3** in conjunction with the diagrams of FIGS. **4**A–FIG. **4**H, exemplary processing steps for fabricating the V_{SS} contact **52** between stacked gate layers **54, 56** of a flash memory device are shown.

The process begins with a layer of semiconductor material **100** as shown in step **202**. In step **204**, a gate oxide layer **102** is deposited or grown on a semiconductor substrate **100**. Deposition or growth may be performed through various well known processes, such as chemical vapor deposition (CVD) or dry oxidation in an oxygen and nitrogen ambient atmosphere, for example. Following the formation of the gate oxide layer **102**, a floating gate layer **104** is deposited over the gate oxide layer in step **206**, and in step **208** an inter-gate dielectric layer **106** is deposited over the floating gate layer **104**. The inter-gate dielectric layer **106** typically is an oxide-nitride-oxide (ONO) composition and is formed using conventional techniques. For example, the ONO layer can be formed in a three-stage process, which includes forming a first film of silicon dioxide, depositing a film of silicon nitride on the silicon dioxide, and then depositing a second film of silicon dioxide on the silicon nitride film.

At step **210**, a control gate layer **108** is formed over the inter-gate dielectric layer **106**. Formation of the control gate layer **108** includes, for example, depositing a layer of polysilicon material on the surface of the inter-gate dielectric layer **106** using low pressure chemical vapor deposition as is known by those skilled in the art. Using conventional photolithographic processes, the stacked gate layer is patterned at step **212** to form a stacked gate pattern, e.g., stacked gate layers **54, 56**, as shown in FIG. **4**B and FIG. **4**C.

Next at step **214**, impurities are implanted into the substrate **100** using the stacked gate pattern as an implanting mask to form source **110** and drain **112** regions outside the stacked gate pattern, as is conventional. At step **216**, an interlayer insulating layer **114** is deposited on the resulting structure, as shown in FIG. **4**D. The interlayer insulating layer **114**, for example, can be formed by depositing a silicon oxide film on the stacked gate pattern by means of sputtering or CVD and subsequently polishing the silicon oxide film by chemical mechanical polish (CMP). Alternatively, the interlayer insulating layer **114** may be a multilayer film such as a silicon nitride film, an SOG (spin on glass) film or a BPSG (boron phosphor silicate lass) film.

Moving to step **218**, a V_{SS} contact hole **116** is patterned in the interlayer insulating layer **114** between stacked gate layers **54, 56** using conventional photolithographic techniques, as shown in FIG. **4**E and FIG. **4**F. As disclosed previously, the V_{SS} contact hole **116** is patterned in an elliptical shape, wherein the minor axis **60** of the ellipse is substantially perpendicular to the stacked gate layers **54, 56** and the major axis **58** of the ellipse is substantially parallel to the stacked gate layers **54, 56**.

At step **220**, the contact hole **116** is filled with a suitable conductive material (e.g., a metal, a metal containing compound or a semiconductor). For example, a conductive layer **118** such as a doped polysilicon layer or a metal polycide layer is deposited in the contact hole **116** and on the interlayer insulating layer **114** as shown in FIG. **4**G. Moving to step **222**, a planarization process such as an etch-back or a chemical mechanical polish is carried out to leave the conductive layer in the contact hole and remove the portion of the conductive layer that is outside of the contact hole, thereby forming the V_{SS} contact **52** as shown in FIG. **4**H.

As one skilled in the art will appreciate, the exemplary method described herein can be modified. For example, certain steps can be omitted, certain steps can be carried out concurrently, and other steps can be added.

Referring now to FIG. **5**, a stacked gate pattern **50'** of a flash memory device in accordance with another embodiment of the invention is illustrated. The stacked gate pattern **50'** includes a plurality of stacked gate layers **54, 56**. A V_{SS} contact **52'** is formed between the first stacked gate layer **54** and the second stacked gate layer **56**. The V_{SS} contact is formed as an elongated shape having a major axis and a minor axis (e.g., in the shape of a rectangle, wherein a first pair of sides **300** are longer than a second pair of sides **302**). The first pair of sides **300** lie in the z-axis and are substantially parallel to the stacked gate layers **54, 56**. The second pair of sides **302** lie in the y-axis and are substantially perpendicular to the stacked gate layers **54, 58**. With respect to the rectangular V_{SS} contact **52'**, a major axis **58'** is defined as an axis parallel to the first pair of sides **300** and intersecting a midpoint of the second pair of sides **302**, and a minor axis **60'** is defined as an axis parallel to the second pair of sides **302** and intersecting a midpoint of the first pair of sides **300**.

As was described previously with respect to the elliptical V_{SS} contact **52**, the rectangular V_{SS} contact **52'** formed between stacked gate layers **54, 56** can occupy a larger area than a circular V_{SS} contact formed between the same stacked gate layers. Additionally, the rectangular V_{SS} contact **52'** can be dimensioned along the z-axis so as to maintain feature size above a threshold value, and thus minimize DOF issues. For example, the length of the first pair of sides **300** can be increased as the length of the second pair of sides **302** are decreased, thereby maintaining the contact area above a threshold value.

Furthermore, since the first pair of sides **300** of the rectangular V_{SS} contact **52'** can be increased to maintain feature size above a threshold value, the length of the second pair of sides **302** can be reduced to a greater extent than can the radius "r" of a circular contact. This provides an increase in overlay margin between the V_{SS} contact **52'** and the stacked gate layers **54, 56** when compared to a circular V_{SS} contact. In one embodiment, the ratio of the second pair of sides **302** relative to the first pair of sides **300** (first pair/second pair) is about 1.1 to 1.4, or in other words, the length of the second pair of sides **302** are about 71 percent to about 90 percent of the length of the first pair of sides **300**.

Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto. For example,

while the exemplary embodiment has been illustrated using a floating gate memory cell, it will be appreciated by those skilled in the art that the invention also may be applied to a flash memory device employing a silicon-oxide-nitride-oxide-silicon (SONOS) memory cell.

What is claimed is:

1. A method of forming a contact in a flash memory device that improves the depth of focus (DOF) margin and the overlay margin between a plurality of stacked gate layers and the respective contact, comprising the steps of:

forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers;

depositing an interlayer insulating layer over the plurality of stacked gate layers;

patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elongated shape having a major axis and a minor axis, and the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit; and

depositing a conductive layer in the contact hole.

2. The method of claim **1**, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes aligning the major axis of the contact hole substantially parallel to the predefined direction of the stacked gate layers.

3. The method of claim **1**, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes aligning the minor axis of the contact hole substantially perpendicular to the predefined direction of the stacked gate layers.

4. The method of claim **1**, further comprising the step of:

removing a portion of the conductive layer that is outside the contact hole to leave the conductive layer in the contact hole.

5. The method of claim **1**, wherein the step of patterning a contact hole between a first stacked gate layer and a second stacked gate layer includes forming the minor axis of the contact hole to be about 71 percent to about 90 percent of a major axis of the contact hole.

6. The method of claim **1**, wherein the step of patterning a contact hole in an elongated shape includes patterning the contact hole in the shape of an ellipse.

7. The method of claim **1**, wherein the step of patterning a contact hole in an elongated shape includes patterning the contact hole in the shape of a rectangle.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

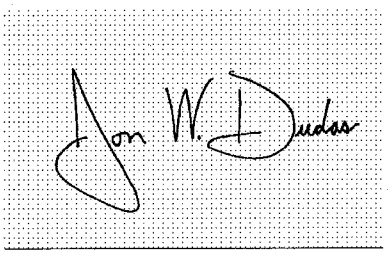
PATENT NO. : 7,018,922 B1
APPLICATION NO. : 10/968713
DATED : March 28, 2006
INVENTOR(S) : Kim et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page item
54 (Title), replace "CONTACT FLASH" with --CONTACT ON FLASH--.
Col. 6, Ln. 33, replace "layers 54, 58. With" with --layers 54, 56. With--.

Signed and Sealed this

Fourth Day of July, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

US007151027B1

(12) **United States Patent**
Ogawa et al.

(10) **Patent No.: US 7,151,027 B1**
(45) **Date of Patent: Dec. 19, 2006**

(54) **METHOD AND DEVICE FOR REDUCING INTERFACE AREA OF A MEMORY DEVICE**

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(73) Assignee: **Spansion LLC**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 29 days.

(21) Appl. No.: **10/859,369**

(22) Filed: **Jun. 1, 2004**

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/257**; 438/238; 438/381; 257/E21; 257/613; 257/694; 257/645

(58) **Field of Classification Search** 438/257, 438/258, 238, 381, 647, 657, 734, 735, 954
See application file for complete search history.

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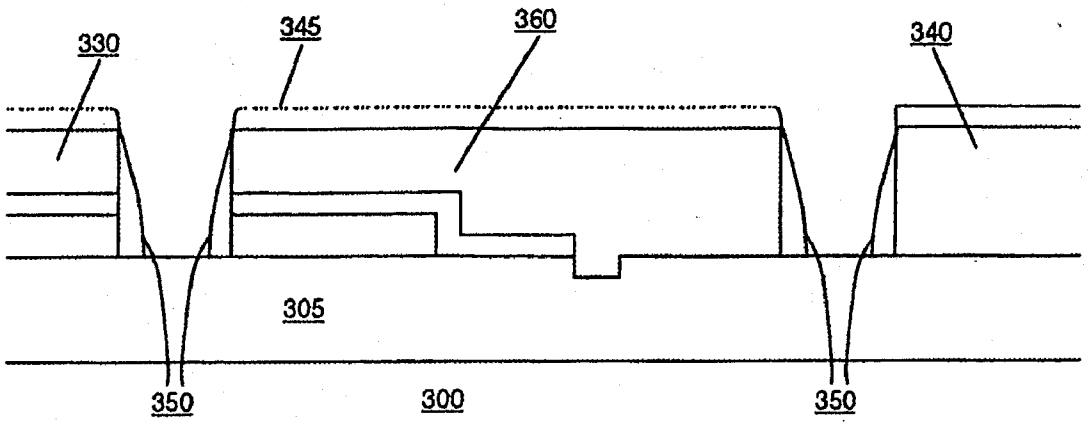
Primary Examiner—David Nhu

(57) **ABSTRACT**

A method and device for reducing interface area of a memory device. A poly-2 layer is formed above a substrate at an interface between a memory array and a periphery of the memory device. The poly-2 layer is etched proximate to the memory array. The poly-2 layer is etched proximate to the periphery such that a portion of the poly-2 layer remains at the interface.

14 Claims, 6 Drawing Sheets



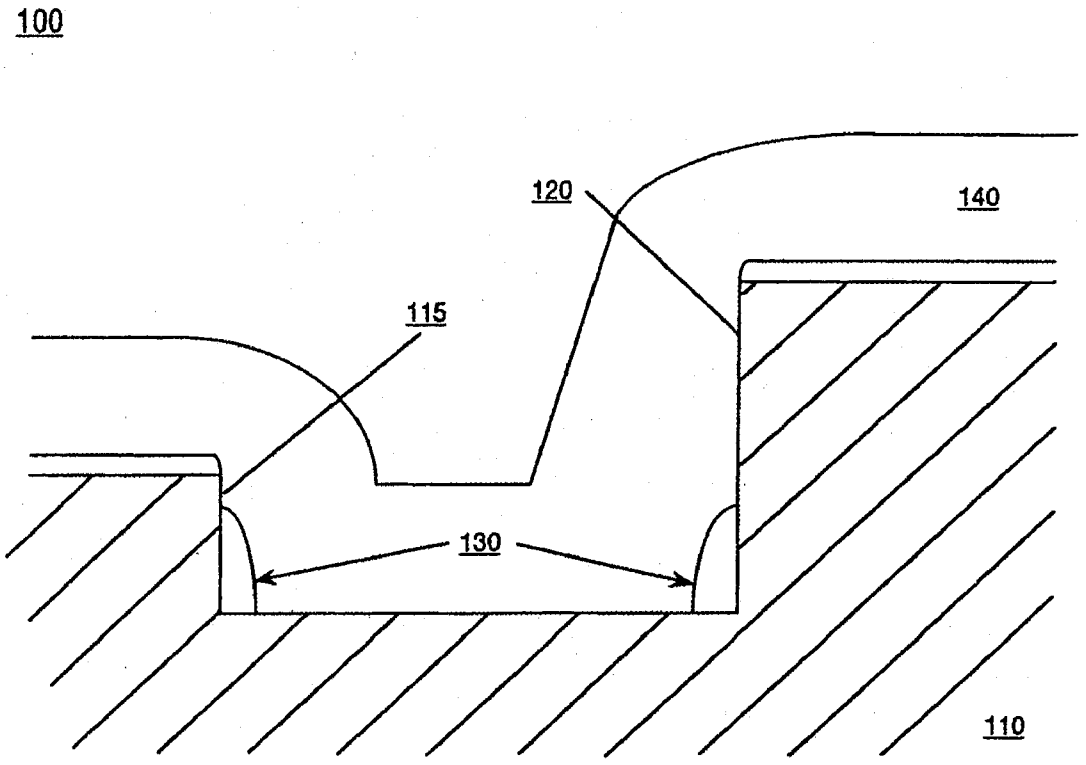


Figure 1
(Prior Art)

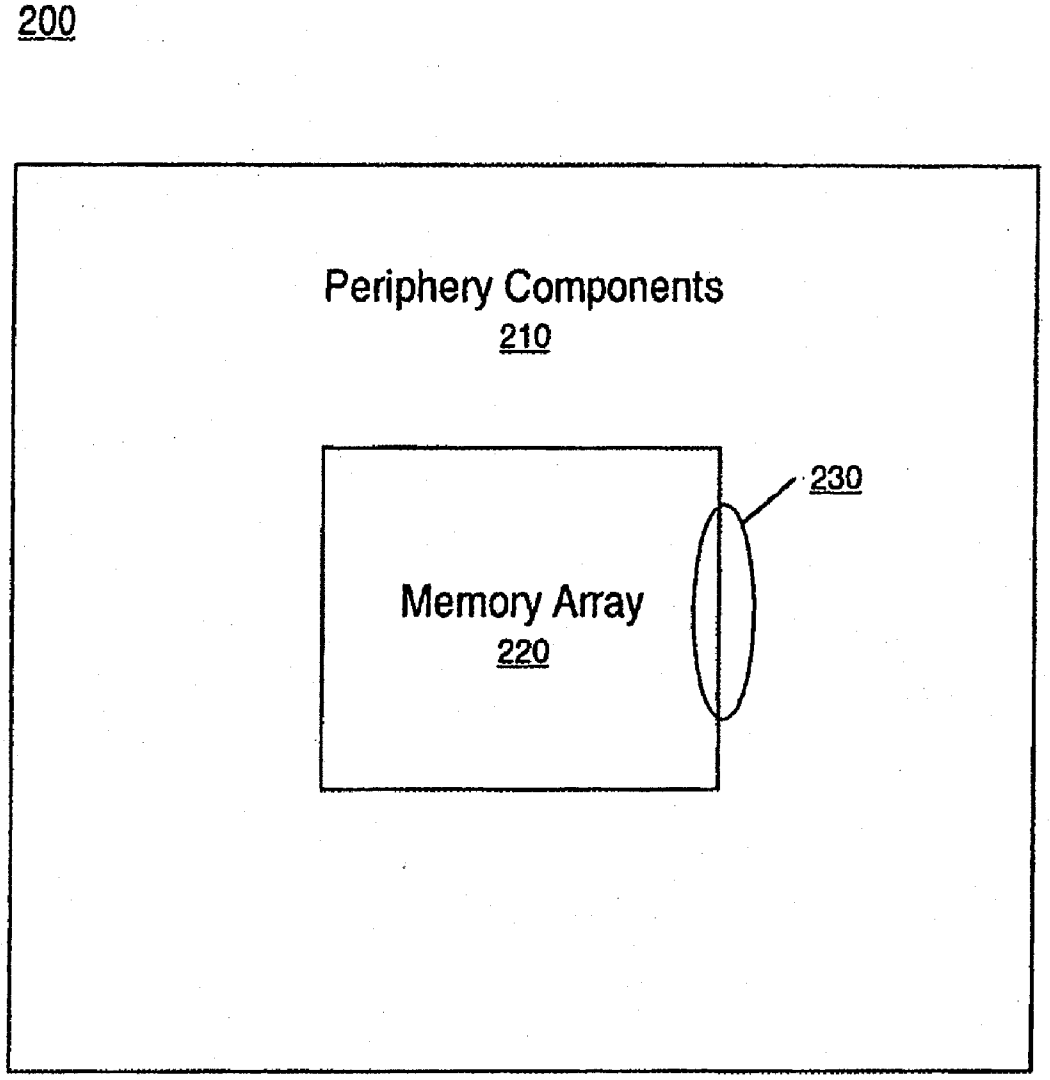


Figure 2

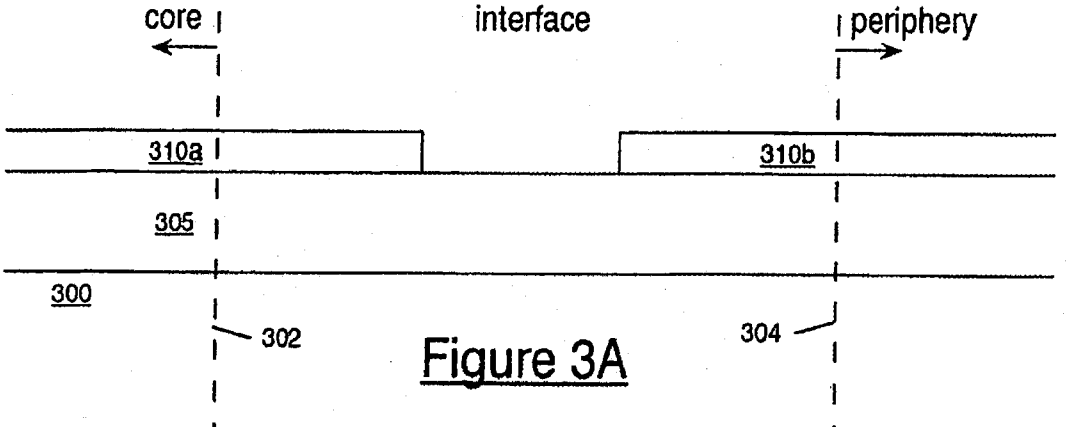


Figure 3A

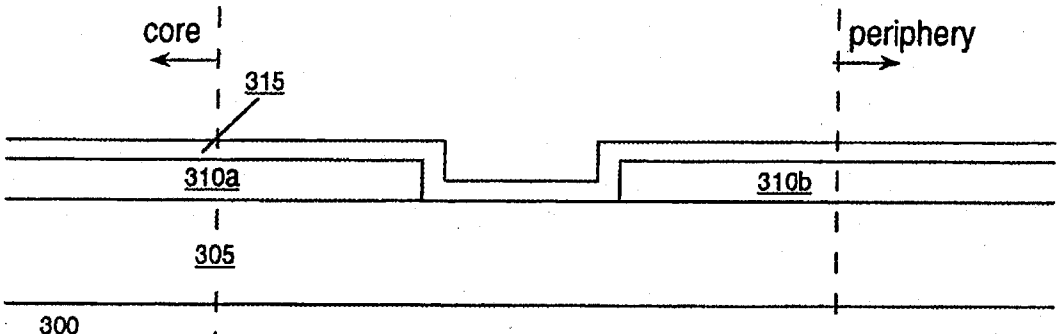


Figure 3B

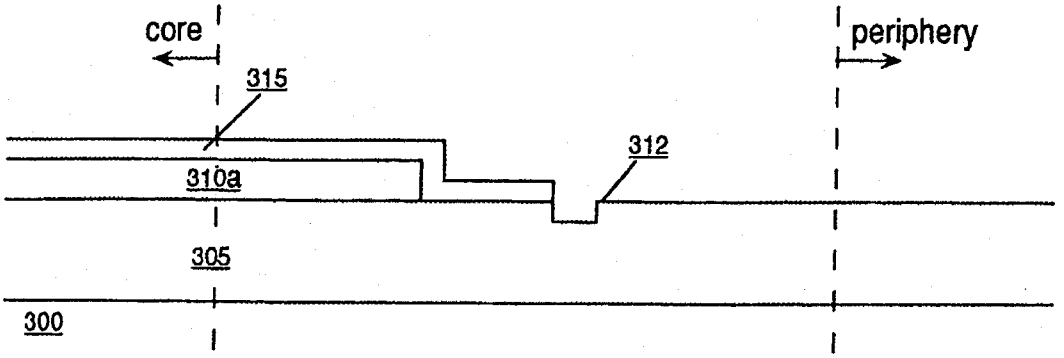


Figure 3C

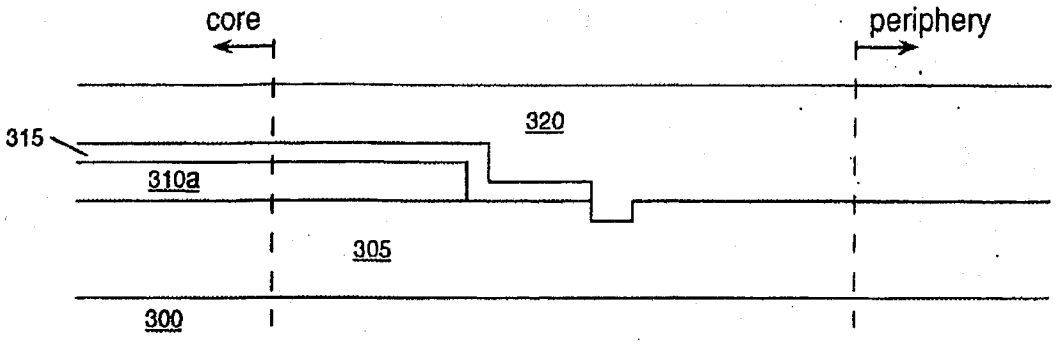


Figure 3D

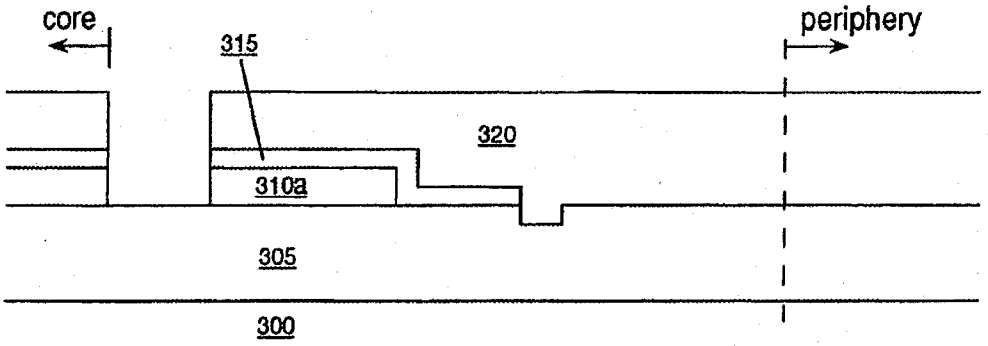


Figure 3E

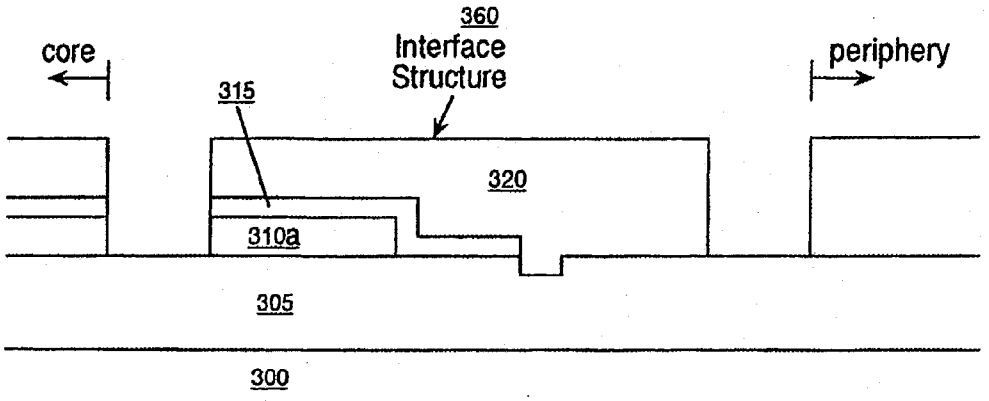


Figure 3F

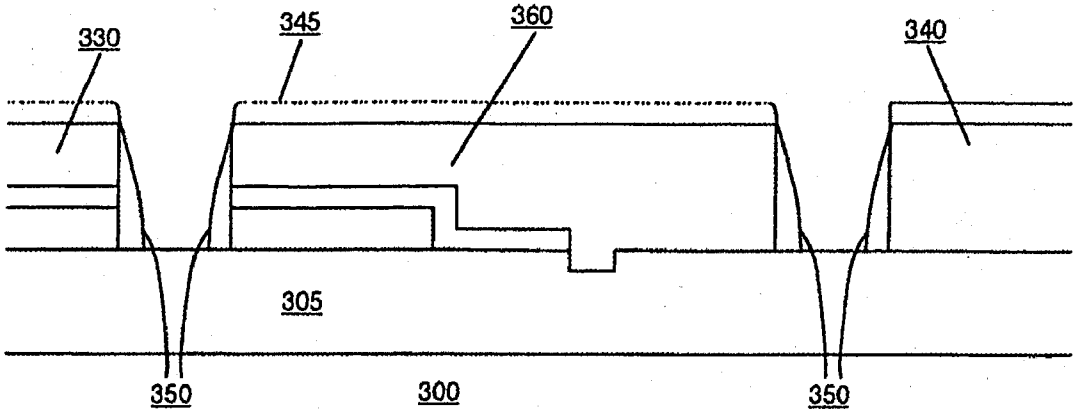


Figure 3G

400

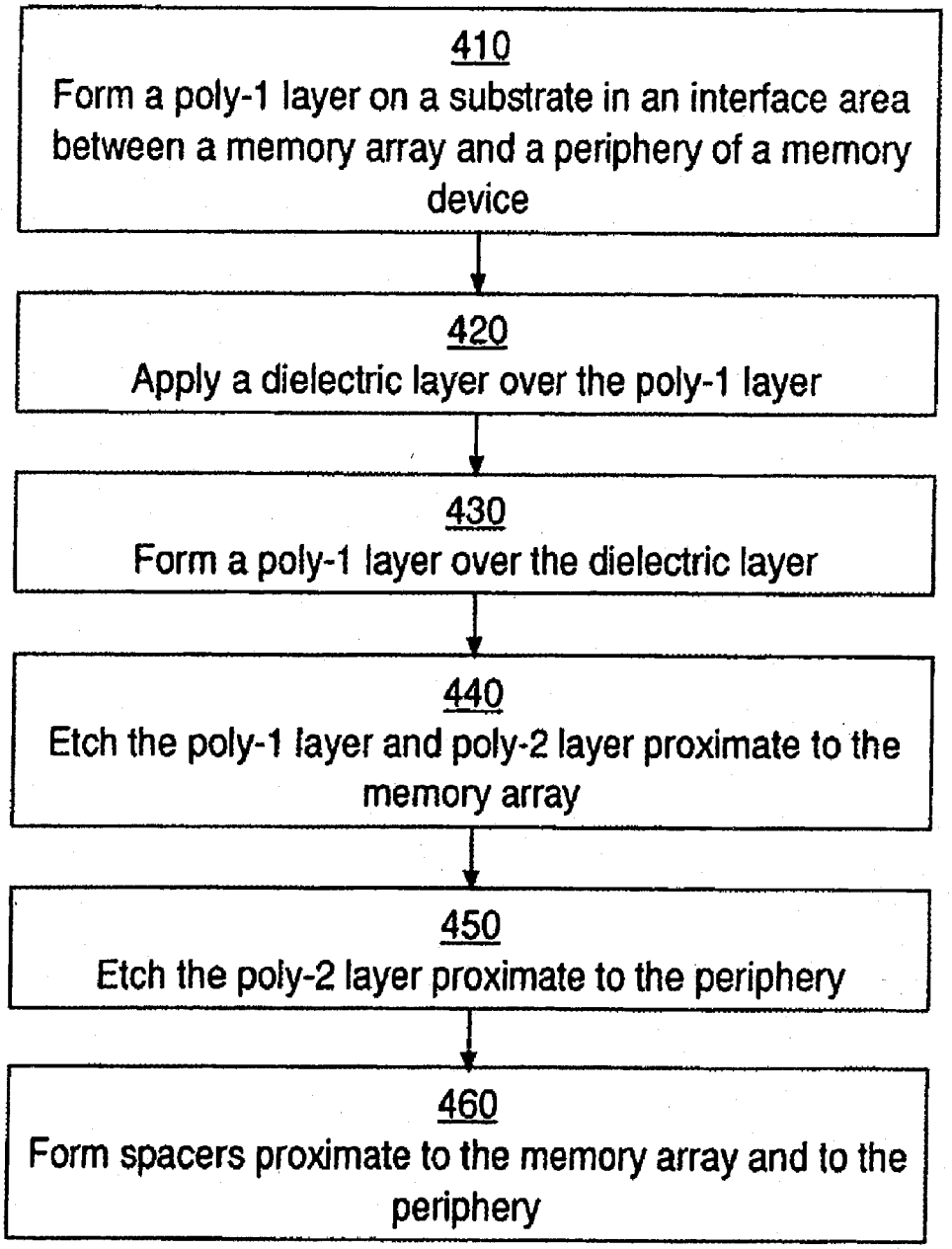

410
Form a poly-1 layer on a substrate in an interface area between a memory array and a periphery of a memory device
420
Apply a dielectric layer over the poly-1 layer
430
Form a poly-1 layer over the dielectric layer
440
Etch the poly-1 layer and poly-2 layer proximate to the memory array
450
Etch the poly-2 layer proximate to the periphery
460
Form spacers proximate to the memory array and to the periphery

Figure 4

METHOD AND DEVICE FOR REDUCING INTERFACE AREA OF A MEMORY DEVICE

TECHNICAL FIELD

The present invention relates to the field of floating gate devices. Specifically, the present invention relates to reducing the interface area between a memory array and a periphery of a memory device.

BACKGROUND ART

A modem integrated circuit (IC), for example a flash memory device, may have millions to hundreds of millions of devices made up of complex, multi-layered structures that are fabricated through hundreds of processing steps. Those structures are formed by repeated deposition and patterning of thin films on a silicon substrate, also known as a wafer.

One important goal of the semiconductor industry is to reduce the size of memory devices. In reducing the size of operational components (e.g., a memory array) and periphery components, an important consideration is the interface between the operational components and periphery components. Current fabrication processes for forming memory devices typically form the operational components and the periphery components using separate processes. For example, when the periphery components are formed only the periphery is etched, and when the memory array is formed, only the memory array is etched. By forming the periphery components and the memory array using different processes, a number of steps in the interface area are created. A step exists where two adjacent structures have a different height, as shown in FIG. **1**.

FIG. **1** is a diagram of a side view of a portion of an interface area of an exemplary memory device **100**, in accordance with the prior art. By using different processes to form the memory array and the periphery components, respectively, steps are created. Substrate **110** has been etched wherein two structures **115** and **120** remain. As can be seen, structure **120** is higher than structure **115**. In particular, the height of the step is hard to control because the different heights are created using different processes.

Sidewall spacers are commonly formed after the individual transistors of the memory array have been formed. When the sidewall spacers are formed, stringer spacers (e.g., stringer spacers **130** of FIG. **1**) are formed in the interface area at the steps. A stringer spacer is a small component that is easily peeled or removed from the memory device. If removed, the debris may be displaced to the memory array or periphery componentry. This debris may result in a yield loss of performance by the memory array. Furthermore, because it is difficult to control the height of the steps, it is also hard to control the height of the stringer spacers.

In order to eliminate the risks caused by stringer spacer debris, current memory devices include a salicide block fabricated over the interface area (e.g., salicide layer **140** of FIG. **1**). After transistor formation, a salicide block is formed over the interface, requiring an additional mask, adding costs to the fabrication process. Moreover, the salicide block requires additional area of the interface. In particular, the area required by the salicide block considerably limits the ability to reduce the size of the interface area.

DISCLOSURE OF INVENTION

Various embodiments of the present invention, a method and device for reducing interface area of a memory device,

are described. In one embodiment, a memory device is fabricated, in which a poly-2 layer is formed above a substrate at an interface between a memory array and a periphery of the memory device. The poly-2 layer is etched proximate to the memory array. The poly-2 layer is etched proximate to the periphery such that a portion of the poly-2 layer remains at the interface. In one embodiment, the portion of the poly-2 layer remaining at the interface is the same height as the memory array proximate to the memory array and the same height as the periphery proximate to the periphery, such that step size is smoothed out reducing the occurrence of stringers from spacer etching.

BRIEF DESCRIPTION OF DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. **1** is a diagram of a side view of a portion of an interface area of an exemplary memory device, in accordance with the prior art.

FIG. **2** is a block diagram of a memory device in accordance with an embodiment of the present invention.

FIGS. **3**A through **3**G are diagrams of the side view of an exemplary interface area of a memory device illustrating steps in a process for forming an interface structure, in accordance with an embodiment of the present invention.

FIG. **4** is a flowchart illustrating steps in a process for fabricating a memory device, in accordance with an embodiment of the present invention.

The drawings referred to in this description should be understood as not being drawn to scale except if specifically noted.

MODE(S) FOR CARRYING OUT THE INVENTION

Reference will now be made in detail to embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the described embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

The present invention provides a method and structure for reducing interface area between the memory array and the periphery of a memory device. In one embodiment, the boundaries of the various masks used to form a polysilicon layer are adjusted such that a polysilicon interface structure remains in the interface. The polysilicon interface structure is operable to smooth out any steps caused by the etching. In particular, the height of the polysilicon interface structure is easy to control, eliminating the creation of stringer spacers. Furthermore, embodiments of the present invention do not require a salicide layer, thereby reducing the number of

masks needed to fabricate the memory device and to allow for a reduction in interface area.

FIG. **2** is a block diagram of a memory device in accordance with an embodiment of the present invention. Memory device **200** includes a periphery components portion **210** and a memory array portion **220**. In one embodiment, memory device **200** is a flash memory device. Although only one memory array **220** is shown in memory device **200**, it is completely viable for there to be more than one memory array **220** being formed on memory device **200**. In one embodiment, memory array **220** is manufactured in a flash memory process that is well known in the art. Included in the manufacture of memory array **220** may be source-drain portions, poly one and poly-2 layers, tunnel oxide, silicon, field oxide, and the like. In addition, interface area **230** of FIG. **2**, which is better illustrated in FIGS. **3**A through **3**G, includes poly-1 and poly-2 layers.

FIGS. **3**A through **3**G are diagrams of the side view of an exemplary interface area of a memory device illustrating steps in a process for forming an interface structure **360** (FIG. **3**G), in accordance with an embodiment of the present invention. Specifically, FIGS. **3**A, **3**B, **3**C, **3**D, **3**E, **3**F and **3**G illustrate a process for fabricating an interface structure **360** according to one embodiment of the present invention. In one embodiment, interface structure **360** includes polysilicon. In one such embodiment, interface structure **360** includes a poly-1 layer and a poly-2 layer.

It is understood that FIGS. **3**A through **3**G are not drawn to scale and that only portions of the substrate **300** and other layers are shown. For simplicity of discussion and illustration, the process is described for a single interface structure **360**, although in actuality multiple interface structures may be formed.

Furthermore, although the device being formed is referred to as a an interface structure, it is appreciated that FIGS. **3**A through **3**G only show an interface structure in the process of being formed, and not necessarily a completely formed interface structure. It is appreciated that other processes and steps associated with the fabrication of an interface structure may be performed along with the process illustrated by FIGS. **3**A through **3**G; that is, there may be a number of process steps before and after the steps shown and described by FIGS. **3**A through **3**G. Importantly, embodiments of the present invention can be implemented in conjunction with these other (conventional) processes and steps without significantly perturbing them. Generally speaking, the various embodiments of the present invention can replace a conventional process without significantly affecting the peripheral processes and steps.

Referring first to FIG. **3**A, in the present embodiment, substrate **300**, isolation area **305** (e.g., a shallow trenched area), and gate polysilicon ("poly-1") **310***a* and **310***b* are shown in cross section. In one embodiment, isolation area **305** is filled with SiO_2. Line **302** indicates the approximate border between the memory array (e.g., care) and the interface area. Similarly, line **304** indicates the approximate border between the interface area and the periphery. The portion of substrate **300** of the memory array is typically doped with n-type and p-type materials to form a number of regions in the memory array. For example, in an n-channel transistor—in particular, in a high voltage n-channel transistor—the substrate **300** may include silicon doped with a p-type material, a deep n-well, a high voltage p-well, and high voltage n-wells. It should be appreciated that the portion of poly-1 **310***b* that resides in the interface and periphery regions may not be needed to form active transistors, and is therefore optional.

Referring now to FIG. **3**B, in the present embodiment, a film of dielectric material **315** is applied over substrate **300** and poly-1 **310***a* and **310***b*, essentially coating the exposed (upper) surfaces of substrate **300** and poly-1 **310***a* and **310***b*. Different dielectric materials may be used; in one embodiment, the dielectric material includes SiO_2, and in another embodiment the dielectric material includes Si_3N_4. In one embodiment a oxide-nitride-oxide (ONO) dielectric layer is applied.

Referring next to FIG. **3**C, in the present embodiment, a known process (such as an etch back process) is used to remove selectively the dielectric material **315** and poly-1 **310***b*. Significantly, a portion of the dielectric material **315** overlying poly-1 **310***b* and a portion of substrate **300** is deposited and then selectively removed. In one embodiment, the deposition and removal is necessary for the fabrication of transistors of the memory array. In one embodiment, notch **312** is etched into isolation area **305**. It should be appreciated that notch **312** is a small trench that is etched as a result of the process used to remove dielectric material **315** and poly-1 **310***b*.

With reference to FIG. **3**D, in the present embodiment, a second polysilicon layer (poly-2) **320** is deposited above dielectric material **315** and substrate **300**. In one embodiment, poly-2 layer **320** is used to form a word line for use in the active transistor of the memory array.

With reference next to FIG. **3**E, in the present embodiment, a known process (such as a stacked gate etch) is used to etch a portion of poly-1 **310***a*, dielectric material **315**, and poly-2 **320** proximate to the memory array. The etch is used to form individual transistors of from the polysilicon layers. In one embodiment, the stacked gate edge uses a stacked gate mask above the interface region and the periphery. The etch creates a distinct boundary between the memory array and the interface region. By locating the stacked gate mask close to the core region, poly-1 **310***a* and poly-2 **320** remain in the interface region.

With reference next to FIG. **3**F, in the present embodiment, a known process (such as a second gate etch) is used to etch a portion of poly-2 **320** proximate to the periphery. The etch is used to form interface structure **360**. In one embodiment, the second gate edge uses a second gate mask above the interface region and the memory array. The second gate etch creates a distinct boundary between the memory array and the interface region. By locating the second gate etch close to the periphery region, only part of the poly-2 **320** in the interface region is etched, keeping interface structure **360**, including poly-1 **310***a* and poly-2 **320**, in the interface region. In one embodiment, interface structure **360** is the same height as the memory array proximate to the memory array and the same height as the periphery proximate to the periphery, such that step size is smoothed out reducing the occurrence of stringers from spacer etching.

Referring now to FIG. **3**G, the memory device now includes interface structure **360** as well as transistor **330** and periphery poly-2 **340**. It should be appreciated that transistor **330** is the last active transistor of the memory array next to the interface area. A film of dielectric material **345** is applied over substrate **300**, interface structure **360**, transistor **330** and periphery poly-2 **340**, essentially coating the exposed (upper) surfaces of substrate interface structure **360**, transistor **330** and periphery poly-2 **340**. Different dielectric materials may be used; in one embodiment, the dielectric material includes SiO_2, and in another embodiment the dielectric material includes Si_3N_4. A known process (such as an etch back process) is used to remove selectively the

dielectric material to form a first set of spacers **350** along the side walls of interface structure **360**, transistor **330** and periphery poly-2 **340**. In one embodiment, a second set of spacers are formed adjacent to the first spacers **350**.

FIG. **4** is a flowchart illustrating steps in a process **400** for fabricating a memory device, in accordance with an embodiment of the present invention. Although specific steps are disclosed in process **400**, such steps are exemplary. That is, the present invention is well suited to performing various other steps or variations of the steps recited in process **400**.

At step **410**, a first polysilicon layer (e.g., poly-1) is formed on a substrate in an interface area between a memory array and a periphery of the memory device. In one embodiment, a gate oxide is grown on the substrate. At step **420**, in one embodiment, a dielectric layer is applied over the first polysilicon layer. In one embodiment, the dielectric layer is an ONO layer. At step **430**, a second polysilicon layer (e.g., poly-2) is formed over the dielectric layer. In one embodiment, a gate or gate poly is formed over the gate oxide).

At step **440**, the poly-1 layer and the poly-2 layer are etched proximate to the memory array. In one embodiment, the etching is accomplished by performing a stacked gate etch. At step **450**, the poly-2 layer is etched proximate to the periphery, such that an interface structure including a portion of the poly-1 layer and a portion of the poly-2 layer remains at the interface. In one embodiment, the etching is accomplished by performing a second gate etch.

Thus, according to the various embodiments of the present invention, the interface structure is the same height as the memory array proximate to the memory array and the same height as the periphery proximate to the periphery, such that step size is smoothed out reducing the occurrence of stringers from spacer etching. At step **460**, spacers are formed proximate to the memory array and proximate to the periphery. In one embodiment, the spacers are nitride spacers.

To summarize, the described embodiments provide a method and structure for reducing interface area between the memory array and the periphery of a memory device. In one embodiment, the boundaries of the various masks used to form a polysilicon layer are adjusted such that a polysilicon interface structure remains in the interface. The polysilicon interface structure is operable to smooth out any steps caused by the etching. In particular, the height of the polysilicon interface structure is easy to control, eliminating the creation of stringer spacers. Furthermore, embodiments of the present invention do not require a salicide layer, thereby reducing the number of masks needed to fabricate the memory device and to allow for a reduction in interface area.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

What is claimed is:

1. A method for fabricating a memory device, said method comprising:

forming a poly-2 layer above a substrate at an interface between a memory array and a periphery of said memory device;

etching said poly-2 layer proximate to said memory array; and

etching said poly-2 layer proximate to said periphery such that a portion of said poly-2 layer remains at said interface.

2. The method as recited in claim **1** further comprising:

forming a poly-1 layer above said substrate at said interface, such that said poly-1 layer is above said substrate and beneath said poly-2 layer;

etching said poly-1 layer proximate to said memory array; and

etching said poly-1 layer proximate to said periphery such that a portion of said poly-1 layer remains at said interface.

3. The method as recited in claim **1** wherein said etching said poly-2 layer proximate to said memory array is accomplished by performing a stacked gate etch.

4. The method as recited in claim **1** wherein said etching said poly-2 layer proximate to said periphery is accomplished by performing a second gate etch.

5. The method as recited in claim **1** further comprising:

forming spacers proximate to said memory array; and

forming spacers proximate to said periphery.

6. The method as recited in claim **2** further comprising forming an ONO layer above said poly-1 layer such that said ONO layer is above said poly-1 layer and beneath said poly-2 layer.

7. The method as recited in claim **1** wherein said portion of said poly-2 layer remaining at said interface is a same height as said memory array proximate to said memory array a same height as said periphery proximate to said periphery, such that step size is smoothed out reducing an occurrence of stringers from spacer etching.

8. A method for fabricating a memory device, said method comprising:

forming a poly-1 layer above a substrate at an interface between a memory array and a periphery of said memory device;

forming a poly-2 layer above said poly-1 layer at said interface;

etching said poly-1 layer and said poly-2 layer proximate to said memory array; and

etching said poly-2 layer proximate to said periphery, such that an interface structure including a portion of said poly-1 layer and a portion of said poly-2 layer remains at said interface.

9. The method as recited in claim **8** wherein said etching said poly-1 layer and said poly-2 layer proximate to said memory array is accomplished by performing a stacked gate etch.

10. The method as recited in claim **8** wherein said etching said poly-2 layer proximate to said periphery is accomplished by performing a second gate etch.

11. The method as recited in claim **8** further comprising:

forming spacers proximate to said memory array; and

forming spacers proximate to said periphery.

12. The method as recited in claim **11** wherein said spacers are nitride spacers.

13. The method as recited in claim 8 further comprising forming an ONO layer above said poly-1 layer such that said ONO layer is above said poly-1 layer and beneath said poly-2 layer.

14. The method as recited in claim 8 wherein said interface structure is a same height as said memory array proximate to said memory array and a same height as said periphery proximate to said periphery, such that step size is smoothed out reducing an occurrence of stringers from spacer etching.

* * * * *