UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN STATIC RANDOM ACCESS MEMORIES AND PRODUCTS CONTAINING THE SAME**	**Inv. No. 337-TA-792**

ORDER 29: CONSTRUING THE TERMS OF THE ASSERTED CLAIMS OF THE PATENTS AT ISSUE

(February 9, 2012)

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I. INTRODUCTION

This Investigation was instituted by the Commission on July 28, 2011 to determine whether certain static random access memories and products containing same infringe U.S. Patent Nos. 6,534,805 (the "'805 patent"); 6,651,134 (the "'134 patent"); 7,142,477 (the "'477 patent"); and 6,262,937 (the "'937 patent").[1] *See* Fed. Reg. 45,295-96 (July 28, 2011). The named respondents are GSI Technology, Inc.; Telefonaktiebolaget LM Ericsson; Ericsson Inc.; Motorola Mobility, Inc.; Motorola Solutions, Inc.; Tellabs, Inc.; Cisco Systems, Inc.; Avnet, Inc.; and Hewlett-Packard Company/Tipping Point (collectively, "Respondents").

Pursuant to Ground Rule 5A, a *Markman* hearing was held on October 14, 2011 regarding the interpretation of certain terms of the asserted claims of the patents at issue, namely:

- Claims 1, 2, and 4–6 of the '805 patent;
- Claims 1, 2 and 12–15 of the '134 patent;
- Claims 8 and 9 of the '477 patent; and
- Claims 1, 2, 6, 12, and 13 of the '937 patent.

Prior to the hearing, Complainant Cypress Semiconductor Corp. ("Cypress") and Respondents met and conferred in an effort to reduce the number of disputed claim terms to a minimum. The parties also filed initial and reply claim construction briefs, wherein each party offered its construction for the claim terms in dispute, along with support for its proposed interpretation. After the hearing and pursuant to Order No. 7, the parties submitted an updated Joint Claim Construction Chart.[2]

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[1] Complainant Cypress Semiconductor Corp. is presently the owner, by assignment, of the patents-in-suit. (2d Am. Compl. at ¶ 1.3; Ex. 4 to 2d Am. Compl.)

[2] The claim terms discussed in detail in this Order were identified in the Updated Joint Proposed Claim Construction Chart as being agreed upon or remaining in dispute. For convenience, the briefs and chart submitted by the parties for the *Markman* hearing are referred to hereafter as follows:

II. IN GENERAL

The claim terms construed in this Order are done so for the purposes of this Section 337 Investigation. Those terms not in dispute need not be construed. *See Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms).

Hereafter, discovery and briefing in this Investigation shall be governed by this construction of the claim terms. **All** other claim terms shall be deemed undisputed and shall be interpreted by the undersigned in accordance with "their ordinary meaning as viewed by one of ordinary skill in the art." *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1371 (Fed. Cir. 2003), *cert. denied*, 540 U.S. 1073 (2003).

III. RELEVANT LAW

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a "matter of law exclusively for the court." *Id.* at 970-71. "The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

CMIB	Cypress's *Markman* Initial Brief
CMRB	Cypress's *Markman* Reply Brief
RMIB	Respondents' *Markman* Initial Brief
RMRB	Respondents' *Markman* Reply Brief
JC	Updated Joint Proposed Claim Construction Chart

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *see also Markman*, 52 F.3d at 979. As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in art at the time of the invention. 415 F.3d at 1313. "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms." *Id.* at 1314; *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [ ] out and distinctly claim [ ] the subject matter which the patentee regards as his invention."). The context in which a term is used in an asserted claim can be "highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.*

The specification "is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." *Id.* at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification

may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be . . . the correct construction." *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Id.* at 1317; *see also Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see also Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* at 1317. "The court may receive extrinsic evidence to educate itself about the invention and the relevant

technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims, however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, "if the only claim construction that is consistent with the claim's language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid." *Id.*

IV. LEVEL OF ORDINARY SKILL IN THE ART

Neither Cypress nor Respondents set forth a position as to the level of ordinary skill in the art in their briefs. Respondents' expert, Dr. Robert Murphy, did, however, address this issue with respect to the '134, '937, and '477 patents in his initial expert report on claim construction, wherein he stated:

> A person of ordinary skill in the relevant art of the '134, '937, and '477 patents at that time would have had a BS in Electrical Engineering and 5 years experience with direct SRAM design experience.

(RX-9 at ¶ 15.)

Accordingly, as to "one of ordinary skill in the art," the undersigned finds that, with respect to the '134, '937, and '477 patents, one of ordinary skill in the art for the would be an engineer with a bachelor's degree or higher in electrical engineering or its equivalent and five or more years of experience in direct SRAM design. The undersigned similarly finds that with respect to the '805 patent, one of ordinary skill in the art would be an engineer with a bachelor's

degree or higher in electrical engineering or its equivalent and five or more years of experience in SRAM design.

V. THE '805 PATENT

A. Overview

The '805 patent is entitled "SRAM Cell Design." The '805 patent issued on March 18, 2003 to named inventor Bo Jin, and was subsequently assigned to Cypress. The '805 patent has 10 claims of which claims 1, 2, and 4–6 are asserted against Respondents. Claim 1 is an independent claim. Claims 2 and 4–6 are dependent claims. The asserted claims read as follows (with the first instance of the agreed-upon terms highlighted in *italics* and the first instance of the disputed term highlighted in **bold**):

1. A memory cell comprising a series of four *substantially oblong active regions* formed within a semiconductor substrate and arranged side-by-side with long axes substantially parallel, wherein each of the inner active regions of the series comprises a pair of source/drain regions for a respective p-channel transistor, and each of the outer active regions of the series comprises a pair of source/drain regions for a respective n-channel transistor.

2. The memory cell as recited in claim 1, further comprising a plurality of *substantially oblong polysilicon structures* arranged above and substantially perpendicular to the active regions.

4. The memory cell as recited in claim 2, further comprising source/drain contacts to the source/drain regions of transistors, wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures.

5. The memory cell as recited in claim 4, further comprising a series of *substantially oblong local interconnects* arranged substantially perpendicular to the active regions, wherein the shared contact is connected to another of the source/drain contacts by one of the **local interconnects**.

6. The memory cell as recited in claim 5, wherein the local interconnects are dielectrically spaced above the semiconductor substrate.

B. Agreed-Upon and Disputed Claim Terms

1. Construction of Agreed-Upon Claim Terms

a) "active regions"

The term "active regions" appears in claim 1 of the '805 patent. The parties have agreed that said term should be interpreted to mean "areas, separated by isolation regions, where active transistors and/or diffusion regions are formed." (JC at 7.)

Accordingly, the undersigned adopts the parties' proposed construction and construes the term "active regions" as "***areas, separated by isolation regions, where active transistors and/or diffusion regions are formed.***"

b) "substantially oblong[3] active regions"

Cypress and Respondents agree that the phrase "substantially oblong active regions," which appears in appears in claim 1 of the '805 patent, should be construed as "an active region: (1) the length of which is substantially constant and the width of which varies by approximately one-third or less along the length of the region; (2) the length of which is substantially constant and the width of which by design varies only with respect to the widths of the access and latch transistors; or (3) the length of which is greater than or equal to approximately three times its maximum width; and (4) which does not include markedly L-shaped regions." (*See* Notice Of Claim Construction With Respect To "Substantially Oblong" As Used In U.S. Patent No. 6,534,805 (Jan. 9, 2012); JC at 6.)

Accordingly, the undersigned hereby adopts the parties' proposed construction and shall construe "substantially oblong active regions" to mean "***an active region: (1) the length of***

[3] Cypress previously proposed the term "substantially oblong" as it is used in claims 1, 2, and 5 of the '805 patent be construed. Subsequent to the *Markman* hearing, Cypress withdrew its proposed construction of "substantially oblong" and stipulated to Respondents' construction of "substantially oblong" as used in the '805 patent. (*See* Notice Of Claim Construction With Respect To "Substantially Oblong" As Used In U.S. Patent No. 6,534,805 (Jan. 9, 2012).)

which is substantially constant and the width of which varies by approximately one-third or less along the length of the region; (2) the length of which is substantially constant and the width of which by design varies only with respect to the widths of the access and latch transistors; or (3) the length of which is greater than or equal to approximately three times its maximum width; and (4) which does not include markedly L-shaped regions."

c) "substantially oblong polysilicon structures"

The term "substantially oblong polysilicon structures" appears in claim 2 of the '805 patent. Cypress has stipulated to Respondents' proposed construction for this term, which is "a polysilicon structure the length of which is greater than about three times its width, provided that a polysilicon structure still is substantially oblong despite having a substantially wider region." (*See* Notice Of Claim Construction With Respect To "Substantially Oblong" As Used In U.S. Patent No. 6,534,805 (Jan. 9, 2012); JC at 6.)

Accordingly, the undersigned hereby construes "substantially oblong polysilicon structures" as "***a polysilicon structure the length of which is greater than about three times its width, provided that a polysilicon structure still is substantially oblong despite having a substantially wider region if the wider region solely accommodates a contact region.***"

d) "substantially oblong local interconnects"

Cypress and Respondents do not dispute the construction of the claim term "substantially oblong local interconnects," which appears in claim 5 of the '805 patent. All parties agree that said term should be construed as "a local interconnect the length of which is greater than or equal to approximately three times its maximum width." (*See* Notice Of Claim Construction With Respect To "Substantially Oblong" As Used In U.S. Patent No. 6,534,805 (Jan. 9, 2012); JC at 6.)

Accordingly, the undersigned shall hereby construe "substantially oblong local interconnects" to mean "***a local interconnect the length of which is greater than or equal to approximately three times its maximum width***."

2. Construction of Disputed Claim Term

a) "local interconnects"

The term "local interconnects" appears in claim 5 of the '805 patent. The parties disagree on the proper claim construction of the term, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Short, circuit connections confined to a particular region within a single memory cell	A relatively short circuit connection that does not extend across the entire memory cell

Cypress asserts that its claim construction comes straight from the specification. Cypress cites the following language: "Local interconnections are generally used for short runs relative to much longer metal conductors used for global connections. Thus, the term 'local interconnect' may refer to the function of connecting features within a circuit . . . ." (CMIB at 11 (citing '805 patent at 11:17-22).) Cypress states that the prosecution history further confirms this definition of the term wherein the patentee stated that the "local interconnects" are "confined to a particular region within a single memory cell." (CMIB at 11 (citing Ex. 2 at 4).)

Cypress argues that, contrary to the position of Respondents, the specification does not state that "local interconnects" are "relatively short circuit connection[s.]" Cypress argues that the specification actually says that "[l]ocal interconnects are generally used for short runs relative to much longer [] global connections." (CMIB at 11; CMRB at 7 (citing '805 patent at 11:18-20).) Cypress states that what the specification language is saying is that in comparison to global connections, that is "relatively" to global connections, local connections are shorter. Thus, Cypress asserts, in this context, it is clear what "relatively" means. (CMRB at 7.)

Cypress disagrees with Respondents' assertion that the part of their construction, "does not extend across the entire memory cell," is more "objectively stated" and easier to apply than the definition given in the prosecution history. Yet, Cypress alleges, Respondents concede that the prosecution history defines the term as "confined to a particular region within a memory cell." (CMRB at 8 (citing Ex. 2 at 4).) Cypress also argues that its definition is also consistent with the specification, which contemplates that local interconnects may "refer to the function of connecting features **'within a circuit.'**" (*Id.* (citing '805 patent at 11:20-21 (emphasis added)).) Cypress also argues that the prosecution history states that "a local interconnect does not extend across the entire cell such that when memory cells are abutted against each other, a local interconnect would extend globally across the entire integrated circuit comprising an array of memory cells." (*Id.* (citing Ex. 2 at 4).). Cypress claims that this confirms that the local interconnect is used in a single memory cell. (*Id.*)

In support of their claim interpretation, Respondents argue that the local interconnects should be "relatively short," as opposed to "short," as proposed by Cypress. Respondents state that the "relatively short" language comes from both the specification and the prosecution history. (RMIB at 19.) Respondents note that the specification states that the "[l]ocal interconnections are generally used for shorter runs relative to much longer metal connections used for global connections." (RMIB at 20; RMRB at 8 (citing '805 patent at 11:18-20).) Respondents argue that, during prosecution, the applicant stated, in the context of distinguishing prior art, that "[a] local interconnect is defined in the present specification as one which is relatively short . . . ." (RMIB at 20 (citing RX-3 at 4-5).) Thus, Respondents argue that the "relatively short" language of Respondents' proposed construction is well-supported in the intrinsic evidence.

Second, Respondents note that their construction states that a local interconnect "does not extend across the entire memory cell," whereas Cypress states that a local interconnect "is confined to a particular region within a memory cell." Respondents state that both of these statements come *verbatim* from the prosecution history except that Cypress adds the word "single" to its construction. (RMIB at 20 (citing RX-3 at 4-5).) Respondents state that they believe that these two statements make the same point, but "that the point is more objectively stated (and that it is easier to determine whether the claimed feature exists in a memory device) using the phrase 'does not extend across the entire memory cell.'" (*Id.*)

Taking into account the language from the prosecution history cited by the parties (RX-3 at 4-5) and the language of the specification ('805 patent at 11:18-20), the undersigned hereby construes the claim term "local interconnect" to mean "***a connection that is short relative to a much longer metal connection used for a global connection, is confined to a particular region within a memory cell, and does not extend across the entire memory cell.***"

VI. THE '134 PATENT

A. Overview

The '134 patent is entitled "Memory Device With Fixed Length Non Interruptible Burst." The '134 patent issued on November 18, 2003 to named inventor Cathal G. Phelan, and was subsequently assigned to Cypress. The '134 patent has 21 claims of which claims 1, 2 and 12–15 are asserted against Respondents. Claim 1 is an independent claim. Claim 2, 12, 13, 14, and 15 depend from claim 1. These claims read as follows (with the first instance of the agreed-upon terms highlighted in *italics* and the first instance of the disputed terms highlighted in **bold**):

1. A circuit comprising: a memory comprising a plurality of storage elements each configured to read and write data in response to an **internal address signal**; and a **logic circuit** configured to generate a **predetermined number of said internal address signals** in response to (i) an *external address signal*, (ii) a clock signal and (iii) one or

more control signals, wherein said generation of said predetermined number of internal address signals is *non-interruptible*.

2. The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed *burst* length.

12. The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

13. The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

14. A memory device according to claim 1, wherein said circuit is an integrated circuit.

15. The circuit according to claim 1, further comprising address and control busses configured to present said external address signal and said one or more control signals, wherein said busses are freed up during the generation of said predetermined number of internal address signals.

B. Agreed-Upon and Disputed Claim Terms

1. Construction of Agreed-Upon Claim Terms

a) "external address signal"

Cypress and Respondents agree that the term "external address signal," which appears in appears in claims 1, 13, and 15 of the '134 patent, should be construed as "an address signal that originates outside of the circuit." (JC at 7.)

Accordingly, the undersigned hereby adopts the parties' proposed construction and shall construe "external address signal" to mean "***an address signal that originates outside of the circuit***."

b) "non-interruptible"

Cypress and Respondents do not dispute the construction of the claim term "non-interruptible," which appears in claim 1 of the '134 patent. All parties agree that said term should be construed as "cannot be stopped or terminated once initiated until the fixed number of internal addresses has been generated." (*Id.* at 8.)

Accordingly, the undersigned hereby construes "non-interruptible" as "***cannot be stopped or terminated once initiated until the fixed number of internal addresses has been generated.***"

c) "burst"

The term "burst" appears in claim 2 of the '134 patent. The parties have agreed that said term should be interpreted to mean "a number of words transferred as a group." (*Id.*)

Accordingly, the undersigned shall hereby construe the term "burst" as "***a number of words transferred as a group.***"

2. Construction of Disputed Claim Terms

a) "internal address signal"

The term "internal address signal" appears in claims 1, 2, 12, and 15 of the '134 patent. The parties disagree on the proper claim construction, and construe the term as follows:

CYPRESS	RESPONDENTS
Address signal generated inside a logic circuit associated with a memory to enable said memory to read and write data to said memory	An address signal that is generated within the circuit claimed by the preamble

Cypress asserts that its proposed construction comes directly from the claim language itself, namely: "What is claimed is: A circuit comprising: a memory . . . ; and a logic circuit." (CMIB at 13 (citing '134 patent at 5:21-26; 10/14/11 Tr. at 56:20-22).) Cypress contends that, contrary to Respondents' objection, its construction does not read the word "internal" out of the claim for "Cypress's construction noted that the address signal is generated 'by' the 'logic circuit' and 'memory,' the two elements that make up the 'circuit' referenced by the preamble in claim 1." (CMRB at 11; *see also* CMIB at 14 (arguing that the signal is generated inside the circuit referenced in the preamble).)

Respondents submit that their proposed construction is consistent with the plain meaning of the word "internal." (RMIB at 25.) Respondents also claim that their construction is consistent with the understanding of the term to one of ordinary skill in the art, "who understands that the internal address signals are generated within the circuit." (*Id.* (citing RX-9 at ¶ 27).)

Cypress's construction, Respondents argue, fails to require that the claimed "internal address signal" be generated inside the circuit referenced in the preamble. (RMRB at 11; *see also* RMIB at 25 (arguing that Cypress's construction essentially writes the word "internal" out of the claim).) Respondents also assert that Cypress's construction incorrectly suggests that the internal address signals read and write data to the memory. Internal address signals, Respondents argue, do not themselves read and write; rather, they identify the locations in the memory to which data is written or from which it is read. (*Id.*)

The parties concede that while they agree on the substance (*i.e.*, that the internal address signal comes from the circuit referenced in the preamble), they cannot agree on the wording of the construction. (*See* 10/14/11 Tr. at 56:4-9, 57:22-23, 58:4-7, 59:9-22; CMIB at 14-15; RMIB at 25; *see also* '134 patent at Fig. 1.) The central dispute between the parties is whether the "a circuit" in the preamble of claim 1 is a claim limitation.[4]

According to Federal Circuit precedent, "a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim. *Catalina Mktg., Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). In other words, "if the preamble helps to determine the scope of the patent claim, then it is construed as part of the claimed invention." *NTP, Inc. v. Research in Motion, Ltd.*, 418 F.3d 1282, 1306 (Fed. Cir. 2005); *see also Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.*, 55 F.3d 615, 620

[4] Counsel for Cypress indicated at the *Markman* hearing that Cypress would agree to Respondents' construction if the word "referenced" was substituted for "claimed." (*See* 10/14/11 Tr. at 61:22-24 ("I won't belabor this, Your Honor. The circuit, referenced circuit. That would be fine to us.").)

(Fed. Cir. 1995). Furthermore, "[w]hen limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003). Here, the "said circuit" in dependent claim 14 derives its antecedent basis from "a circuit" recited in the claim 1 preamble. Because the preamble is necessary to provide context for an ensuing claim term, the undersigned finds that the preamble limits the scope of the claimed invention.[5]

Accordingly, the undersigned hereby construes "internal address signal" to mean "***an address signal that is generated within the circuit claimed by the preamble.***"

b) "logic circuit"

The term "logic circuit" appears in claims 1 and 12 of the '134 patent. The parties disagree on the proper claim construction, and construe the term as follows:

CYPRESS	RESPONDENTS
Plain meaning. Alternatively, "circuit that is designed to perform one or more logic operations or to represent logic functions."	A circuit within the circuit claimed by the preamble that receives an external address signal, a clock signal and one or more control signals

Cypress asserts that "logic circuit" needs no construction for "[a]ny person of ordinary skill in the art understands the term." (CMRB at 12.) However, to the extent the undersigned believes a construction is necessary, Cypress believes the term "logic circuit" should be construed according to its plain meaning, which is a "circuit that is designed to perform one or more logic operations or to represent logic functions." (CMIB at 15 (citing IEEE Dictionary (7th ed. 2000)).) As for Respondents' construction, Cypress contends that said construction is

[5] As noted above, Cypress does not dispute that the internal address signal comes from the circuit referenced in the preamble. (*See* CMIB at 14 ("The internal address signal, in other words, does come from the circuit referenced in the preamble.").) The fact that Cypress itself acknowledges that the preamble helps to determine the scope of claim 1 undercuts its argument that the preamble is not limiting. *See, e.g., Seachange Int'l, Inc. v. C-Cor Inc.*, 413 F.3d 1361, 1376 (Fed. Cir. 2005).

problematic for it "says only what a logic circuit ***does***, *i.e.*, its functionality, as opposed to what it ***is***." (CMRB at 12 (emphasis original).) Cypress further argues that Respondents' construction is circular and if adopted, would render other claim language superfluous. (*Id.*)

Respondents submit that their proposed construction follows the express teachings of the claims and the specification. (RMIB at 26; RMRB at 11.) In support thereof, Respondents assert that the claimed "logic circuit" resides within the claimed "circuit." (*Id.*) This is, Respondents contend, confirmed by the specification, which describes the logic circuit 102 as being part of circuit 100. (*Id.*) Respondents argue that Cypress's construction is incorrect for it does not require the claimed "logic circuit" to reside within the claimed "circuit." (RMIB at 27; RMRB at 11.) Respondents also object to Cypress's proposed construction as lacking support in the specification and being inconsistent with the understanding of one of ordinary skill in the art. (RMIB at 27-28.)

The undersigned concurs with Cypress's criticism of Respondents' proposed construction, finding their construction to fail because it provides little to no clarity as to the meaning of this term. In fact, were Respondents' construction of "logic circuit" inserted into claim 1, it would render the claim barely comprehensible as illustrated below:

> 1. A circuit comprising:
>
> a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and
>
> a [**circuit within the circuit claimed by the preamble that receives an external address signal, a clock signal and one or more control signals**] configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

('134 patent at claim 1 (insertion in brackets with emphasis added).) The undersigned also agrees with Cypress that a person of skill in the art would understand the plain meaning of "logic

circuit" to be "a circuit that is designed to perform one or more logic operations or to represent logic functions." (*See, e.g.*, McAlexander Decl. at ¶ 20; *see also* IEEE Dictionary at 637 (7th ed. 2000).)

Accordingly, the undersigned hereby construes the term "logic circuit" as "***a circuit that is designed to perform one or more logic operations or to represent logic functions***."

c) "predetermined number of [said] internal address signals"

The phrase "predetermined number of [said] internal address signals" appears in claims 1, 2, 12, and 15 of the '134 patent. The parties disagree on the proper claim construction, and construe the phrase as follows:

CYPRESS	RESPONDENTS
Plain meaning. Alternatively, "a fixed number of internal address signals."	A fixed number of internal address signals for a burst access

Cypress submits that the phrase "predetermined number of [said] internal address signals" should be construed according to its plain meaning. (CMIB at 15.) If a construction is necessary, Cypress believes that "predetermined number of [said] internal address signals" should be construed to mean "a fixed number of internal address signals" for this construction comports with the plain language of the claim and is well-supported by the specification. (*Id.* at 15-16; CMRB at 13.)

Cypress criticizes Respondents' construction as improperly adding on an extra limitation – "for a burst access." (*Id.*) Cypress argues that "[n]othing in *Phillips* or its progeny allows the Respondents to include an extra limitation when neither the claim nor the specification supports that limitation." (*Id.*) Cypress further asserts that claim 2 references "burst" with respect to a "predetermined number of internal address signals," and thus, under the doctrine of claim

differentiation, "for burst access" should not be read into claim 1. (*Id.* at 13-14 (arguing that the phrase "predetermined number of [said] internal address signals" should not include "for a burst access").)

Respondents assert that the claim language and specification confirm the "fixed number of internal address signals" must be for a "burst access." (RMIB at 27 (arguing, *inter alia*, that one of ordinary skill in the art would understand from the claim language that claim 1 is directed to a burst access); RMRB at 12 ("the claims are by necessity directed to a burst access.").) In this regard, Respondents insist that because the object and teaching of the patent is directed to burst accesses, any construction that divorces this claim term from a burst access would be untenable. (RMIB at 28.)

All parties appear to agree that "predetermined number of [said] internal address signals" should be construed to mean "a fixed number of internal address signals transferring," and the undersigned will not dispute that consensus. (*See* 10/14/11 Tr. at 66:4-7 ("The parties have otherwise essentially agreed that this is properly construed as a fixed number of internal address signals.").) The main point of contention between the parties is whether the "predetermined number of internal address signals" are used for a burst access. Respondents contend that by necessity this phrase refers to a burst access. Cypress disagrees. The undersigned agrees with Respondents, finding that the "predetermined number of internal address signals" are generated for a burst access to the memory.

As Respondents rightly note and Cypress does not dispute, the object and teaching of the '134 patent is directed to burst access. (*See, e.g.*, '134 patent at 1:13-18, 1:44-45, 1:57-66, 2:16-18, 2:26-30, 3:5-5:15.) While Cypress is indeed correct that claim 2 does reference a "fixed burst length," claim 2 does not introduce burst accesses; rather, claim 2 sets forth a specific way

to implement the burst access. In doing so, claim 2 presupposes that claim 1 is directed to burst accesses and thus, by necessity, the "predetermined number of internal address signals" in claim 1 must be for burst access to a memory. Thus, one of ordinary skill in the art would understand that the "predetermined number of [said] internal address signals" language in claim 1 refers to burst access. (*See* Murphy Initial Rpt. at ¶ 39; 10/14/11 Tr. at 66:22-67:4.)

Accordingly, the undersigned hereby construes the "predetermined number of [said] internal address signals" as "***a fixed number of internal address signals for a burst access***."

VII. THE '477 PATENT

A. Overview

The '477 patent is entitled "Memory Interface System And Method For Reducing Cycle Time Of Sequential Read And Write Accesses Using Separate Address And Data Buses." The '477 patent issued on November 28, 2006 to named inventors Thinh Tran, Joseph Tzou, and Suresh Parameswaran, and was subsequently assigned to Cypress. The '477 patent has 15 claims of which claims 8 and 9 are asserted against Respondents. Claim 8 is an independent claim. Claim 9 depends from claim 8. The asserted claims read as follows (with the first instance of the agreed-upon terms highlighted in *italics* and the first instance of the disputed terms highlighted in **bold**):

8. A method for accessing an array of storage elements, comprising: **storing** upon an input to a *multiplexer* a write address sent over a write address path; **sending** upon another input to the multiplexer a read address sent over a read address path *in parallel* with the write address path; *sensing read data* from the array of storage elements sent across a read data path read data accessed by the read address; and *while* sensing read data, *sending write data across a write data path* to be written to the array at the write address.

9. The method as recited in claim 8, wherein said storing comprises **holding the write address held within a set of registers.**

B. Agreed-Upon and Disputed Claim Terms

1. Construction of Agreed-Upon Claim Terms

a) "sensing read data"

Cypress and Respondents agree that the phrase "sensing read data," which appears in claim 8 of the '477 patent, should be interpreted as "detecting read data." (JC at 8.)

Accordingly, the undersigned hereby adopts the parties' proposed construction and shall construe "sensing read data" to mean "***detecting read data***."

b) "sending write data across a write data path"

Cypress and Respondents do not dispute the construction of the phrase "sending write data across a write data path," which appears in claim 8 of the '477 patent. All parties agree that said phrase should be construed as "moving write data across a write path." (*Id.*)

Accordingly, the undersigned hereby construes "sending write data across a write data path" as "***moving write data across a write path***."

c) "multiplexer"

The parties agree that the term "multiplexer," which appears in claim 8 of the '477 patent, means "a device or components that allow(s) the interleaving of two or more input signals to a single output line or terminal." (*Id.* at 9.)

Accordingly, the undersigned shall hereby construe the term "multiplexer" as "***a device or components that allow(s) the interleaving of two or more input signals to a single output line or terminal***."

d) "in parallel"

The phrase "in parallel" appears in claim 8 of the '477 patent. The parties have agreed the phrase should be construed as "separately from."

Accordingly, the undersigned hereby adopts the parties' construction and shall construe "in parallel" to mean "***separately from***."

e) "while"

Cypress and Respondents agree that the term "while," which appears in claim 8 of the '477 patent should be construed to mean "partially concurrent or concurrent."

Accordingly, the undersigned hereby adopts the parties' joint construction and shall construe the term "while" to mean "***partially concurrent or concurrent***."

2. Construction of Disputed Claim Terms

a) "storing" and "sending"

The terms "storing" and "sending" appear in claim 8 of the '477 patent. The parties disagree on the proper claim construction of the terms, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Plain meaning.	The claimed "storing" must occur on a different clock edge than the claimed "sending."

Cypress contends that the terms "storing" and "sending" need no construction, "as their plain meanings are clear in the context of the claims and in the field of digital circuit design." (CMIB at 19 (arguing that "[s]toring is storing; sending is sending."); CMRB at 18 ("the meanings of these terms are evident even to lay persons further obviating the need for construction.").)

Cypress objects to Respondents' construction, arguing that it "is not claim construction at all" because "it does not even purport to define what the terms mean. . . . [n]or does the proposed 'construction' distill technical jargon into commonly understood language." (CMRB at 15.) Cypress asserts that Respondents' proposed construction rewrites the claims to add

limitations from the first and second disclosed embodiments and thus is improper. (*Id.* at 16.) While Cypress agrees that an objective of the invention is to increase speed of the memory device by reducing cycle time, Cypress disputes that the claims are limited to achieve only that goal. (*Id.* at 16.) Cypress insists that simultaneous "storing" and "sending" is both possible and described in the specification. (*Id.* at 18.) In support thereof, Cypress provides diagrams of a proposed circuit capable of performing the method of claim 8, which on the rising edge of the clock cycle stores the write address in the register and simultaneously sends the read address to the multiplexer and the memory array. (*See* CMRB at 17-18.)

Respondents assert that the "unambiguous teaching of the specification" is that "storing" and "sending" must occur on the rising and falling edges of the same clock cycle. (RMIB at 33, 35 (citing '477 patent at 6:60-65 ("FIG. 3 is a timing diagram of read and write operations and, specifically shows a read operation followed by a write operation, both of which occur during a single clock cycle of the system clock. . . . [s]ynchronized to the rising and falling edges of the clock is the read enable and write enable circuit.").) Respondents contend that, in fact, this is the only way the disclosed invention can accomplish its purpose of reducing cycle time. (*Id.* at 36-38.) Respondents claim that storing cannot occur on one edge of a clock cycle and sending on the same edge of the next clock cycle because "[w]aiting a full clock cycle after a read address has been sent to send a write address" would not reduce cycle time and thus, "is directly contrary to the stated purpose of the alleged invention," as well as the express teaching of the specification. (*Id.* at 37-38 (citing *Fujitsu Ltd. v. Netgear Inc.*, 620 F.3d 1321 (Fed. Cir. 2010); *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351 (Fed. Cir. 2007); *Carroll Touch Inc. v. Electro Mech. Sys.* 15 F.3d 1573 (Fed. Cir. 1993)).) Respondents further insist that the read and

write address cannot be transmitted on the same clock edge of the same clock cycle because the read and write address paths share the same latch. (*Id.* at 36-37.)

As an initial matter, there appears to be no dispute between the parties that the plain meaning of "storing" and "sending" is evident to one of ordinary skill. Indeed, Respondents do not argue that "storing" and "sending" mean something other than "storing" and "sending" (*i.e.* plain meaning). Respondents, however, assert that read in light of the specification, the terms "storing" and "sending" must occur on the rising and falling edges of the same clock cycle. (RMIB at 33-38.) It is Respondents' addition of this timing limitation to the plain meaning of the terms that is contested.

Respondents argue that "the specification uniformly teach[es] that the claimed 'storing' and the claimed 'sending' occur on a different clock edge" of the same clock cycle. (*Id.* at 36.) The undersigned disagrees. The specification does, in fact, contemplate that the claimed "storing" and "sending" can occur on the same clock edge. (*See* '477 patent at 8:22-26 ("Therefore, portions of the read and write address operations can overlap one another. Moreover circuit 60 allows the read data to be output and stored along the read data path at the same time as write data is initiated onto the column select circuit.").) The undersigned is similarly not persuaded by Respondents' argument that the only way to achieve faster sequential read and write cycle time is by restricting the "storing" of the write address and the "sending" of the read address to different clock edges of a single clock cycle.[6] Claim 8 does not include any language restricting the timing of "storing" and "sending". Moreover, when the patentees intended to

[6] Respondents cite *Fujitsu* and *Carroll Touch* for the proposition that claims cannot be construed in a way that conflicts with the purpose of the invention. In those cases, the Federal Circuit rejected claim constructions that both read an express limitation ***out*** of the claim language and conflicted with the inventions' objectives. *See Fujitsu*, 620 F.3d at 1335 (rejecting a construction of "synchronously" that encompassed any temporal relationship); *Carroll Touch*, 15 F.3d at 1577-78 (rejecting a construction of "spaced apart" that included intersecting). The undersigned finds those cases inapposite. Here, Respondents are attempting to read a limitation from the preferred embodiment ***into*** the definition of "storing" and "sending" simply because they contend it is the only way to align the claim with the objective of the invention.

restrict the sequence of the patented method, they expressly did so by using words like "before" and "while" in the claim language. (*See* '477 patent 10:37-39 ("The method as recited in claim 8, further comprising forwarding the read address from the multiplexer ***before*** forwarding the write address."); 10:40-42 ("The method as recited in claim 8, further comprising forwarding the read address from the multiplexer ***while*** storing upon an input to the multiplexer the write address.").) The undersigned therefore finds that neither the claims nor the intrinsic record support the inclusion of such a limitation and agrees with Cypress that these terms should be given their ordinary and customary meaning. *Intervet Inc. v. Merial Ltd.*, 617 F.3d 1282, 1287 (Fed. Cir. 2010) (limitations from the specification are not to be imported into the claims); *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 (Fed. Cir. 2003) ("In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art.").

Accordingly, "storing" and "sending" shall be construed according to their plain meaning.

b) "holding the write address held within a set of registers"

The phrase "holding the write address held within a set of registers" appears in claim 9 of the '477 patent. The parties disagree on the proper claim construction of the term, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Plain meaning. Alternatively, "holding the write address within a set of registers."	Holding, at the output of a latch, the write address that is stored within a set of registers.

Cypress contends that the phrase "holding the write address held within a set of registers" needs no construction, as it is well understood by persons of ordinary skill in the art. (CMIB at 22; CMRB at 22.) Should, however, the undersigned deem construction necessary, Cypress submits the phrase be construed as: "holding the write address within a set of registers." (CMRB at 22; *see also* 10/14/11 Tr. at 81:7-13.) Cypress objects to Respondents' proposed construction as improperly appending additional language (*i.e*, "at the output of a latch") that is nowhere present in the claims.[7] (CMIB at 22.) In this regard, Cypress argues that the Respondents' construction is "entirely reliant on imported limitations from the preferred embodiments," and insists that "nothing in the intrinsic evidence shows or suggests that the patentees intended to limit the invention to embodiments using a 'latch.'" (*Id.* at 22.)

Respondents contend that the disputed phrase uses the verb "to hold" in two different ways: (1) "holding the write address"—"uses the word 'hold' in the sense of temporarily stopping something, as one does when staging a series of transmissions until the time comes to release what is being held;" and (2) "held within a set of registers"—"refers to the act of storing something in a location." (RMIB at 43-44.) The entire phrase, Respondents submit, "describes temporarily holding back a write address that was stored in a set of registers before it is released." (*Id.*) Because the '477 patent specification teaches that the "holding back" of a write address occurs after the write address is sent from the register to a latch, Respondents contend that "holding the write address held within a set of registers" must be construed as "holding, at the output of the latch, the write address that is stored within a set of registers." (RMIB at 44-45 (citing the '477 patent at 9:23-31 ("States F and G are similar to states B and C, which sends the

[7] Cypress would agree to Respondents' construction if the latch limitation was omitted. (*See* 10/14/11 Tr. at 81:20-25 ("With the exception of . . . "at the output of a latch' I'd be fine with [Respondents'] construction. If it simply said holding the write address that is stored within a set of registers, that's essentially the same as our construction.").)

next write address to the latch and holds within the latch to await the second internal clock transition, as shown by state 108 (Fig.6) . . . Overlap 110 is made possible due to the second latch 73 holding the write address . . .")).) As for Cypress's construction, Respondents argue that it is flawed because it omits one type of holding, *i.e.*, "held." (10/14/11 Tr. at 84:12-15.)

The undersigned finds both constructions problematic. Cypress's construction, on the one hand, reads the "held" action out of the claim. Respondents' construction, on the other hand, imports a limitation from one of the embodiments, *i.e.*, that the "holding" must occur at the output of a latch. While it is indeed correct that the one of the embodiments discloses holding the write address at a latch (*see* '477 patent at Fig. 6), there is no requirement that you must do so. In other words, write addresses may, but need not come directly from a latch. For example, it is conceivable that a write address can "come from a latch and then go to a register and only then go to the memory array." (*See* 10/14/11 Tr. at 82:19-21.) The undersigned therefore declines to limit this term as Respondents have proposed in the absence of an unequivocal statement from the inventor manifesting an intent to so limit the "holding" action to the "output of a latch." *Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1381 (Fed. Cir. 2009) ("[E]ven where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words of expressions of manifest exclusion or restriction."). Moreover, courts generally disfavor importing limitations into the claims from the specification. *See MBO Labs., Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007) ("[P]atent coverage is not necessarily limited to inventions that look like the ones in the figures. To hold otherwise would be to import limitations onto the claim from the specification, which is fraught with danger."); *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1288 (Fed. Cir. 2009) ("When consulting the specification to clarify

the meaning of claim terms, courts must take care not to import limitations into the claims from the specification."). Accordingly, the undersigned hereby construes the phrase "holding the write address held within a set of registers" as "***holding the write address that is stored within a set of registers***."

VIII. THE '937 PATENT

A. Overview

The '937 patent is entitled "Synchronous Random Access Memory Having a Read/Write Address Bus and Process for Writing to and Reading From the Same." The '937 patent issued on July 17, 2001 to named inventors Mathew R. Arcoleo, Cathal G. Phelan, Ashish Pancholy, and Simon J. Lovett, and was subsequently assigned to Cypress. The '937 patent has fourteen claims of which claims 1, 2, 6, 12, and 13 are asserted against Respondents. Claim 1 is an independent claim. Claims 2, 6, 12, and 13 depend from claim 1. The asserted claims read as follows (with the first instance of the agreed-upon terms highlighted in *italics* and the first instance of the disputed terms highlighted in **bold**):

1. A random access memory comprising: a random access memory array configured to transfer data to random write addresses and from random read addresses in said random access memory array in response to a periodic signal; a data input bus connected to said random access memory array; a data output bus connected to said random access memory array; and an address bus connected to said random access memory array and configured to provide said random read addresses and said random write addresses, **wherein said *periodic signal* is configured to control data transfer operations** (i) to said random access memory array **in response to a first transition of said periodic signal** and (ii) from said random access memory array in response to a second transition of said periodic signal, wherein said second transition of said periodic signal is **complementary** to said first transition of said periodic signal.

2. A random access memory as claimed in claim 1, further comprising a write circuit configured to write said data into said random access memory array at said random write address in response to one transition of said periodic signal, said one transition being either a rising transition or a falling transition.

6. A random access memory as claimed in claim 1, wherein said periodic signal comprises a periodic control signal.

12. A random access memory as claimed in claim 1, wherein each of said data input bus and said data output bus is unidirectional.

13. A random access memory as claimed in claim 1, wherein said periodic signal comprises a clock signal.

B. Agreed-Upon and Disputed Claim Terms

1. Construction of Agreed-Upon Claim Term

a) "periodic signal"

Cypress and Respondents agree that the term "periodic signal," which appears in claims 1, 2, 6, and 13 of the '937 patent, should be interpreted as "a signal that has an oscillating waveform, the frequency of which may be predicted and/or controlled in accordance with techniques known in the art, and that can be configured to control one or more circuit functions performed as part of a read operation or a write operation." (JC at 10.)

Accordingly, the undersigned hereby adopts the parties' proposed construction and shall construe "periodic signal" to mean "***a signal that has an oscillating waveform, the frequency of which may be predicted and/or controlled in accordance with techniques known in the art, and that can be configured to control one or more circuit functions performed as part of a read operation or a write operation***."

2. Construction of Disputed Claim Terms

a) "wherein said periodic signal is configured to control data transfer operations"

The term "wherein said periodic signal is configured to control data transfer operations" appears in claim 1 of the '937 patent. The parties disagree on the claim construction of said term, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Wherein the data transfer operations are synchronized to transitions of said periodic signal	The term "periodic signal" is already construed – this claim term otherwise has a plain meaning

Cypress asserts that its proposed construction is supported by the specification of the '937 patent. (CMRB at 28 (citing '937 patent at 3:11-20, 3:51-53).) Cypress claims that it is widely understood in the industry that synchronous circuits (*i.e.*, the type of circuit claimed by the '937 patent) are designed to respond or be synchronized to transitions of a periodic signal. (*Id.* (citing McAlexander Decl. at ¶ 29).) Cypress claims that by designing a circuit that is synchronized to a periodic signal, which is often a clock, the periodic signal is configured to control the memory circuit. (*Id.*)

Cypress disagrees with Respondents' proposed construction because Cypress claims that while synchronous memory operations may be triggered by clock signal transitions, the '937 patent makes clear that they are controlled and caused by other input signals. (*Id.* at 28-29 (citing McAlexander Decl. at ¶ 29).) For example, Cypress claims that the preferred embodiment initiates a READ command during a rising transition of the CLK periodic signal only when RPS and CS are logic level "0". (*Id.* at 29 (citing '937 patent at Fig. 3).) Similarly, Cypress claims that the preferred embodiment initiates a WRITE access during a rising transition of the CLK periodic signal only when WPS[8] and CS are logic level "0". (*Id.* at 29-30 (citing '937 patent at Fig. 4).) Thus, Cypress asserts that signals other than the periodic signal initiate, or control and cause, data transfer. (*Id.* at 30.) Specifically, Cypress asserts that data is transferred when the appropriate input or output signals are set and when a periodic signal has a transition. (*Id.*)

[8] Cypress's brief states "only when RPS and CS are logic level '0'," but it appears from the figure cited (Fig. 4) that it should have been WPS instead of RPS. (*See* CMRB at 29-30.)

In opposition, Respondents argue that Cypress's proposed construction is incorrect because the claim limitation itself states that the periodic signal must "control" the data transfer operations, which is also confirmed by the specification of the '937 patent. (RMRB at 21-22 (citing '937 patent at 1:53-54, 2:2-3, 3:9-10, 4:5-9, 4:27-28).) Respondents claim that Cypress's proposed construction reads the "control" requirement out of the claim and replaces it with "synchronized." (*Id.* at 21.) Respondents assert that having a first thing control a second thing is very different from having two things merely synchronized in some way. (*Id.*) Thus, Respondents claim that Cypress may not read the expressly recited "control" limitation out of the claim. (*Id.* (citing *Phillips*, 415 F.3d at 1312).)

Respondents also argue that the "in response to" language of claim 1 requires that the periodic signal transitions cause the data transfer operations. (*Id.* at 22; *see also* Section VIII.B.2.b. herein.) Respondents claim that some of Cypress's arguments even confirm that the claim requires causation and not merely synchronization. (*Id.* (citing CMIB at 24 ("Accordingly, data transfer operations are 'initiated . . . with,' 'triggered' by, and 'respon[d] to' the periodic signal . . . .")).) Respondents contend, however, that instead of reflecting causation, Cypress's proposed construction merely requires that the data transfer operations be "synchronized to" the periodic signal transitions. (*Id.*)

The undersigned finds Respondents' arguments persuasive. "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips*, 415 F.3d at 1312 (quoting *Vitronics*, 90 F.3d at 1582). Moreover, claims themselves provide substantial guidance as to the meaning of particular claim terms. *Id.* at 1314; *see also Vitronics*, 90 F.3d at 1582 ("First, we look to the words of the claims themselves, both asserted and nonasserted, to define the scope of the patented invention.") (internal citations omitted). Here, the claim limitation itself dictates

that the "periodic signal is *configured to control* data transfer operations." ('937 patent at 11:54-55 (emphasis added).) The undersigned disagrees with Cypress's assertion that "[b]y designing a circuit that is 'synchronized' to a periodic signal (often a clock), the periodic signal is 'configured to control' the memory circuit." (*See* CMRB at 28.) Describing two events as synchronized does not convey the idea of control. Indeed, two events could be synchronized, *i.e.*, occur or exist at the same time, yet one event does not control the other. Thus, the undersigned agrees with Respondents' contention that Cypress's proposed construction would essentially read the "control" limitation out of the claim. The undersigned finds the plain and ordinary meaning of the claim limitation to require control and not mere synchronization given that the specification of the '937 patent confirms that the periodic signal is used to "control" data transfer operations. (*See, e.g.,* '937 patent at 1:53-54, 2:2-3, 3:9-10, 4:5-9, 4:27-28.) In addition, portions of the specification cited by Cypress do not support its argument. For example, the specification states:

> The periodic signal may be configured to control one or more data transfer operations to or from the random access memory array in response to first and second transitions of the periodic signal, respectively, where the second transition is complementary to the first transition of the periodic signal. Therefore, the memory operates in a synchronous manner.

('937 patent at 3:11-20.) Contrary to Cypress's assertion that this supports the "synchronized to" language in its proposed construction, this excerpt actually indicates that the *result* of the periodic signal's control is that the memory operates in a synchronous manner, not that the periodic signal and the data transfer operations are merely synchronized. Furthermore, Cypress's argument that data transfer operations are controlled by other input signals is not persuasive. Regardless of whether other input signals (other than the periodic signal) may be involved in

initiating data transfer operations, the express language of the claim makes clear that at the very least, the periodic signal "is configured to control data transfer operations."

Having rejected Cypress's proposed construction, the undersigned hereby construes the term "wherein said periodic signal is configured to control data transfer operations" according to its plain meaning.

b) "in response to a . . . transition of said periodic signal"

The term "in response to a . . . transition of said periodic signal" appears in claims 1 and 2 of the '937 patent. The parties disagree on the claim construction of said term, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Plain meaning, or alternatively, "corresponding to a transition of said periodic signal"	Caused by the transition of said periodic signal

Cypress contends that this term needs no construction and that it has a plain meaning that is well-understood by persons skilled in the art. (CMIB at 26-27; CMRB at 27 (citing McAlexander Decl. at ¶ 28).) In the alternative, Cypress proposes that the plain meaning be "corresponding to a transition of said periodic signal," which Cypress claims is supported by the specification. (CMRB at 27 (citing '937 patent at 3:16-21).) Cypress contends that according to the specification, "the memory is linked to a periodic signal, and it takes action when there is a change of state in that periodic signal." (*Id.*)

Respondents submit that the "in response to" language in the claim requires that the "data transfer operations" be caused by the claimed "transitions" of the periodic signal. (RMRB at 20.) For example, Respondents claim that in explaining a write data transfer operation, the specification describes the write operation occurring on the falling edge of the positive clock. (RMIB at 53 (citing '937 patent at 8:13-18).) Likewise, Respondents claim that the specification

also describes read operations as occurring in response to the rising or falling edges of the periodic signal. (*Id.* (citing '937 patent at Table 2, 9:52-65).)

Respondents disagree with Cypress's proposed construction because it replaces the required causation with the mere correspondence of two events. (RMRB at 20.) Respondents assert that contrary to Cypress's arguments, the claim does not recite that two events must simply correspond in some manner – it expressly recites that the data transfer operations occur "in response to" the transitions of the periodic signal. (*Id.* at 20-21.) Thus, Respondents contend that Cypress's proposed construction is incorrect because it is contrary to the requirements of the claim. (*Id.* at 21.)

The undersigned finds Respondents' arguments persuasive because the '937 patent discloses a cause-and-effect relationship between the first and second transitions of the periodic signal and the data transfer operations. In describing read operations, the specification states that "[r]ead accesses can be initiated, for example, on every rising edge of the positive clock." ('937 patent at 7:31-32.) Similarly, with respect to write operations, the specification states that "[w]rite accesses can be initiated on every falling edge of the same clock that initiates read accesses." (*Id.* at 8:20-21.) The word "initiate" means "to cause or facilitate the beginning of." *Merriam-Webster's Collegiate Dictionary* (11th ed. 2003). Thus, the rising or falling edge of the clock, *i.e.*, the transition of the periodic signal, causes read or write operations, which are data transfer operations. Cypress's use of the word "corresponding" does not express a cause-and-effect relationship and is thus incorrect. The only support in the specification cited by Cypress is the statement that "the memory operates in a synchronous manner." (*See* CMRB at 27 (citing '937 patent at 3:16-21).) Cypress claims that this means that "the memory is linked to a periodic signal." However, as described above, there is a cause-and-effect relationship between the first

and second transitions of the periodic signal and the data transfer operations, not just a mere link. Thus, Cypress's proposed construction is not supported by the specification. Moreover, Cypress even admits that the memory "takes action *when* there is a change of state in that periodic signal." (*See id.* at 27 (emphasis added).) As with the phrase "in response to," the use of "when" denotes a causal relationship, and not just a correspondence.

Accordingly, the undersigned hereby construes the term "in response to a . . . transition of said periodic signal" as "***caused by the transition of said periodic signal.***"

c) "transition"

The term "transition" appears in claims 1 and 2 of the '937 patent. The parties disagree on the claim construction of said term, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Change of a periodic signal from one state to another	A falling or rising edge of the periodic signal

Cypress asserts that its proposed construction is straightforward and well-understood by persons of ordinary skill in the field. (CMIB at 24.) Cypress claims that the plain meaning of "transition," which in the context of the '937 patent, refers to either a falling or rising edge of the signal, is confirmed by the specification. (*Id.* (citing '937 patent at 4:34).) In addition, Cypress argues that Respondents' proposed construction fails to capture that a "transition" involves change between both an origin and a destination point. (CMRB at 26.) Thus, Cypress claims that while a falling or rising edge may result in a change from one state to another, it is unclear when that change occurs. (*Id.*)

Respondents contend that their proposed construction is correct and that Complainant agrees that the claimed "transitions" refer to rising and falling edges of the periodic signal. (RMRB at 19 (citing CMIB at 24).) Respondents claim that the rising and falling edges of the

signal constitute the acts of changing the state of the periodic signal from low to high and from high to low. (*Id.* at 19.) Respondents further claim that Cypress's proposed construction is incorrect because the term "transition" refers on its face to the actual transition itself, and not to the resulting logic level. (RMIB at 51.) Respondents assert that the specification of the '937 patent makes clear that the applicants considered a "transition" and a "logic" level to be distinct. (*Id.*) For example, Respondents claim that the specification teaches that a data transfer operation may occur in response to either a "transition" or a "logic" level. (*Id.* (citing '937 patent at 2:10-21, 3:55-60, 5:33-34).) Indeed, Respondents claim that the specification describes the alternative approaches of using a "transition or logic level," a "transition or level," or an "edge or logic level," at least 16 times. (*Id.* (citing '937 patent at 2:10-21, 3:55-60, 5:33-34, 46-65, 6:5, 30, 35, 42, 46, 9:22-23).) Moreover, Respondents claim that the specification also teaches that a "logic level" results from a "transition." (*Id.* (citing 7:9-10, 7:16-17, 9:65-66, 10:22-24).) Thus, Respondents claim that the specification makes clear that the applicants considered a "transition" and a "logic level" to be distinct things. (*Id.*)

The undersigned finds Respondents' arguments persuasive. On one hand, Cypress argues that Respondents' proposed construction is incorrect, yet on the other hand, Cypress admits that in the context of the '937 patent, "transition" refers to "either a falling or rising edge of the signal."[9] (*See* CMIB at 24.) In making that contention, Cypress even cites to a portion of the specification that states that "[a]ccesses can be initiated on any edge of any periodic signal." ('937 patent at 4:34.) Additionally, Cypress provides no evidence from the specification supporting its own proposed construction of "change of a periodic signal from one state to

[9] In Cypress's discussion of the term "complementary" (*see* below at Section VIII.B.2.d.), Cypress even states that "[p]ersons skilled in the art of digital circuit design recognize the term 'complementary' with a periodic signal as referring to either the falling edge or rising edge of that periodic signal." (CMIB at 26.) Because the term "complementary" in claim 1 refers to a "transition," this again supports Respondents' proposed construction for the term "transition."

another," and instead is forced to rely solely on extrinsic evidence from the IEEE Dictionary. (*See* CMIB at 24; CMRB at 26.) Extrinsic evidence, however, is generally viewed as less reliable than the patent itself in determining how to define claim terms. *Phillips*, 415 F.3d at 1317. Here, while the specification does not expressly assign a definition to the word "transition," it describes data transfer operations numerous times as occurring on the rising or falling edge of the periodic signal. ('937 patent at 3:55-60 ("the input port transfers data on one of the rising or falling edges . . . of the periodic signal cycle(s), and the output port transfers data on the other of the rising or falling edges . . . of the periodic signal cycle(s)"; 4:34 ("Accesses can be initiated on any edge of any periodic signal . . . ."); 7:30-31 ("Read accesses can be initiated, for example, on every rising edge of the positive clock."); 8:19-20 ("Write accesses can be initiated on every falling edge of the same clock that initiates read accesses . . . ."); 9:23-26 ("the input port select is preferably sampled on the rising edge of the positive clock input (CLK), and the output port select is preferably sampled on the falling edge of the positive clock input (CLK)").)

Accordingly, the undersigned hereby construes the term "transition" as "***a falling or rising edge of the periodic signal.***"

d) "complementary"

The term "complementary" appears in claim 1 of the '937 patent. The parties disagree on the claim construction of said term, and have proposed the following constructions:

CYPRESS	RESPONDENTS
Plain meaning, or alternatively, "reciprocal"	Opposite

Cypress claims that the term "complementary" need not be construed because its plain meaning is clear from the context of its use with "transition of said periodic signal." (CMIB at 26.) Cypress claims that persons skilled in the art would recognize the term "complementary"

with a periodic signal as referring to either the falling or rising edge of that periodic signal. (*Id.*; CMRB at 24.) However, in the alternative, Cypress proposes that the proper plain meaning is "reciprocal." (CMIB at 26.) Cypress submits that "complementary" within the context of claim 1 refers to the relationship between transitions within the same periodic signal. (CMRB at 25.) Cypress further submits that "[a]s each periodic signal needs both rising and falling transitions to function properly, the use of 'reciprocal' identifies the complementary transitions within the given signal." (*Id.*)

Cypress disagrees with Respondents' proposed construction because Cypress claims it limits the scope of the claim term to the preferred embodiment. (CMIB at 26 (citing '937 patent at 2:10-21).) Cypress further contends that Respondents' proposed construction is incorrect because without clarifying language, "opposite" could refer to spatial, temporal, or functional counterparts. (CMRB at 23.) Cypress also asserts that Respondents' citations to the specification do not support their position because those citations disclose complementary clock signals, not complementary transitions of the periodic signal. (*Id.*)

Respondents contend that in the context of the claimed transitions of a periodic signal, "complementary" is well-understood by those of ordinary skill in the art to mean "opposite." (RMIB at 49 (citing Murphy Initial Rpt. at ¶ 95); RMRB at 18 (citing Murphy Rpt. at ¶¶ 89-96).) For example, Respondents point to Table 3 of the specification, which describes "CLK" as a "Positive Clock input" and "$\overline{\text{CLK}}$" as a "Negative Clock input" that is "[c]omplementary to CLK." (RMIB at 49 (citing '937 patent at Table 3).)

Respondents also contend that Cypress does not present any evidence of how one of ordinary skill in the art understands this claim term and does not cite any part of the patent as supporting its proposed construction. (RMRB at 18.) Respondents disagree with Cypress's

reliance on an English language dictionary because it does not suggest that it applies to the field of SRAM design, or even memory design generally. (*Id.*)

The undersigned notes that claim 1, in part, recites that "said second transition of said periodic signal is complementary to said first transition of said periodic signal." ('937 patent at 11:59-61.) According to the specification, the periodic signal can be an internal or external clock signal or a set of differential input clocks, and "[a]ccesses can be initiated on any edge of any periodic signal." (*Id.* at 3:53-55, 4:26-31, 3:22-24, 4:34-35.) Moreover, "the second, complementary transition of the periodic signal is also the next transition following the first transition of the periodic signal." (*Id.* at 6:48-50.) Similarly, the specification explains that circuitry is operable to write data to or read data from the random access memory array "in response to successive transitions . . . of a periodic signal." (*Id.* at 5:28-36.) Thus, whether or not there is one periodic signal or a set of differential clocks, the second complementary transition is the next transition following the first transition of the periodic signal.

At the hearing, Cypress's counsel argued that Respondents' proposed construction was ambiguous because it ignores differential clocks. (*See* 10/14/2011 Tr. at 90:9-92:1.) The undersigned agrees, but finds that Cypress's proposed construction is ambiguous as well. In the case of a single periodic signal, if the first transition is a rising edge, the second transition will be the next transition, *i.e.*, the next falling edge. However, while claim 1 relates to one periodic signal, that periodic signal can comprise a pair of differential input clocks, *e.g.*, CLK and $\overline{\text{CLK}}$ as shown in Figure 5 of the '937 patent, reproduced below. (*See* '937 patent at 3:53-55, 4:26-31, 3:22-24.) For example, dependent claim 14, which is not presently asserted, recites that "said periodic signal comprises a differential input clock pair having a first clock signal configured to generate said first transition and a second clock signal configured to generate said second

transition." (*Id.* at 14:6-10.) Thus, pursuant to claim 14, in the case of a differential input clock, the first transition will be produced by the first clock signal (*e.g.*, CLK) and the second transition will be produced by the second clock signal (*e.g.*,). In this situation, both Cypress's and Respondents' proposed constructions are ambiguous. If the first transition is a rising edge of the first clock signal CLK, the second clock signal will generate the second complementary or next transition, *i.e.*, the next rising edge of the second clock signal. (*See id.* at Fig. 5, reproduced below.)

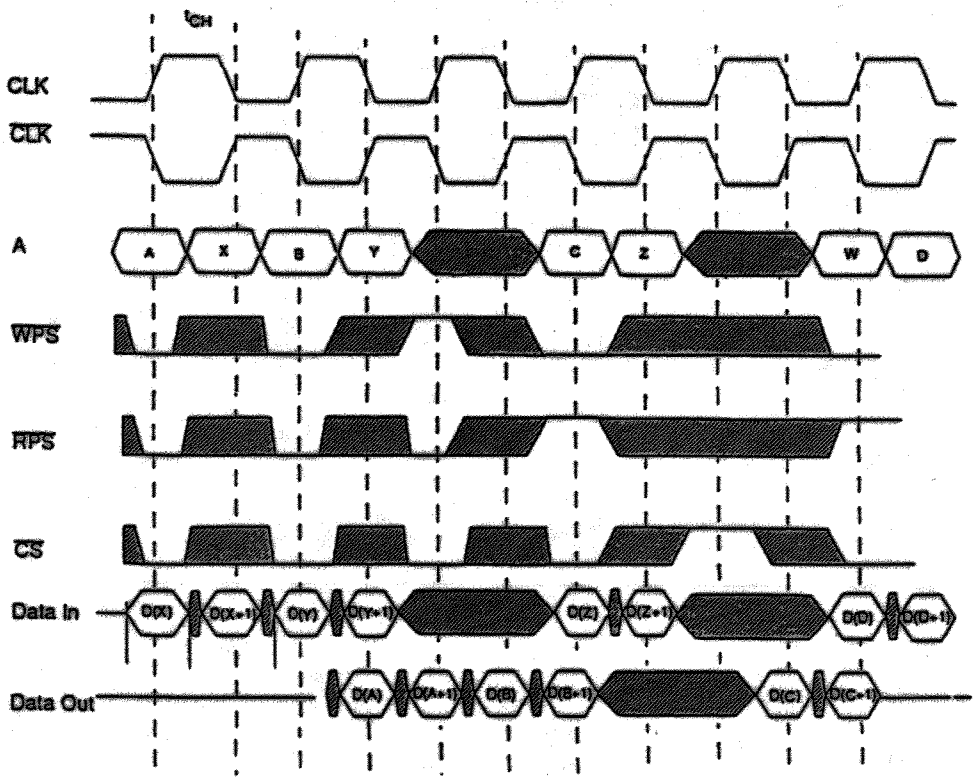

Fig. 5 of the '937 patent

It is unclear whether the next rising edge of the second clock signal can be considered "opposite" to or a "reciprocal" of the rising edge of the first clock signal, thus rendering the parties' proposed constructions ambiguous. However, according to the specification, it is "the next transition following the first transition of the periodic signal." (*Id.* at 6:48-50.)

Accordingly, the undersigned hereby construes the term "complementary" as "***the next subsequent transition of the periodic signal***."

SO ORDERED.

Charles E. Bullock
Chief Administrative Law Judge

IN THE MATTER OF CERTAIN STATIC RANDOM ACCESS MEMORIES AND PRODUCTS CONTAINING SAME **337-TA-792**

CERTIFICATE OF SERVICE

I, James R. Holbein, hereby certify that the attached **ORDER NO. 29** has been served upon, the following parties via first class mail and air mail where necessary on February 9, **2012.**

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IN THE MATTER OF CERTAIN STATIC RANDOM ACCESS MEMORIES AND PRODUCTS CONTAINING SAME **337-TA-792**

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