PUBLIC VERSION

United States International Trade Commission
Washington, DC 20436

In the Matter of **CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III)**	**Investigation No. 337-TA-630**

COMMISSION OPINION

This investigation is before the Commission for a final disposition. The Commission has determined to affirm the presiding administrative law judge's ("ALJ") determination that Respondents did not violate section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in connection with claims 1-4, 9, 10 and 33-35 of United States Patent No. 5,663,106 ("the '106 patent"), claims 17 and 18 of United States Patent No. 5,679,977 ("the '977 patent") and claims 1-4, 9-12, 15 and 16 of United States Patent No. 6,133,627 ("the '627 patent"). Specifically, the Commission has determined to (1) modify the ALJ's construction of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent; (2) reverse the ALJ's finding that the accused μBGA products do not meet all of the limitations of the asserted claims of the '106 patent but affirm his finding that there is no infringement due to patent exhaustion for these products; (3) affirm the ALJ's finding that the accused wBGA products do not infringe the asserted claims of the '106 patent; (4) affirm the ALJ's validity and domestic industry analyses pertaining to the asserted claims of the '106 patent; (5) affirm the ALJ's finding that the Direct Loading testing methodology employed by Complainant's expert fails to prove infringement; and (6) affirm the ALJ's finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17

and 18 of the '977 patent under the on-sale bar provision of 35 U.S.C. § 102(b), but modify a portion of the ALJ's final initial determination ("ID"). This opinion sets forth the Commission's reasoning underlying its determinations. The Commission adopts the ALJ's ID to the extent it is not inconsistent with this opinion.

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation on January 14, 2008, based on a complaint filed by Tessera, Inc. of San Jose, California ("Tessera"). 73 *Fed. Reg.* 2276 (Jan. 14, 2008). The complaint alleged violations of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips with minimized chip package size and products containing the same by reason of infringement of claims 1-4, 9, 10 and 33-35 of the '106 patent; claims 17 and 18 of the '977 patent; claims 1-4, 6, 9-12, 15 and 16 of the '627 patent; and claim 4 of United States Patent No. 6,458,681 ("the '681 patent"). Tessera named eighteen respondents.

On May 29, 2008, the ALJ[1] granted Tessera's motion to terminate the '681 patent from the investigation. *See* Order No. 16. On June 20, 2008, the Commission determined not to review the order. *See* Notice of Commission Determination Not to Review an Initial Determination Granting Complainant's Motion for Partial Termination of the Investigation with Respect to

[1] The investigation was originally assigned to Judge Bullock. On July 11, 2008, the investigation was reassigned to Judge Essex. *See* Notice of Commission Decision to Reassign Certain Section 337 Investigations.

United States Patent No. 6,458,681.

After the termination of several respondents based on settlement agreements, consent orders and defaults,[2] the following groups of respondents remained in the investigation:

1. Acer Inc. of Taipei, Taiwan; and Acer America Corp. of San Jose, CA (collectively, "Acer");
2. Centon Electronics, Inc. of Aliso Viejo, CA ("Centon");
3. Elpida Memory, Inc. of Tokyo, Japan; and Elpida Memory (USA), Inc. of Sunnyvale, CA (collectively, "Elpida");
4. Kingston Technology Co., Inc. of Fountain Valley, CA ("Kingston");
5. Nanya Technology Corporation of Taoyuan, Taiwan; and Nanya Technology Corp. USA of San Jose, CA (collectively, "Nanya");
6. Powerchip Semiconductor Corporation of Hsinchu, Taiwan ("Powerchip");
7. ProMOS Technologies, Inc. of Hsinchu, Taiwan ("ProMOS");
8. Ramaxel Technology Ltd of Hong Kong, China ("Ramaxel"); and
9. SMART Modular Technologies, Inc. of Fremont, CA ("SMART").

The ALJ held an evidentiary hearing from September 19, 2008, to October 3, 2008, and thereafter received post-hearing briefing from the parties. During the hearing, the ALJ granted Tessera's motion to withdraw claim 6 of the '627 patent from the investigation. Hearing Tr. at

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[2] The investigation was terminated as to respondents International Sourcing Group, Inc. (Order No. 17), Peripheral Devices and Product Systems d/b/a Patriot Memory (Order No. 25), and A-Data Technology Co., Ltd., and A-Data Technology (USA) Co. (Order No. 35) based on consent orders and/or settlement agreements. *See* Notice of Commission Determination Not to Review an Initial Determination Granting Joint Motion to Terminate Investigation as to One Respondent Based on Consent Order and Settlement Agreement (July 14, 2008); Notice Of Commission Determination Not To Review an Initial Determination Granting a Joint Motion to Terminate the Investigation as to Respondent Patriot Memory Based on a Consent Order and Settlement Agreement; Issuance Of Consent Order (Oct. 2, 2008); Notice of Commission Determination Not to Review an Initial Determination Granting the Motion of Respondent A-Data Technology Co., Ltd., and A-Data Technology (USA) Co. to Terminate the Investigation as to Them Based on a Consent Order; Issuance of Consent Order (Oct. 23, 2008). TwinMOS Technologies, Inc. and TwinMOS Technologies, USA, Inc. defaulted. *See* Order No 46; Notice of Commission Determination Not to Review an Initial Determination Finding Two Respondents in Default (Sept. 15, 2009).

95:23-25.

On January 30, 2009, the Commission issued its decision to review in part the final initial determination finding no violation of section 337 in a related investigation, Investigation No. 337-TA-605 ("the 605 Investigation"). *See* Notice of Commission Decision to Review in Part a Final Initial Determination Finding No Violation of Section 337. The '977 and '627 patents and the patents that were asserted in the 605 Investigation, U.S. Patent Nos. 5,852,326 and 6,433,419, belong to the same family of patents and name identical inventors. In addition, Tessera, the complainant in this investigation, was also the complainant in the 605 Investigation and relied on the same testing methodology employed by the same expert, Dr. Qu, to prove infringement in both investigations. Because of the Commission's decision to review in part the final initial determination in the 605 Investigation, the ALJ extended the target date in this investigation due to the relationship between the patents at issue in both investigations as well as the fact that the Commission was reviewing the methodology used by Tessera in the 605 Investigation, which is the same methodology used in this investigation to prove infringement. *See* Order No. 40. The Commission determined not to review Order No. 40. *See* Notice of Commission Decision Not to Review an Initial Determination Extending the Target Date for Completion of This Investigation.

On April 2, 2009, the ALJ extended the target date in this investigation to November 17, 2009, based on the Commission's decision to request additional briefing on remedy and to extend the target date in the 605 Investigation. *See* Order No. 41. On April 23, 2009, the Commission determined not to review Order No. 41. *See* Notice of Commission Decision Not to Review an

Initial Determination Extending the Target Date for Completion of This Investigation.

On May 20, 2009, the Commission issued its opinion in the 605 Investigation. *See Certain Semiconductor Chips With Minimized Chip Package Size and Products Containing Same,* Inv. No. 337-TA-605, Commission Opinion (May 20, 2009). On June 3, 2009, the Commission issued a public version of its opinion. *See Certain Semiconductor Chips With Minimized Chip Package Size and Products Containing Same,* Inv. No. 337-TA-605, Commission Opinion (Public Version) (May 20, 2009) ("605 Comm'n Op").

On June 12, 2009, the ALJ issued Order No. 43, seeking supplemental briefing on "how the Commission's Opinion in the 605 Investigation and its findings on Dr. Qu's infringement analysis will affect the ALJ's analysis in this investigation, if at all." *See* Order No. 43 at 2. In light of the supplemental briefing, the ALJ extended the target date in this investigation to December 29, 2009, with the final initial determination on violation being due no later than the close of business on August 28, 2009. *See* Order No. 43. On July 13, 2009, the Commission determined not to review Order No. 43. *See* Notice of Commission Determination Not to Review an Initial Determination Extending the Target Date for Completion of the Investigation by Six Weeks.

On August 28, 2009, the ALJ issued his final ID, finding no violation of section 337 by Respondents with respect to any of the asserted claims of the asserted patents. Specifically, the ALJ found that the accused products do not infringe the asserted claims of the '106 patent. ID at 53-54. The ALJ also found that none of the cited references anticipated the asserted claims and

that none of the cited references rendered the asserted claims obvious. ID at 109-116, 132-134. The ALJ further found that the asserted claims of the '106 patent satisfied the requirements of 35 U.S.C. § 112, first, second and fourth paragraphs. ID at 135-136. Likewise, the ALJ found that the accused products do not infringe the asserted claims of the '977 and '627 patents and that none of the cited references anticipated the asserted claims. ID at 79-80, 97, 118-126. The ALJ further found that the asserted claims of the '977 and '627 patents satisfied the definiteness requirement of 35 U.S.C. § 112, second paragraph, and that Respondents waived their argument with respect to obviousness. ID at 134, 136-139. The ALJ also found that all chips Respondents purchased from Tessera licensees were authorized to be sold by Tessera and, thus, Tessera's rights in those chips became subject to exhaustion, but that Respondents, except Elpida, did not purchase all their chips from Tessera licensees. ID at 143-153. The ALJ concluded that an industry existed within the United States with respect to Tessera's products that practiced the '106, '977 and '627 patents, as required by 19 U.S.C. § 1337(a)(2) and (3). ID at 154.

On September 17, 2009, Tessera filed a petition requesting review of the ALJ's construction of claim terms "top layer" and "thereon" recited in independent claim 1 of the '106 patent, the ALJ's finding that the testing methodology employed by its expert to prove infringement is unreliable, and the ALJ's finding that all chips Respondents purchased from Tessera licensees were authorized to be sold by Tessera and thus Tessera's rights in those chips became subject to exhaustion. *See* Complainant Tessera's Petition for Review of Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and

Bond ("Tessera Pet."). That same day, the Commission investigative attorney ("IA") also filed a petition seeking review of the ALJ's construction and application of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent as well as the ALJ's finding that the testing methodology employed by Tessera's expert to prove infringement is unreliable. *See* Office of Unfair Import Investigations' Petition for Review of the Initial Determination ("IA Pet."). Also on September 17, 2009, Respondents filed various contingent petitions for review of the ALJ's findings should the Commission decide to review the subject ID. The contingent petitions sought review of the ALJ's construction of claim terms "providing a protective barrier," "terminals" and "above" recited in asserted claim 1 of the '106 patent and the ALJ's findings regarding validity of the asserted claims and the adequacy of Respondents' representative products tested by Tessera for infringement. On October 1, 2009, Tessera, Respondents and the IA filed replies to the petitions for review.

On October 30, 2009, the Commission determined to review the final ID in part and requested briefing on several pertinent issues, and on remedy, the public interest and bonding. 74 *Fed. Reg.* 57192 (Nov. 4, 2009). The Commission determined to review (1) the finding that the claim term "top layer" recited in claim 1 of the '106 patent means "an outer layer of the chip assembly upon which the terminals are fixed," the requirement that "the 'top layer' is a single layer," and the effect of the findings on the infringement analysis, invalidity analysis and domestic industry analysis; (2) the finding that the claim term "thereon" recited in claim 1 of the '106 patent requires "disposing the terminals on the top surface of the top layer," and its effect on the

infringement analysis, invalidity analysis and domestic industry analysis; (3) the finding that the Direct Loading testing methodology employed by Tessera's expert to prove infringement is unreliable; and (4) the finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent. *Id.* The Commission determined not to review the remaining issues decided in the ID. In its notice of review, the Commission asked the parties the following questions:

1. Would the accused products infringe the asserted claims of the '106 patent if construction of the claim term "top layer" does not encompass only a single layer? Please cite record evidence and/or relevant legal precedent to support your position.

2. Did the patentees of the '106 patent expressly disclaim the embodiment described in Figure 7 of United States Patent No. 5,148, 265 ("the '265 patent")? How would that affect the infringement analysis of the asserted claims of the '106 patent? *See* '106 Patent Prosecution History (JX-167) June 24, 1996, Office Action and December 24, 1996, Amendment; '265 patent (JX-2) at column 14, lines 19-34; FIG. 7. Please cite record evidence and relevant legal authority to support your position.

3. Does Dr. Qu state anywhere in the record that he relied on his direct loading testing methodology to independently prove infringement of the asserted claims of the '977 and '627 patents by the accused packages? Please cite only record evidence.

4. Was Dr. Qu's demonstrated stress relief in the solder balls of the accused packages due to terminal-to-chip displacement caused by the applied external load? Please cite only record evidence.

On November 13, 2009, the parties filed written submissions on the issues under review, remedy, the public interest and bonding. *See* Complainant Tessera, Inc.'s Response to Commission Questions on Review of ID ("Tessera Br."); OUII's Response to Notice of

Commission Determination to Review in Part a Final ID Finding No Violation of Section 337 and to Commission Questions ("IA Br."); Response to Commission Review of ID by Respondents Acer, Nanya, and Powerchip ("Resp Br."). On November 20, 2009, the parties filed reply briefs.

B. Patents and Technology at Issue

This investigation involves both semiconductor chip packages and a process for encapsulating certain semiconductor chip packages. ID at 8. The technology at issue in the '977 and '627 patents is generally directed to semiconductor chip packages and specifically to semiconductor chips having ball grid array ("BGA") packages that use solder balls to connect the semiconductor chip to a printed circuit board ("PCB") through an array of tiny solder balls that are arranged in a grid-like pattern under the package. *Id.* The technology at issue in the '106 patent is generally directed to a method of encapsulating small format BGA semiconductor chip packages, including DRAM chip packages. *Id.*

The BGA packages at issue in this investigation are either in the "face-up" or "face-down" orientation. *Id.* The orientation of a chip package is determined based on the orientation of the "face" of the semiconductor chip, which is the surface of the chip that contains the circuitry and contacts for electrical connection. *Id.* In a "face-up" BGA, the face points away from the PCB, whereas in a "face-down" BGA, the face points in the direction of the PCB. *Id.*

To prevent damage to the wire bonds or leads, the chip and other elements of the package during use, the chip is coated with a protective layer of encapsulant, in a process known as encapsulation. Tessera Pet. at 7-8. During the encapsulation process, the terminals of the package

are typically exposed and, because of the small size of the packages, encapsulation commonly contaminates the terminals. *Id.* Such contamination inhibits the ability to connect the package to the other system components and undermines the usability of the package. *Id.* The '106 patent discloses an allegedly novel process of protecting terminals of a face-down BGA package during the encapsulation process. *Id.* The process protects the terminals from contamination by using a protective barrier that comes in contact with the layer of the package that carries the exposed terminals. *Id.*

The '977 and '627 patents address certain problems attributable to stress caused by mismatches in coefficients of thermal expansion ("CTE") between the various materials, *e.g.*, the semiconductor chip, the package substrate, and/or the PCB, used in a semiconductor assembly. *Id.* at 44-47. Semiconductor devices generate heat during operation and subsequently cool when operation ceases. *Id.* Because the different materials have different CTEs, they expand and contract at different rates in response to temperature changes, leading to differential thermal expansion ("DTE") between the materials. *Id.* Moreover, joining together multiple materials with different CTEs causes the CTE of the combination to be different from any single material. *Id.* The repeated cycles of heating and cooling can place stress and strain on the electrical interconnections in a semiconductor assembly, particularly the solder balls, leading ultimately to breakage and electrical failure in the package. *Id.*

The asserted patents disclose an allegedly novel way to avoid the problem of stress and strain associated with DTE. *Id.* By using structures that transfer at least some of the strain from

the solder balls, or solder joints, into the semiconductor package itself, the asserted patents move strain from the outside of the package to the inside of the package, thereby improving reliability of the external connections. *Id.* As an example, the patents teach that this can be accomplished by introducing a compliant layer between the chip and the backing element to allow the package terminals to move relative to the chip when the package is heated and cooled. *Id.* By permitting this movement to occur, the patents claim that the inventive structures appreciably relieve the stresses that would otherwise be present in the solder balls as a result of DTE between the chip and the PCB. *Id.* In other words, the asserted patents teach transferring the strain from second-level electrical interconnections outside of the package *(e.g.,* solder balls) into the package using particular structures that allow relative movement between the chip and the terminals. *Id.*

The '106 patent, entitled "Method of Encapsulating Die and Chip Carrier," issued on September 2, 1997, to Konstantine Karavakis, Thomas H. Distefano, John W. Smith Jr. and Craig Mitchell. Tessera owns the '106 patent and has asserted claims 1-4, 9, 10 and 33-35 in this investigation. ID at 10-11. The '106 patent incorporates by reference two United States patents: United States Patent No. 5,148, 265 ("the '265 patent") and United States Patent No. 5,477,611 ("the '611 patent").[3]

The '977 patent, entitled "Semiconductor Chip Assemblies, Method of Making Same and

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[3] Patents incorporated by reference into another patent become part of that patent and the incorporated patents' disclosures become "effectively part of [that patent] as if [they] were explicitly contained therein." *Cook Biotech Inc. v. Acell, Inc.*, 460 F.3d 1365, 1367 (Fed. Cir. 2006).

Components for Same," issued on October 21, 1997, to Igor Y. Khandros and Thomas H. Distefano. Tessera owns the patent and has asserted claims 17 and 18 in this investigation. ID at 11-12.

The '627 patent, entitled "Semiconductor Chip Package with Center Contacts," issued on October 17, 2000, to Igor Y. Khandros and Thomas H. Distefano. Tessera owns the patent and has asserted claims 1-4, 9-12 and 15-16 in this investigation. ID at 12-14.

C. Products at Issue

The accused products in this investigation are primarily DRAM packages in the face-down orientation having a "center bonded" structure, where the chip is connected to the package substrate through wire bonds routed through a channel formed across the center of the package substrate. Tessera Pet. at 4. A few of the accused products have a face-up orientation or stacked configuration, with multiple chips being stacked on top of each other within a single package. *Id.* A majority of the accused packages use a laminate package substrate (wBGA packages), although a small handful use polyimide tape instead (μBGA packages). *Id.*

Specifically, products accused of infringing the '106 patent have the following characteristics: "(1) BGA packages, (2) that contain one or more chips where the chip nearest the package substrate is in a face-down orientation and (3) the chip is electrically bonded to the package substrate through a window in that substrate." *Id.* Products accused of infringing the '977 and '627 patents include packages that have the following characteristics: "(1) BGA packages (2) with solder ball pitch of 1.2 mm or less, (3) with at least one solder ball under the

die, (4) with a die attach modulus of elasticity of 3.5 GPa or less and (5) with more than 36 solder balls." *Id.*

Each Respondent manufactures or sells DRAM chip packages, memory modules, and/or consumer electronic products containing either DRAM chip packages or memory modules. ID at 14. Complainant Tessera does not manufacture products meeting the description of the accused products at issue. *Id.* Instead, Tessera's business is in developing and licensing technologies. *Id.*

II. STANDARD OF REVIEW

Under the Administrative Procedure Act, upon review of the initial determination of the ALJ, "the agency has all of the powers which it would have in making the initial decision except as it may limit the issues on notice or by rule." 5 U.S.C. § 557(b); *Certain Acid-Washed Garments and Accessories*, Inv. No. 337-TA-324, Commission Opinion at 4-5 (Aug. 28, 1992) (the Commission examines for itself the record on the issues under review); 19 C.F.R. § 210.45(c). In other words, once the Commission decides to review the decision of the ALJ, the Commission may conduct a review of the findings of fact and conclusions of law presented by the record under a *de novo* standard.

III. CLAIM CONSTRUCTION

A. Legal Standard

Claim construction "begin[s] with and remain[s] centered on the language of the claims themselves." *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 830 (Fed. Cir. 2003). That is, the words of the claims "define the scope of the patented invention." *Vitronics Corp. v.*

Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art, viewing the claim terms in the context of the entire patent. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*). In construing claims, a court looks first to the intrinsic evidence, which consists of the language of the claims, the patent's specification and the prosecution history, as such evidence "is the most significant source of the legally operative meaning of disputed claim language." *Vitronics,* 90 F.3d at 1582. The claims themselves, however, "provide substantial guidance as to the meaning of particular claim terms." *Phillips,* 415 F.3d at 1314. In addition, it is essential to consider a claim as a whole when construing each term, because the context in which a term is used in a claim "can be highly instructive." *Id.*

When the meaning of a claim term remains uncertain, the specification is usually the first and best place to look, aside from the claim itself, in order to find that meaning. *Phillips,* 415 F.3d at 1315. The specification of a patent "acts as a dictionary" both "when it expressly defines terms used in the claims" and "when it defines terms by implication." *Vitronics,* 90 F.3d at 1582; *Phillips,* 415 F.3d at 1323. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Phillips,* 415 F.3d at 1316. "[I]t is axiomatic that a claim construction that excludes a preferred embodiment . . . is rarely, if ever correct and would require highly persuasive evidentiary support." *Anchor Wall Sys. v. Rockwood Retaining Walls Inc.*, 340 F.3d 1298, 1308 (Fed. Cir. 2003) (quoting *Vitronics,* 90 F.3d at 1583). A court, however, may not

read particular examples or embodiments discussed in the specification into the claims as limitations. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*). "Absent a clear disclaimer of particular subject matter, the fact that the inventor anticipated that the invention may be used in a particular manner does not limit the scope to that narrow context." *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301 (Fed. Cir. 2003).

The prosecution history, which includes the cited prior art "provides evidence of how the PTO [United States Patent and Trademark Office] and the inventor understood the patent." *Phillips,* 415 F.3d at 1317. The prosecution history may inform the meaning of the claim language by demonstrating how an inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it otherwise would be. *Vitronics,* 90 F.3d at 1582-83. "The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution." *Chimie v. PPG Indus., Inc.,* 402 F.3d 1371, 1384 (Fed. Cir. 2005). For example, "[a]n amendment or argument made in the course of prosecution may . . . serve as a disclaimer of a particular interpretation of a claim term." *Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 345 F.3d 1318, 1328-29 (Fed. Cir. 2003). For prosecution history disclaimer to attach, however, "the alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable." *Omega Eng'g, Inc. v. Raytek Corp.*, 34 F.3d 1314, 1326 (Fed. Cir. 2003). Moreover, "[t]here is no 'clear and unmistakable' disclaimer if a prosecution argument is subject to more than one reasonable interpretation, one of which is consistent with a proffered meaning

of the disputed term." *SanDisk Corp. v. Memorex Prods.*, 415 F.3d 1278, 1287 (Fed. Cir. 2005).

Differences between claims may be helpful in understanding the meaning of claim terms. *Phillips,* 415 F.3d at 1314. A claim construction that gives meaning to all the terms of a claim is preferred over one that does not do so. *Merck &* Co. *v. Teva Pharms. USA, Inc.,* 395 F.3d 1364, 1372 (Fed. Cir. 2005). In addition, the presence of a specific limitation in a dependent claim raises a presumption that the limitation is not present in the independent claim. *Phillips,* 415 F.3d at 1315. This presumption of claim differentiation is especially strong when the only difference between the independent and dependent claim is the limitation in dispute. *SunRace Roots Enter. Co. v. SRAM Corp.,* 336 F.3d 1298, 1303 (Fed. Cir. 2003).

B. Construction of the Claim Term "Top Layer" Recited in Asserted Independent Claim 1 of the '106 Patent

The Commission determined to review the finding that the claim term "top layer" recited in claim 1 of the '106 patent means "an outer layer of the chip assembly upon which the terminals are fixed," the requirement that "the 'top layer' is a single layer," and the effect of these findings on the infringement analysis, invalidity analysis and domestic industry analysis. Claim 1 of the '106 patent, with the key claim term emphasized for clarity, is reproduced below:

1. A method of encapsulating a semiconductor chip assembly having a **top layer** with an array of exposed terminals thereon, the terminals being electrically connected to the chip, said method comprising the steps of:

> placing an encapsulant barrier adjacent the semiconductor chip assembly, said encapsulant barrier at least partially defining an encapsulant area;
>
> providing a protective barrier in contact with said **top layer** for

> protecting the terminals on the **top layer** from an encapsulant material; and
>
> introducing an encapsulation material into at least a portion of the encapsulation area so that the encapsulation material flows to fill the encapsulation area and then cures to a substantially solid condition, the protective barrier preventing the encapsulation material from contacting the terminals on the **top layer**.

The ALJ construed the claim term "top layer" as "an outer layer of the chip assembly upon which the terminals are fixed," adding that "the 'top layer' is a single layer." ID at 24. We find that the ALJ erred in his construction of the claim term. Specifically, by adding the word "outer" to his claim construction, the ALJ impermissibly broadened the claim, and by requiring a single layer, the ALJ impermissibly narrowed the claim. We therefore modify the ALJ's claim construction by reversing his substitution of "outer" for "top" and reversing his requirement that "the 'top layer' is a single layer."

The claim at issue recites "[a] method of encapsulating a semiconductor chip assembly having a top layer with an array of exposed terminals thereon." In other words, the plain language of the claim specifically requires that the "array of terminals" be located on a **top** layer. By substituting the word "outer" for "top," the ALJ improperly broadened the claim term because the word "outer" includes more scope than "top." For example, "outer" can refer to "top," "bottom" or "sides." In addition, the '106 patent incorporates by reference, the '265 patent, which defines a frame of reference for "top." The '265 patent states:

> The front or contact-bearing face 22 of the chip is regarded as **defining the top of the chip**. Thus, in specifying direction pointing out of front face 22, and away from the chip, *i.e.*, the

> direction pointing out of the plane of the drawing towards the viewer in FIG. 1. The downward direction is the opposite direction. As used in the present disclosure with respect to a semiconductor chip assembly, such terms should be understood as based on this convention and should not be understood as implying any particular direction with respect to the ordinary gravitational frame of reference.

'265 patent, col. 9, ll. 22-33 (emphasis added). In other words, the patent requires that "[t]he front or contact-bearing face" of the chip is the top of the chip and specifies a direction for "top." We share Tessera's view that "top" as recited in the patent modifies "layer" by providing specific directional reference, and the ALJ's construction, substituting the word "outer" for "top" renders the claim term "top" meaningless because "outer" does not provide any directional reference. Moreover, the ALJ's construction does not include language that would account for the directional reference that the claim term "top" conveys.

Tessera also asserted that the "top layer" need not be limited to a single layer but that it could encompass a composite layer as well. The ALJ rejected this assertion, finding that "top layer" meant a single layer. ID at 22. In reaching his decision, the ALJ noted that Figure 1 of the '106 patent describes a semiconductor chip and chip carrier, wherein "[t]he chip carrier 14 is made up of a top layer 16 (preferably a polyimide layer or the like) and an elastomeric pad 20 disposed between the top layer 16 and the semiconductor chip 12" and that "other embodiments in the '106 patent similarly describe the top layer as separate and distinct from the elastomeric pad, which in combination form the chip carrier." ID at 23 (citing '106 patent, col. 5, ll. 8-13;

col. 7, ll. 22-26; col. 9, ll. 1-4; Figures 1, 9, and 13). The ALJ further noted that the '265 patent specification describes an interposer, a component of the chip carrier, as "includ[ing] a flexible top layer 38 (FIG.3) formed by a thin sheet of material having a relatively high elastic modulus and a compliant bottom layer formed from a material having a relatively low elastic modulus." *Id.* (citing '265 patent, col. 9, ll. 50-54). The ALJ added that "the '611 patent describes a single 'dielectric layer' that carries the terminals, *i.e.*, the dielectric layer is the 'top layer' in the '611 patent." *Id.* (citing '611 patent, col. 4, ll. 23-25). Based on those disclosures, the ALJ concluded that "the '106 Patent specification explicitly distinguishes the different layers, *e.g.* 'top layer' and 'elastomeric' layer of the chip carrier," adding that "in both the '611 Patent and the '265 Patent, the term 'layer' refers to a single layer." *Id.*

We disagree with the ALJ's reasoning. Importantly, neither the specification of the '106 patent, the '265 patent, nor the '611 patent include any language indicating that the patentees expressly limited the claim term to a single layer, and the patentees did not explicitly disavow the use of a composite or multi-tiered layer during prosecution of the patent application.[4] Absent

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[4] Respondents argue that Tessera limited the scope of the claim to a single layer when during prosecution of the patent application it stated that "[t]he embodiment of Khandros Fig. 3 does not utilize the step of providing 'a protective barrier in contact with said top layer'" and that Tessera could have amended the claim to include the limitation "in contact with the [multi-layered] interposer layer," but chose not to. Resp Br. at 27-28. Respondents add that "[b]y specifically limiting the amendment to require contact with the single-layer 'top layer,' Tessera disclaimed any construction of 'top layer' as a composite layer." *Id.* We find this argument unpersuasive. Merely amending to state "said top layer" does not expressly disavow a multi-tiered top layer. Indeed, there is some evidence in the specification of the '265 patent that a layer may encompass more than one material. *See* '265 patent, col. 14, ll. 32-34.

clear indication that the patentees intended to limit the scope of the claim term to a single layer, the claim term should not be limited to a single layer. Even if there is no disclosure in the specification showing the top layer as a composite or multi-tiered layer, because nothing in the intrinsic evidence limits the claim term to a single layer, the ALJ incorrectly limited the claim term. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) ("Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope."). Thus, we construe the term "top layer" to mean "a layer disposed on the active side of the chip and which carries the terminals."

We note that our changes to the ALJ's claim construction do not affect his validity and domestic industry analyses.

C. Construction of the Claim Term "Thereon" Recited in Asserted Independent Claim 1 of the '106 Patent

The Commission determined to review the finding that the claim term "thereon" recited in claim 1 of the '106 patent requires "disposing the terminals on the top surface of the top layer," and its effect on the infringement analysis, invalidity analysis and domestic industry analysis.

The ALJ stated that he adopted the ordinary meaning of the claim term "thereon," concluding that construction of the term was unnecessary. ID at 26. In applying the claim term to the accused products, however, the ALJ applied a narrow meaning of the claim term by

requiring the terminals to be "'on or upon'—on the top of—the 'top layer.'" ID at 50. We find that the scope of the claim is broad enough to encompass locating the terminals on other surfaces of the "top layer" other than the top surface, such as on the bottom or side surfaces.

After careful review of the prosecution history of the '106 patent, we disagree with Respondents that it clearly disavows locating terminals on the bottom surface of the top layer under all conditions. Instead, we believe that if the applicants disavowed any subject matter, they disavowed locating terminals on the bottom of the top layer when the terminals are unexposed during encapsulation. This condition, however, does not arise in this investigation because the asserted claims of the '106 patent require exposed terminals. '106 patent, claim 1 ("A method of encapsulating a semiconductor chip assembly having a top layer with an array of **exposed** terminals thereon" (emphasis added)).

Respondents point to remarks made during prosecution of the '106 patent to support their argument that the patent applicants disclaimed locating the terminals on the bottom surface of the claimed "top layer." Response of Elpida Respondents to Tessera's and the IA's Petitions for Review ("Elpida Rep.") at 28-29; Resp Br. at 12. The '106 patent incorporates the '265 patent by reference and thus the '265 patent's disclosure is part of the '106 patent. However, the '265 patent is prior art to the '106 patent, and during prosecution of the '106 patent application, the Patent Office rejected the then-pending claims in light of the '265 patent. The Patent Office based its rejection on the view that the "interposer" described in the '265 patent corresponds to

the "protective barrier" recited in claim 1 of the '106 patent application. *See* '106 Patent Prosecution History (JX-6) June 24, 1996, Office Action. In order to overcome the Patent Office's rejection, the applicants of the '265 patent application amended the then-pending claims to stress that the "interposer" described in the '265 patent and the "protective barrier" of the '106 patent application do not correspond to each other.[5] The applicants added the following remarks:

> In the interview, the alternative embodiment of Khandros (Khandros Fig. 7) and column 14, line 19 – column 15, line 4 was also discussed. As pointed out in the interview, however, this embodiment of Khandros 265 does not involve encapsulation of a semiconductor chip layer which has "a top layer with an array of exposed terminals thereon." Rather, the terminals 148 are disposed on the undersurface of the top layer 138. At the time encapsulation 158 is applied, there are not exposed terminals to be protected. Rather, after application of encapsulant 158, radiant energy source 159 is used to punch holes 160 in top layer 138, thereby exposing the terminals. Clearly, this embodiment of Khandros '265 has no need for . . . "a protective barrier in contact with said top layer."

'106 Patent Prosecution History (JX-6) December 24, 1996 Amendment. According to Respondents, those remarks support their argument that the '106 patent disclaims locating the terminals on the bottom surface of the claimed "top layer." Elpida Rep. at 28-29; Resp Br. at 12. We disagree. Instead, the applicants explained that because the terminals are disposed on the undersurface of the top layer in the '265 patent, they are not exposed during encapsulation and

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[5] Specifically, the amendment required that the "protective barrier" be provided "in contact with [the] top layer." '106 Patent Prosecution History (JX-6) December 24, 1996, Amendment.

that it is after application of the encapsulant that radiant energy is used to punch holes in the top layer to expose the terminals. The applicants thus argued that the '265 patent does not involve encapsulation of a semiconductor chip layer which has "a top layer with an array of exposed terminals thereon," as recited in claim 1 of the '106 patent application. If the applicants disclaimed any subject matter, they disclaimed only locating terminals on the bottom surface of the top layer when the terminals are not exposed during encapsulation.

The doctrine of claim differentiation provides further support for our conclusion. Claim 20, which depends from claim 1, includes the recitation, "wherein said top layer includes a top surface on which the array of terminals is disposed and said barrier includes a dam extending upwardly from said top surface." That is, dependent claim 20 further limits the invention described in independent claim 1 by requiring, *inter alia*, that the array of terminals be located on the top surface of the top layer, indicating that independent claim 1 is not so limited.

Respondents argue that Tessera presents the argument that the terminals are located on the bottom surface of the top layer for the first time in its petition for review and as such the argument is waived. Elpida Rep. at 28-29. Likewise, Tessera argues that Respondents' "disclaimer" argument, which is in response to its argument that the terminals are located on the bottom surface of the top layer, is untimely. Tessera Br. at 24. We, however, believe that Tessera only had the opportunity to present its arguments for the first time in its petition for review. The ALJ decided not to construe the claim term "thereon" and stated that he would

apply its plain and ordinary meaning. Tessera and the IA could have reasonably assumed that their argument was inherent in the plain and ordinary meaning of "thereon." In other words, Tessera and the IA had no reason to make their arguments until they realized what the ALJ meant by "plain and ordinary meaning" of the claim term "thereon." In addition, we believe that the argument was subsumed in Tessera's presentation explaining how the accused products infringe. *See* Tessera's Post-Hearing Brief at 52-53. Similarly, Respondents could not respond until Tessera made its argument, so we consider Respondents' argument.

We note that our changes to the ALJ's claim construction do not affect his validity and domestic industry analyses.

III. INFRINGEMENT

A. Legal Standard

After construing the claims of the patent, a factual determination must be made as to whether the properly construed claims read on the accused devices. *Markman*, 52 F.3d at 976. Literal infringement of a claim occurs when the properly construed claim reads on the accused device exactly, *i.e.,* when every limitation recited in the claim appears in the accused device. *Amhil Enters., Ltd. v. Wawa, Inc.,* 81 F.3d 1554, 1562 (Fed. Cir. 1996). In a section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a "preponderance of the evidence." *Enercon GmbH v. Int'l Trade Comm'n,* 151 F.3d 1376, 1384 (Fed. Cir. 1998).

B. Infringement Analysis of the '106 Patent

The ALJ identified the elastomeric layer in Respondents' accused μBGA packages as the "top layer" and the laminate substrate core in Respondents' accused wBGA packages as the "top layer" because the record evidence showed that those were the layers that the terminals appeared to be "on or upon." ID at 50-51. The ALJ then found that the accused packages met the claimed "a top layer with an array of exposed terminals thereon," namely the "solder ball pads on the substrate core layer in wBGA products and the solder ball pads on the eastomeric layer of the package substrate in the μBGA products." *Id.* The ALJ, however, concluded that the accused packages do not infringe because "the 'protective barrier' never comes into contact with either the core substrate layer or the elastomeric layer." *Id.* at 52. Tessera and the IA dispute the ALJ's identification of "top layer" in the accused packages, and contend that the application of a proper construction of the claim terms "top layer" and "thereon" shows that the polyimide layer with an array of terminals thereon constitutes the "top layer" in the μBGA packages, and the multi-part laminate substrate layer, having the solder mask layer as the outer most layer represents the "top layer" in the wBGA packages.

To support their position, Tessera and the IA primarily rely on the embodiment described in Figure 7 of the '265 patent. *See* Tessera Pet. at 12, 23-24; IA Pet. at 7-8. Tessera emphasizes that the accused "μBGA packages have the exact structure of the interposer/chip carrier described and depicted in the '106 and '265 patents" and that although "like the accused

packages, the terminal is sandwiched between the top layer and the elastomeric layer; it comes in contact with, and can be said to be 'on' both surfaces," the '265 patent identifies the polyimide layer as the top layer. Tessera Pet. at 36. In other words, according to Tessera, although the terminals "can be said to be on both surfaces," the polyimide layer represents the claimed "top layer" because the '265 patent identifies it as such.

Nothing precludes identifying the polyimide layer as the claimed "top layer" in the μBGA packages. Indeed the '106 patent states that "[t]he chip carrier 14 is made up of a top layer 16 (preferably a polyimide layer or the like) and an elastomeric pad 20 disposed between the top layer 16 and the semiconductor chip 12." '106 patent, col. 5, ll. 10-13. That is, the '106 patent itself identifies the polyimide layer as the "top layer" and distinguishes between the "top layer" and the "elastomeric layer," which the ALJ determined was the "top layer." We therefore reverse the ALJ's finding that the polyimide layer cannot represent the claimed "top layer."

The ALJ found that the accused μBGA packages do not infringe because of his finding that the "protective barrier" (the second mold chase) does not come into contact with the top—elastomeric—layer. *See* ID at 51-53. As noted above, we disagree with the ALJ that the elastomeric layer exclusively represents the claimed "top layer." Rather, in our judgment, the polyimide layer may also represent the "top layer." The record evidence shows that the "protective barrier" comes into contact with the polyimide layer. *See* ID at 52 ("In μBGA products, the second mold chase is in contact with the polyimide layer."); RX 323C; RX-9C;

RX-310C; RX-311C. Thus, the μBGA packages meet each limitation of asserted claim 1 of the '106 patent. Nevertheless, the μBGA packages do not infringe because they are exclusively Elpida products (*See* Complainant Tessera Inc.'s Corrected Post-hearing Brief at 50-51) and Elpida established its patent exhaustion defense for all its products. ID at 153 (stating that "the ALJ finds that 100% of Elpida's suppliers were licensed entities").[6]

With respect to the wBGA products, Tessera's theory of infringement requires the claimed "top layer" to include the solder mask layer, either as a single layer or as part of a composite laminate substrate. *See* Tessera Pet. at 32-33. The intrinsic evidence of the '106 patent, however, makes clear that the solder mask layer and the claimed "top layer" are distinct components. For example, the figures of the patent identify the solder mask as component 30

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[6] At this late stage of the investigation, after the Commission has adopted the ALJ's determination with respect to Respondents' affirmative defense of patent exhaustion, Tessera invites the Commission in its brief on the issues of remedy, the public interest and bonding, to reconsider the ALJ's patent exhaustion determination. Complainant Tessera, Inc.'s Corrected Brief on the Issues of Remedy, the Public Interest, and Bonding at 65. Tessera asserts that *Jazz Photo Corporation v. United States International Trade Commission*, 264 F.3d 1094, 1105 (Fed. Cir. 2001) and the Commission opinion on enforcement in *Certain Ink Cartridges and Components Thereof*, Inv. No. 337-TA-565 (Sept. 24, 2009) stand for the proposition that only a "patent exhausting first sale" taking place in the United States can trigger patent exhaustion. *Id.* at 63. The IA appears to support Tessera's assertion, though the IA does not request review. *See* OUII's Reply to Respondents' Responses to Commission Questions at 18-19. Tessera and the IA, however, failed to present this argument to the ALJ during the course of the investigation to give him an opportunity to consider the argument and make appropriate findings. Indeed, Tessera did not even raise this argument in its petition for review to the Commission, and the IA did not even petition the Commission to review the ALJ's patent exhaustion determination. Against this backdrop, we decline Tessera's invitation and find that Tessera has waived the argument. *Broadcom Corp. v. Int'l Trade Comm'n*, 542 F.3d 894, 901 (Fed. Cir. 2008) ("Broadcom has therefore waived that argument by failing to preserve it in the proceedings before the administrative law judge."); 19 C.F.R. § 210.43(b)(2).

and the top layer as component 16. In addition, the patent states that "[p]referably, the solder mask is vacuum laminated to the top layer of the semiconductor chip assembly. More preferably, the solder mask is vacuum laminated not only to the top layer of the semiconductor chip assembly but also to the top side of the encapsulant barrier." '106 patent, col. 2, ll. 35-40. Nowhere does the '106 patent describe or suggest that the top layer includes the solder mask layer. Rather, the patent continually depicts them as separate and distinct components. *See, e.g.*, 106 patent, FIG. 1.

Unasserted claim 22 of the '106 patent, which depends from asserted independent claim 1, provides further support. Claim 22 includes the recitation:

> The method in claim 1, wherein said top layer includes a top surface on which the array of terminals are disposed, said protective barrier includes a sheet like mask [*i.e.*, solder mask layer], and said providing step includes attaching said mask to said top surface of said top layer and to said encapsulant barrier such that said mask extends over said encapsulation area.

In other words, consistent with the specification, claim 22 teaches attaching the solder mask layer to the top layer. The solder mask layer, therefore, cannot be the top layer. Given that the top layer cannot include the solder mask layer, the ALJ correctly concluded that for the wBGA packages, the laminate-based substrate core layer represents the claimed "top layer," and that because the "protective barrier" does not come into contact with that layer, the wBGA packages do not infringe the asserted claims of the '106 patent. ID at 51.

C. Infringement Analysis of the '977 and '627 Patents

We note that determinations reached by the Commission in prior investigations are not binding on subsequent investigations and each investigation must be decided on its own record evidence. *See Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-526, Final Initial and Recommended Determinations (Public Version) at 4-5 (Jan. 17, 2006). There is no doctrine of *stare decisis* in an administrative practice. Notwithstanding, no dispute exists that the testing methodology at issue in this investigation is the same as the testing methodology the Commission reviewed in the 605 Investigation. ID at 4; Order No. 40. Accordingly, we believe that the Commission's opinion regarding that testing methodology, while not binding in this investigation, remains instructive.

As described *supra* at Part I.B., the '977 and '627 patents are drawn to a semiconductor chip assembly that allegedly improves solder joint reliability by reducing the stress and strain on the solder joints caused by mismatched CTEs. The claimed inventions concentrate on the incorporation of a compliant layer into the semiconductor assembly to allow for terminal displacement to appreciably relieve stress caused by external loads. The stress relief on the solder joints improves the reliability of the semiconductor assembly when it is subjected to repeated heating and cooling cycles during operation. The patents do not claim achieving the improvement by matching the effective CTE of the semiconductor package to the CTE of the circuit board. Rather, the patents claim improvement by using movable terminals.

The parties agree that the central dispute is whether the accused products meet the recited "movable terminals" limitations. *See* ID at 54. The ALJ construed the term "movable terminals" to require that "in the operation of the assembly, the terminals are capable of being displaced relative to the central contacts of the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement." *Id.* at 40. The limitation at issue in this investigation, "movable terminals" is the same limitation that was at issue in the 605 Investigation and in both investigations, the ALJ gave the limitation essentially the same construction. The main difference between this investigation and the 605 Investigation is that in the 605 Investigation, the asserted claims as well as the accused products were limited to "face up" packages. The Commission must determine whether the ALJ erred in finding that the methodology employed by Tessera's expert, Dr. Qu, to prove infringement failed to prove infringement.

In the 605 Investigation, the Commission noted that the ALJ criticized Dr. Qu's results because Dr. Qu admitted that chip packages are, in reality, non-linear systems and that his "linearity assumption" is merely an approximation of the packages' behavior. 605 Comm'n Op at 39. The Commission found the ALJ's criticism to be misplaced because Respondents' expert, Dr. Sitaraman, acknowledged the appropriateness of using the linearity assumption to determine displacement due to only external loads in his own modeling of the prior art and an accused package. *Id.* The Commission further noted that Dr. Qu's method of determining displacement

due to only external loads "is inherently logical" and that "[a]ny off-board displacement observed in the accused packages during thermal cycling must be due to internal forces only, as there are no external forces present when the package is off-board." *Id.* The Commission concluded that "[t]herefore, any deviation from the off-board displacement when the package is on-board must be due to the counteracting forces applied by the PCB, which is the very definition of 'external load'" and that "it is completely logical, as confirmed by both Drs. Qu and Sitaraman, to consider this deviation in displacement as an approximation of the external load." *Id.*

We note that Dr. Sitaraman's testimony is not of record in this investigation. Dr. Qu specifically testified that the linearity assumption would only be an accurate reflection of the accused packages if the accused packages were first proven to be linear and that the linearity assumption can provide a good approximation only if the accused packages were slightly non-linear. Qu, Tr. 807:1-14; 603:17-20. Dr. Qu, however, admitted that the accused packages in this investigation were non-linear:

> Q. Dr. Qu, these packages that are accused in this investigation, they are nonlinear, are they not?
>
> A. Yes, I agree they are nonlinear.

Qu, Tr. 539:7-10. Dr. Qu added that:

> [f]or solder, it is a little more complex because the behavior is nonlinear. In other words, when you double the amount of the force, you don't get double the amount of displacement. You get a nonlinear relationship. And not only that, that stress-strain relationship also depends on temperature. So it is not purely linear elastic deformation.

Qu, Tr. at 813:17-21. Dr. Qu did not determine the degree of non-linearity of the accused packages because in his own words it is "rather difficult to estimate the degree of non-linearity of the package assemblies." Qu, Tr. 604:5-15; CX-6486C (Qu. W.S.) Q.453. Due to the difficulty in determining the linearity of the accused packages, Dr. Qu testified that he did not rely on his direct loading methodology to prove infringement:

> Q. Can you tell us what types of methodologies or what different methodologies did you use to analyze the accused products?
>
> A. There are basically two types of methodologies . . . Then in one chapter I presented alternative method. That alternative method used the so-called linearity assumption. Okay? Now, that alternative method, as I discuss in my report is not an exact method because you have used the assumption that a system is linear. If you know the system linearity (sic, nonlinearity) is very weak, then that might be a good assumption. Therefore, the solution might be a good one. But if the nonlinearity is very high, that may not be. So I do not rely my opinion on that alternative methodology.

Qu, Tr. 806:17-807:14. In the 605 Opinion, the Commission found evidence in the expert report submitted by Dr. Qu that he believed that his direct loading testing independently showed infringement. 605 Comm'n Op at 38-39. Such evidence is not present in this investigation.[7] In addition, the expert for Respondents, Dr. Clech, testified that "[s]older is highly non-linear. Solder creeps and its response to loads is time and temperature dependent. Because of the non-

[7] The ALJ excluded all expert reports from being admitted into evidence in this investigation. *See* Prehearing Conf. Tr. 96:4-6.

linearity of the mechanical behavior of solder, applying a force is not equivalent to applying a displacement." RX-946C (Clech Rebuttal W.S.) Q. 253. We find that the record lacks sufficient evidence to show that the direct loading methodology as employed in this investigation proves infringement. The ALJ, therefore, did not err in his finding.

[

] The ALJ found this explanation troubling, stating that "[i]t is difficult to rely on science that is so inexact as to suggest a deviation should be somehow canceled out." ID at 74. In addition, Dr. Clech testified that the "physical and thermal-mechanical properties of solders are highly sensitive to the solder alloy composition." RX-946C (Clech, RWS) at Q. 185. Based on the evidence, the

ALJ concluded that [ ] was not scientifically sound, noting that "Dr. Qu himself testified multiple places that the correct materials properties are important to the accuracy of the model and changing them can have unpredictable results." *Id.* (citing Qu, Tr. 648:7-649:14; 673:7-18; 673:25-674:15; 675:8-21; 683:13-17.). We find nothing wrong with the ALJ's findings. Both experts for Tessera and Respondents testified to the unreliability of the linearity assumption when dealing with materials that are non-linear—as the record evidence indicates the solder material may be. Both experts also testified to the "dramatic effect" that can result in using the wrong material composition in the tested models—as was done here.

Moreover, Dr. Qu admitted that CAE improperly modeled the package substrate and PCB as isotropic, where the x, y and z axes have the same modulus, instead of orthotropic, where the z axis has a different modulus from the x and y axes, as he instructed CAE to do.[8] Dr. Qu explained the importance of correctly modeling the package substrate and PCB as orthotropic, testifying that the package substrate and PCB are reinforced with fiberglass, and as a result, they have different moduli on the x, y and z axes. Qu, Tr. at 573:8-574:13; 577:20-578-4, 833:19-22. Dr. Qu, however, was under the impression that CAE had modeled the substrate and PCB as orthotropic and only became aware of the discrepancy during cross examination at the hearing.

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[8] CAE refers to Computer Aided Engineering Associates, a firm Dr. Qu engaged to model accused packages using Finite Element Analysis ("FEA").

CAE's President, Dr. Veikos, disputes Dr. Qu's assertion and testified that Dr. Qu instructed CAE to model the package substrate and the PCB isotropically. *See* Veikos, Tr. at 2500:14-2501:19.

Qu, Tr. at 576:16-577:20; 836:14-839:11. The ALJ found that "Dr. Qu never investigated, quantified, or even qualitatively analyzed the error because he did not know about the mistake until cross examination" and that "given the precision of these finite element models and the potentially compounding effect of mistakes, it is unclear whether the mistake would make a material difference." ID at 68. The ALJ's misgivings are not misplaced. *See Daubert v. Merrill Dow Pharm., Inc.*, 509 U.S. 579, 594 (1993) (stating that "in the case of a particular scientific technique, the court ordinarily should consider the known or potential rate of error") (citations omitted). The Commission agrees that because Dr. Qu was unaware of the mistake until the hearing, the impact of the mistake on Dr. Qu's analysis is unclear.

Finally, the Commission noted in its 605 opinion that:

> By simulating the external load applied to the packages and applying only this simulated external load to compare the plastic work of the solder joints between a package with a compliant layer and a package without a compliant layer, Dr. Qu successfully demonstrated that the observed increase in the solder reliability in the accused packages as compared to the baseline packages was due to the external load. The only **missing link precluding a finding of infringement** is a showing that the demonstrated stress relief in the solder balls of the accused packages was due to terminal-to-chip displacement caused by the applied external load.
>
> In their attempt to discredit Dr. Qu's testing method, Respondents provide this missing link. The ALJ and Respondents relied on Dr. Sitaraman's exhibit to show that there was little difference in the on-board and off-board terminal-to-chip displacement. RX-3483. As the data that Dr. Sitaraman extracted from Dr. Qu's second testing method shows, however, there is terminal-to-chip displacement in the accused packages when an external load is applied. *Id.* As is clear from the data, there is a difference in the positions of the terminals relative to the chip in the accused

> packages after thermal cycling when the chip is on-board as opposed to when the chip is off-board. This difference in positions is due solely to the external load the PCB is applying to the terminals.

605 Comm's Op at 48-49 (emphasis added). That is, the Commission noted that Dr. Qu's testing omitted a "missing link" necessary for a finding of infringement—a showing that the demonstrated stress relief in the solder balls of the accused packages was due to terminal-to-chip displacement caused by the applied external load. *Id.* The Commission, however, found the missing link in the exhibits presented by Respondents' expert, Dr. Sitaraman. *Id.* As noted, Dr. Sitaraman did not participate in this investigation and the record evidence does not contain evidence consistent with the exhibit that he presented in the 605 Investigation that the Commission found provided the "missing link."

The ALJ correctly concluded that the record evidence shows that Dr. Qu's moiré analysis[9] fails to provide the "missing link" and cannot compensate for the identified mistakes in Dr. Qu's direct loading methodology as respondents argued. ID at 90. The ALJ noted that Dr. Qu's moiré analysis confirmed his FEA to an extent that computer modeling predicted the actual displacements of packages to a reasonable degree of accuracy. *Id.* The ALJ pointed to Dr. Qu's statement that:

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[9] Tessera explains that "[m]oiré is a technique for determining the deformation of a structure using laser pattern analysis. Lasers are projected onto the surface of a structure at rest as a control, then the structure is subjected to conditions that cause deformation and the lasers are re-projected onto the structure surface. Based on the difference in the patterns, the amount and direction of deformation can be compared to the amount and direction of deformation predicted by FEA." Tessera Pet. at 65.

> [m]ost importantly though, moiré results, regardless of how accurate they are or how many packages are tested, cannot by themselves prove infringement. They only show displacement. They do not allow measurement of whether there has been appreciable relief of stress within a particular package, as required by the claims of the asserted '977 and '627 patents.

CX-06486C (Qu DWS) at Q. 405. In other words, as the ALJ correctly noted, "while Dr. Qu's moiré result does not contradict the displacement results of the FEA, it does little to confirm the baseline comparison methodology and does not confirm any claimed movement." ID at 90.

Although Dr. Qu employed the same direct loading methodology in both this investigation and the 605 Investigation, the record evidence of the two investigations compel reaching different results. In particular, due to the uncertainty of the linearity assumption, Dr. Qu testified in this investigation that he did not rely on his direct loading methodology to prove infringement. In addition, [

] Dr. Qu modeled the solder material without copper, which experts for both Tessera and Respondents agree could result in unpredictable results. Moreover, CAE, the lab Dr. Qu employed, modeled the package substrate and PCB as isotropic instead of orthotropic, and Dr. Qu did not become aware of the discrepancy until the hearing. Finally, the "missing link" precluding a finding of infringement that the Commission found present in the 605 Investigation is absent in this investigation. Thus, we affirm the ALJ's finding of no infringement with respect to the asserted claims of the '977 and

'627 patents.

D. Whether the OMPAC Reference Anticipates the Asserted Claims of the '977 and '627 Patents

"Claimed subject matter is 'anticipated' when it is not new; that is, when it was previously known." *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008). 35 U.S.C. § 102(b) provides that a person shall be entitled to a patent unless "the invention was . . . in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States."

We find that the ALJ erred by relying on the "1990 date of invention" of the asserted claims of the '977 patent. *See* ID at 117. The on-sale bar provision of 35 U.S.C. § 102(b) provides that sales made "more than one year prior to the date of the application" qualify as prior art. In other words, the "date of invention" has no bearing on this analysis. It is instead the earliest effective filing date of the patent that is important. Notwithstanding, the ALJ did not err in his finding that Respondents failed to show by clear and convincing evidence that the 1989 Motorola OMPAC 68-pin chip package ("OMPAC") anticipates under the section 102(b) on-sale bar. The record evidence supports the ALJ's finding that the OMPAC package was an experimental prototype and the "sale" from Citizen Watch to Motorola was subject to a confidentiality agreement. *Id.* at 118.

The ALJ stated that the evidence shows that Motorola contacted Citizen Watch in Japan

about producing "engineering samples" or "prototypes" of a package with characteristics that were specified by Motorola, and that Citizen Watch was subject to a confidentiality agreement with Motorola which precluded it from selling the engineering samples to any other company, or otherwise disclosing any information regarding the OMPAC to any entity but Motorola. *Id.* (citing CX-7349C (Ivey, Direct) Q. 255; CX-07355C (Urbish, Direct) Q. 38; Freyman, Tr. 1669:16-25, 1670: 1-11, 1676:13-15, 1678:8-13). The ALJ thus concluded that the sale to Motorola was for experimental purposes and did not constitute a commercial sale that would trigger the on-sale bar provision of section 102(b). ID at 118 (citing *Manville Sales Corp. v. Paramount Sys., Inc.*, 917 F.2d 544, 550 (Fed. Cir. 1990) (stating that "a sale that is primarily for experimental purposes, as opposed to commercial exploitation, does not raise an on sale bar")).

We agree with the ALJ's finding. We, however, modify the ALJ's decision to clarify that the "invention date" of the patent has no bearing on the section 102(b) on-sale bar analysis. Rather, the operative date is the earliest effective filing date.

VIII. CONCLUSION

For the reasons set forth above, we (1) modify the ALJ's construction of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent; (2) reverse the ALJ's finding that the accused μBGA products do not meet all of the limitations of the asserted claims of the '106 patent but affirm his finding that there is no infringement due to patent exhaustion for the Elpida products; (3) affirm the ALJ's finding that the accused wBGA products do not infringe the

asserted claims of the '106 patent; (4) affirm the ALJ's validity and domestic industry analyses pertaining to the asserted claims of the '106 patent; (5) affirm the ALJ's finding that the Direct Loading testing methodology employed by Complainant's expert fails to prove infringement; and (6) affirm the ALJ's finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent under the on-sale bar provision of 35 U.S.C. § 102(b), but modify a portion of the ID. Nevertheless, we affirm his determination that Respondents did not violate section 337.

By order of the Commission.

Marilyn R. Abbott
Secretary to the Commission

Issued: February 24, 2010

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **COMMISSION OPINION** has been served by hand upon the Commission Investigative Attorney, Kecia J. Reynolds, Esq., and the following parties as indicated, on February 24, 2010.

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
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