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Paper 27
Entered: December 27, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD., FUNAI ELECTRIC CO., LTD., and TOSHIBA CORP.,
Petitioner,

v.

GOLD CHARM LTD.,
Patent Owner.

Case IPR2015-01417
Patent 5,966,589

Before KARL D. EASTHOM, MICHAEL R. ZECHER, and BRYAN F. MOORE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

I. INTRODUCTION

Petitioner, Samsung Display Co., Ltd., Funai Electric Co., Ltd., and Toshiba Corp. (collectively, "Petitioner") filed a Petition requesting an *inter partes* review of claims 2–6[1] of U.S. Patent No. 5,966,589 (Ex. 1001, "the '589 patent"). Paper 1 ("Pet."). In response, Patent Owner, Gold Charm Limited, filed a Preliminary Response. Paper 8 ("Prelim. Resp."). On December 28, 2015, we instituted an *inter partes* review of claims 2, 3, 5, and 6 on the following grounds alleged in the Petition:

Claims	Basis	References
3, 5, and 6	§ 102	Takizawa
2	§ 103	Takizawa and Hoshino
2, 3, and 6	§ 102	Hoshino

Paper 12, 34 ("Institution Decision" or "Dec. on Inst.").[2] Patent Owner filed a Patent Owner Response. Paper 18 ("PO Resp."). Petitioner filed a Reply. Paper 21 ("Pet. Reply"). The parties filed additional authorized briefing

[1] Claim 1 has been disclaimed by Patent Owner. Ex. 1011; Prelim. Resp. 32–33 n.10 (confirming that Patent Owner disclaimed claim 1). The parties did not argue that the limitations of claim 1 are dedicated to the public such that they do not need to be shown separately in a prior art reference for the purpose of anticipating or rendering obvious claims 2, 3, 5, and 6, each of which depend directly from claim 1. We decline to decide that issue as we find that all the limitations of claim 1 are met by the prior art.

[2] Prior to the Patent Owner Response, Petitioner filed a Patent Owner's Request for Rehearing (Paper 14, "Reh'g Req.") challenging the Institution Decision, and we responded with a Decision Denying Petitioner's Request for Rehearing (Paper 17, "Reh'g Dec.").

sought by Patent Owner to address a real party in interest issue. *See* Papers 7, 9–11. The record includes a transcript of the Oral Hearing that occurred on September 27, 2016. Paper 26 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision issues pursuant to 35 U.S.C. § 318(a). For the reasons discussed below, we hold that Petitioner has shown by a preponderance of the evidence that claims 2, 3, 5, and 6 of the '589 patent are unpatentable.

A. Related Matter

The '589 patent is involved in the following lawsuits: (1) *MiiCs & Partners, America, Inc., v. Toshiba Corp.*, No. 1:14-cv-00803-RGA (D. Del.); (2) *MiiCs & Partners, America, Inc., v. Funai Electric Co.*, No. 1:14-cv-00804-RGA (D. Del.); and (3) *MiiCs & Partners, America, Inc., v. Mitsubishi Electric Corp.*, No. 1:14-cv-00805-RGA (D. Del.) (dismissed on July 7, 2015). Pet. 1–2; Paper 5, 2–3. Petitioner also filed additional petitions challenging certain subset of claims in other patents owned by Patent Owner.

B. The '589 Patent

The '589 patent relates to a method of fabricating a thin film transistor ("TFT") array that has various layers of metals, insulators, semiconductor materials, and other materials in a stacked relationship with different layers having different patterns and a number of various conductive connections between certain layers and not others. Ex. 1001, Abstract, 1:10–44, Figs. 4–6, 8–10. The Specification describes forming the requisite patterns in the various layers using photolithography, etching, and other methods. *Id*. at Figs. 7A–7N. The Specification describes a method that fabricates a thin

film transistor with a high fabrication efficiency with a reduction of photolithography steps. *Id.* at 2:56–62. Additionally, the Specification states that because the method "does not employ lift-off unlike the conventional methods, debris caused by lift-off is not generated." *Id.* at 4:6–8.

C. Illustrative Claim

Disclaimed claim 1 (*see supra* note 1) is not challenged, but is the only independent claim related to the instituted claims. Instituted claims 2, 3, 5, and 6 depend directly from claim 1.

Claims 1 and 2, reproduced below, are illustrative.

> 1. A method of fabricating a thin film transistor array comprising a transparent insulating substrate, a plurality of thin film transistors formed on said substrate in a matrix, a gate bus line connected to gate electrodes of said thin film transistors, a drain bus line connected to drain electrodes of said thin film transistors, and a pixel electrode driven by said thin film transistors, said method comprising the steps of:
>
> (a) forming said gate electrodes and said gate bus line on said transparent insulating substrate;
>
> (b) forming a gate insulating film over said substrate;
>
> (c) forming an operative semiconductor on said gate insulating film;
>
> (d) forming source electrodes, said drain electrodes, and said drain bus line of said thin film transistors on said gate insulating film and said operative semiconductor;
>
> (e) forming a protection film over said substrate;

> (f) removing a portion of both said gate insulating film and said protection film, located above a terminal of said gate bus line, and removing a portion of said protection film located above a terminal of said drain bus line; and
>
> (g) forming said pixel electrode on said substrate.

Ex. 1001, 10:19–41.

> 2. The method as set forth in claim 1, wherein said thin film transistor array further comprising an auxiliary capacitive bus line formed on said substrate in facing relation to said pixel electrode with said gate insulating film therebetween, and wherein a portion of both said gate insulating film and said protection film, located above a terminal of said auxiliary capacitive bus line, is also removed in said step (f).

Id. at 10:42–49.

D. Evidence of Record

Petitioner relies upon the following prior art references:

Takizawa	US 5,483,082	Jan. 9, 1996	(Ex. 1003)
Hoshino	JP H6-102528	Apr. 15, 1994	(Ex. 1004[3])
Shin	US 5,825,449	Oct. 20, 1998	(Ex. 1006)

Petitioner also relies on the Declaration of Dr. Anne Chiang (Ex. 1012, "Chiang Declaration"). Patent Owner relies on the Declaration of Dr. Michael P.C. Watts. (Ex. 2025, "Watts Declaration").

[3] Exhibit 1005 is a certified translation of Hoshino.

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1281–82 (Fed. Cir. 2015); *aff'd sub nom. Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard in an *inter partes* review proceeding). Under the broadest reasonable interpretation standard, claim terms are generally given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art, in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

For the purposes of this Final Written Decision, and on this record, most of the claim terms do not require an express construction. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999) (only those terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy).

1. number of photolithography steps

Petitioner asserts that "[t]here is no express limitation on the number of photolithography steps allowed in the claims." Pet. 8. Thus, Petitioner implicitly construes the claims as not requiring any specific number of photolithography steps. *Id.* In its Preliminary Response, Patent Owner asserts that "[t]he broadest reasonable construction of the claimed methods

of the [']589 patent requires that the methods are limited with respect to the formation of the TFT array to no more than the five discretely recited photolithography/etching steps (a), (c), (d), (f) and (g) of claim 1." Prelim. Resp. 35. We determined on the preliminary record that the claims are not limited to a specific number of photolithography steps, as argued by Patent Owner. Dec. on Inst. 15–18. We see no reason to alter the construction of this proposed limitation as set forth in the Institution Decision as recited above.

In its Patent Owner Response, Patent Owner once again asserts that "[t]he broadest reasonable construction of the methods of the challenged claims of the '589 patent requires that the methods are limited with respect to the formation of the TFT array to no more than the five discretely recited patterning/etching steps (a), (c), (d), (f) and (g) of claim 1." PO Resp. 23–24 (citing Ex. 1001, 3:66–4:7).[4] Patent Owner argues: "The Board's construction ignores the express statements of the inventors that: 'the method as defined in claim 1 need[s] to carry out only five photolithography steps.'" *Id.* at 24 (quoting Ex. 1001, 4:1–2). Petitioner argues that this statement is a clear and unmistakable disavowal that constitutes a disclaimer. *Id.* We disagree.

The Specification consistently states that the reduction of

[4] Patent Owner also argues that the claims exclude the use of a lift-off procedure. PO Resp. 24. As explained *infra*, lift-off is only arguably relevant to the motivation to combine the Takizawa and Hoshino references. Thus, we decline to determine whether the claims exclude a lift-off procedure.

photolithography steps is the purpose of the invention:

> It was necessary to carry out six photolithography steps in order to fabricate the conventional TFT. In contrast, in accordance with the above-mentioned first embodiment, TFT may be completed by carrying out only five photolithography steps, which is smaller in the number of photolithography steps than the conventional method by one.

Ex. 1001, 7:8–13. This theme is repeated several times in other statements in the Specification. *See generally* Ex. 1001, Abstract, 2:56–61, 3:66–4:8.

The transition "comprising" in a method claim indicates that the claim is open-ended and allows for additional steps. *See Vivid Techs.*, 200 F.3d at 811 (citing *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1271, (Fed. Cir. 1986)). That is, "comprising" means that the device may contain elements in addition to those explicitly mentioned in the claim. *See CIAS, Inc. v. Alliance Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007).

Patent Owner acknowledges that claim 1 employs the transitional phrase "comprising" before reciting the claimed method steps. PO Resp. 33. Patent Owner asserts, however, that in light of the above statements "the Board's preliminary determination as to what is or is not excluded from the claims is unreasonable in light of the specification[,] as it would be understood by one of ordinary skill in the art at the time of the invention." *Id.* at 25. Notwithstanding Patent Owner's reliance on the statement in the Specification noted above (PO Resp. 24 (quoting Ex. 1001, 4:1–2)), in at least one other place, it uses permissive language stating the first

embodiment "*may* be completed by carrying out only five photolithography steps." Ex. 1001, 7:8–13 (emphasis added).[5]

Patent Owner also suggests that the word "comprising" was used to allow unclaimed pre-processing steps to be considered within the scope of the claim. PO Resp. 33. However, because the Patent Owner does not cite sufficient evidence of a discussion of the pre-processing steps in the Specification, in our view, Patent Owner is merely speculating that the existence of pre-processing steps was a reason the claim drafter chose to use the transitional phrase "comprising."[6]

The term photolithography is not recited explicitly in the claims. Rather, the claims refer generically to "forming" steps which may or may not include photolithography. As discussed above, the Specification, in some places, does have language suggesting that the claims are practiced using only five photolithography steps in comparison to "conventional methods." For instance, the Specification discloses that the "method as defined in claim 1 need[s] to carry out only five photolithography steps."

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[5] Patent Owner cites to decision by the U.S. Court of Appeals for the Federal Circuit in *Retractable Technologies* for the proposition that permissive language can be trumped by distinguishing prior art. PO Resp. 31 (citing *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011)). However, *Retractable Technologies* does not discuss the effect of permissive language when combined with the open ended transitional phrase "comprising."

[6] Furthermore, Patent Owner's argument appears to relate to another possible, but not recited, transitional phrase, the phrase "consisting essentially of."

(Ex. 1001 4:1–2), and the "above-mentioned method needs to carry out only five photolithography steps" (*id.* at Abstract).

The Federal Circuit "counsels the PTO to avoid the temptation to limit broad claim terms solely on the basis of specification passages." *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). "Absent claim language carrying a narrow meaning, the PTO should only limit the claim based on the specification or prosecution history when those sources expressly disclaim the broader definition." *Id.* Additionally, "'words or expressions of manifest exclusion' or 'explicit' disclaimers in the specification are necessary to disavow claim scope." *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1374 (Fed. Cir. 2005).

Patent Owner cites to the recent *Cutsforth* decision from the Federal Circuit for the proposition that the Board's construction "must be reasonable in light of the specification." PO Resp. 26 (quoting *Cutsforth, Inc. v. Motivepower, Inc.*, 643 F. App'x. 1008, 1010 (Fed. Cir. 2016) (non-precedential)). Additionally, Patent Owner cites the *O.I. Corp.* decision for the proposition that "expressly distinguishing the invention from the prior art in the specification would lead one of ordinary skill in the art to conclude, upon reading the specification, that the claims exclude the prior art from which the invention has been distinguished." *Id.* at 27 (citing *O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1581 (Fed. Cir. 1997)).

We note that in *Gillette* the claims specifically recited a three blade razor and the specification distinguished two blade razors from razors with more than two blades; however, the court did not limit the claims to three blades. *Gillette*, 405 F.3d at 1371. The *Gillette* court also relied on

language in the specification that stated that the invention related to a "plurality" of blades as language permitting more than three blades. *Id.* at 1373–74. As to Patent Owner's citations, *O.I. Corp.* did not discuss explicitly the effect of the transitional phrase "comprising" on the construction of the claim. *O.I. Corp.*, 115 F.3d at 1581. Additionally, the *Cutsforth* decision is distinguishable because it is directed to whether the construction of a term explicitly recited in the claims was too broad given the disclosure in specification. *Cutsforth*, 643 Fed. App'x. at 1010. Here, Patent Owner is asserting the existence of a disclaimer of a feature which is not explicitly in the claims. Finally, Patent Owner does not cite a case in which claims using the transitional phrase "comprising" are limited to the number of steps performed to those in the claims.

Another citation in the Specification points out that "it is an object of the present invention to . . . [reduce] the number of photolithography steps." *Id*., 2:56–61. Additionally, the Specification states that the elimination of a lift–off procedure is a separate advantage of the invention over "conventional" methods. Ex. 1001, 4:5–8 ("Since the method in accordance with the present invention does not employ lift-off unlike the conventional methods, debris caused by lift-off is not generated."). The Federal Circuit has explained that "[t]he characterization of a feature as 'an object' or 'another object,' or even as a 'principal object,' will not always rise to the level of disclaimer." *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015). "The fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the

objectives." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 908 (Fed. Cir. 2004). Here, the '589 patent mentions elimination of lift-off and reduction of photolithography steps as separate objectives of the invention. Ex. 1001, 2:56–61, 4:5–8. Therefore, one could realize a benefit of eliminating a lift-off procedure even if more than five photolithography steps are used.

Overall, the statements in the Specification are not consistent in stating that no more than five photolithography steps must be performed according to the invention and suggests that the formation of a transistor array using only five photolithography steps is one of two possible benefits of using the methods described in the Specification. The open-ended claim term "comprising" plainly contradicts any implied five step limit that the Specification indicates "*may* be" employed in a "first embodiment" as an option. *See* Ex. 1001, 7:10–11. Thus, we maintain our initial determination that the claims are not limited to a specific number of photolithography steps, which, in our view, is a broad, yet reasonable construction in light of the Specification and claims of the '589 patent.

2. order of photolithography steps

Patent Owner also argues that steps (c) and (d) of claim 1 must be performed in the same order as recited in the claim. PO Resp. 20. Patent Owner suggests that the structure of the thin film transistor described in the Specification must be achieved by the claims. *Id.* at 18–20.[7] Patent Owner

[7] We note that the claims are not product-by-process claims and do not claim a final article, but rather a series of manufacturing steps. *See* Tr. 21:23–22:2

also suggests Petitioner's Declarant, Dr. Chiang, agrees because she answers "Very important" to the following question: "Is the structure of the TFT that's formed by a fabrication process important?" PO Resp. 19–20 (quoting Ex. 2024, 35–36).

Whether the order of the steps recited in a method claim must be performed in a particular order is properly a part of claim construction. *See, e.g.*, *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371–72 (Fed. Cir. 2003). Generally, steps may be performed in any order so long as "nothing in the intrinsic evidence" compels otherwise. *Id.* at 1370. "*Interactive Gift* recites a two-part test for determining if the steps of a method claim that do not otherwise recite an order, must nonetheless be performed in the order in which they are written." *Altiris*, 318 F.3d 1369 (citing *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342–43 (Fed. Cir. 2001)). "First, we look to the claim language to determine if, as a matter of logic or grammar, they must be performed in the order written." *Id.* "If not, we next look to the rest of the specification to determine whether *it* directly or implicitly requires such a narrow construction." *Id.* at 1370. (citation omitted). If not, the sequence in which such steps are written is not a requirement.

([Counsel for Patent Owner: the challenged claims] are not product-by-process claims. They are method claims, methods of forming TFTs. Our position is that the claimed methods, *as recited*, form a particular structure. And that is a back-channel etched TFT, not an etch stop TFT." (emphasis added)).

The instituted claims require, among other things, the following two steps: "(c) forming an operative semiconductor on said gate insulating film"; and "(d) forming source electrodes, said drain electrodes, and said drain bus lines of said thin film transistors on said gate insulating film and said operative semiconductor." Ex. 1001, 10:29–33. The broadest reasonable interpretation of these words does not require explicitly that the operative semiconductor is formed before step (d), but rather that the source, drain, and bus lines are formed "on" the operative semiconductor.

Patent Owner suggests that the "island" 21 formed as shown in Figure 7F of the Specification is the separate and distinct forming of the operative semiconductor. PO Resp. 36, 43. Assuming this is true, Patent Owner does not point to language in the Specification clearly limiting the claims to the formation of "island" 21. Additionally, Petitioner argues that the operative semiconductor is not "formed" fully until the etch that forms the source and drain is performed. Pet. Reply 9–13.

The claim does not contain the words such as "before" or "after" to indicate an order of the steps. The claim also does not contain words such as "separate" or "distinct" to indicate that the steps must not occur concurrently. Petitioner asserts—and we agree—that the source, drain, and bus lines could be formed concurrently on the operative semiconductor, if there is a forming step that causes the source, drain, and bus lines to be "on," or above, the location of the operative semiconductor. Pet. Reply 8–9. "[O]rdinarily in process claims steps taken concurrently are the equivalent of steps taken successively." *In re White*, 39 F.2d 974, 975 (C.C.P.A. 1930); *see also Cybersettle, Inc. v. Nat'l Arbitration Forum, Inc.*, 243 F. App'x.

603, 609 (Fed. Cir. 2007) (finding "the step of calculating the differences between demands and offers can occur concurrently with the [next enumerated step of] receipt of multiple demands and offers").

Finally, as noted above, Patent Owner relies on the testimony of both party's Declarants to show that the back-channel etch type TFT is required by the claims. Nevertheless, Patent Owner does not cite to any limitation to a back-channel etch in the claims. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that limitations not appearing in the claims cannot be relied upon for patentability). Nor does the Patent Owner point to any disclaimer in the Specification limiting the claims to a back-channel etch. *See Bigio*, 381 F.3d at 1325.

For the reasons above, we determine that the claims are not limited to a specific order of photolithography steps as argued by Patent Owner. Specifically, we determine that steps (c) and (d) recited in claim 1 can be performed concurrently.

B. Principles of Law

Anticipation requires the disclosure in a single prior art reference of each and every element of the claimed invention, arranged as recited in the claim. *Lindemann Maschinenfabrik GmbH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406

(2007). The question of obviousness is resolved on the basis of four underlying factual determinations: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

The level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). We analyze the asserted grounds of patentability with these principles in mind.

C. Anticipation of Claims by Takizawa

Petitioner asserts that claims 3, 5, and 6 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Takizawa. Pet. 17. As noted, claim 1 has been statutorily disclaimed (*supra* note 1, Ex. 1011, Prelim. Resp. 32–33 n.10); however, the remaining instituted claims depend directly from, and contain the limitations of, claim 1. To support its contentions, Petitioner provides detailed explanations as to how Takizawa purportedly meets each claim limitation. *Id.* at 17–27. Petitioner also relies upon the Declaration of Dr. Chiang, who has been retained as a declarant by Petitioner for the instant proceeding. Ex. 1012.

Takizawa discloses insulating film 14 is deposited across the surface substrate in a first step, and then on insulating film 14, amorphous-silicon (a-Si) layer 16 is deposited followed by formation of protecting film 18. Ex. 1003, 15:1–11. After the formation of insulating film 14, a-Si layer 16, and protecting film 18, protecting film 18 is etched so that it remains only above gate electrode 12a to form "the channel protecting film 18a." *Id.* at 15:12–16. Subsequent to the formation of channel protecting film 18a by etching, n+-doped a-Si layer 20 is deposited on the entire surface, followed by deposition of metal film 22. *Id.* at 15:17–20. Then, after depositing a photoresist pattern, metal layer 22, n+-doped a-Si layer 20, and a-Si layer 16 are etched to form source and drain electrodes. *Id.* at 15:21–25.

We agree with and adopt Petitioner's analysis as summarized below. That is, Petitioner contends, and we agree, that Takizawa discloses forming gate electrodes and a gate bus line on a transparent insulating substrate. Pet. 18, 22–23; Ex. 1003 (multiple paragraphs and figures cited in Petition). The present record also supports Petitioner's contention that Takizawa describes forming a gate insulating film over the substrate and forming an operative semiconductor on the gate insulating film. Pet. 18–20, 23; Ex. 1003 (multiple paragraphs and figures cited in Petition). Petitioner further argues, and we agree, that Takizawa discloses forming source electrodes, drain electrodes, and a drain bus line of the TFTs on a gate insulating film and an operative semiconductor, and forming a protection film over the substrate. Pet. 20, 23–24; Ex. 1003 (multiple paragraphs and figures cited in Petition). Petitioner also argues, and we agree, that Takizawa discloses removing a portion of both the gate insulating film and the protection film, located

above a terminal of said gate bus line, and removing a portion of said protection film located above a terminal of said drain bus line and forming the pixel electrode on the substrate. Pet. 20–21, 24–25; Ex. 1003 (multiple paragraphs and figures cited in Petition).

As to claim 3, Petitioner asserts that Takizawa discloses that the gate insulating film is formed to have a multi-layered structure in step (b) of claim 1. Pet. 25 (multiple paragraphs and figures cited in Petition). As to claim 5, Petitioner asserts Takizawa discloses that a portion of said protection film located above said drain and source electrodes is also removed in said step (f) of claim 1. Pet. 26 (multiple paragraphs and figures cited in Petition). As to claim 6, Petitioner asserts that Takizawa discloses that the pixel electrode is formed of indium tin oxide (ITO). Pet. 26 (multiple paragraphs and figures cited in Petition).

Patent Owner asserts Takizawa does not disclose step (c) of claim 1 because an "additional, intervening photolithography step taught by Takizawa is required to form the channel protection film 18a." PO Resp. 48. In order to elucidate this argument, we will review the forming steps (c) and (d) as set forth in the Specification and then the steps (c) and (d) from Takizawa.

In the '589 Specification, in accordance with step (c) of claim 1, an amorphous silicon film 21 containing both a-Si and n+-doped a-Si is deposited over the insulating films by plasma-enhanced chemical vapor deposition; this film is then patterned with photoresist 20b, and thereafter a second patterning/etching step is carried out to form the structure 21 shown in Figure 7F, which serves as the operative semiconductor in the TFT.

Ex. 1001, 5:55–67. Thus, the structure which will be the operative semiconductor portion of the final TFT (corresponding to element 6 in Fig. 4) is formed in a single patterning and etching step from amorphous silicon film 21. Figures 7E and 7F, which show this process, are reproduced below.

FIG. 7E

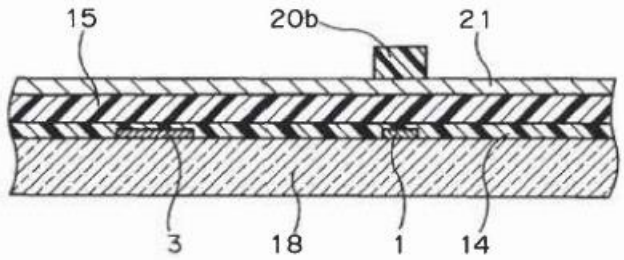
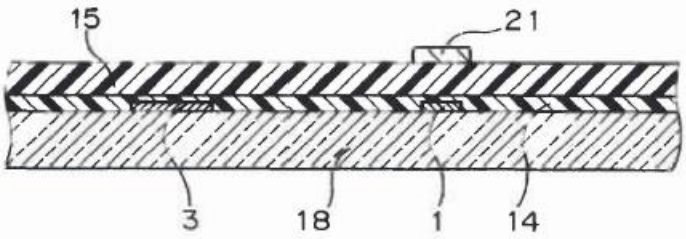


FIG. 7F



Thus, as shown in Figures 7E and 7F above, the structure which will be the operative semiconductor in the final TFT is formed from the amorphous silicon film containing both a-Si and n+-doped a-Si. *Id.*

Next, in accordance with step (d) of claim 1, as shown in Figs. 7G–71, an upper metal layer 22 is deposited over the surface of the array, photoresist 20c is then deposited in a desired pattern, followed by a third patterning/etching step whereby source electrode 7, drain bus line/drain electrode 8 and drain terminal 9 are formed, and a portion of the n+ doped a-Si film between the source and drain electrode is removed. Ex. 1001 at 6: 1–18. Figures 7G, 7H, and 7I, which show this process, are reproduced below.

FIG. 7G

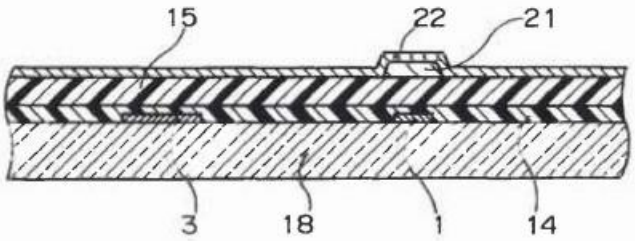


FIG. 7H

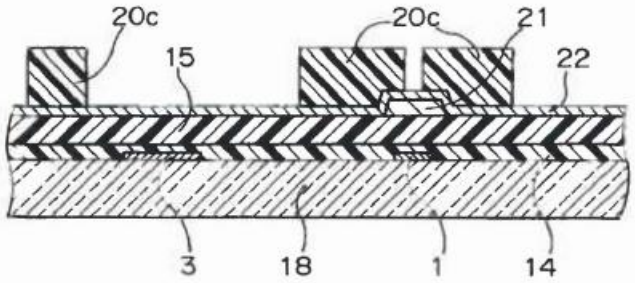
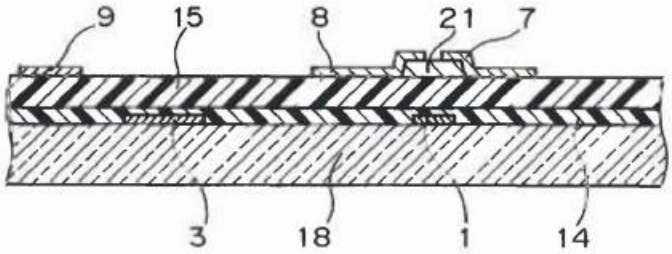
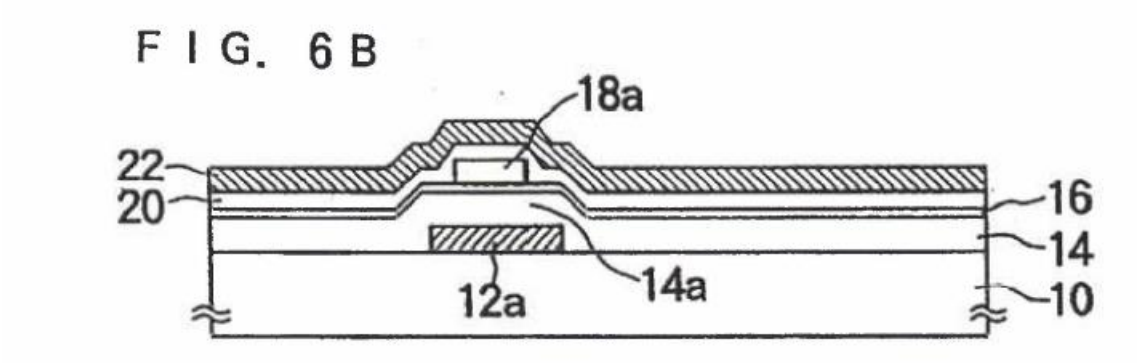


FIG. 7I

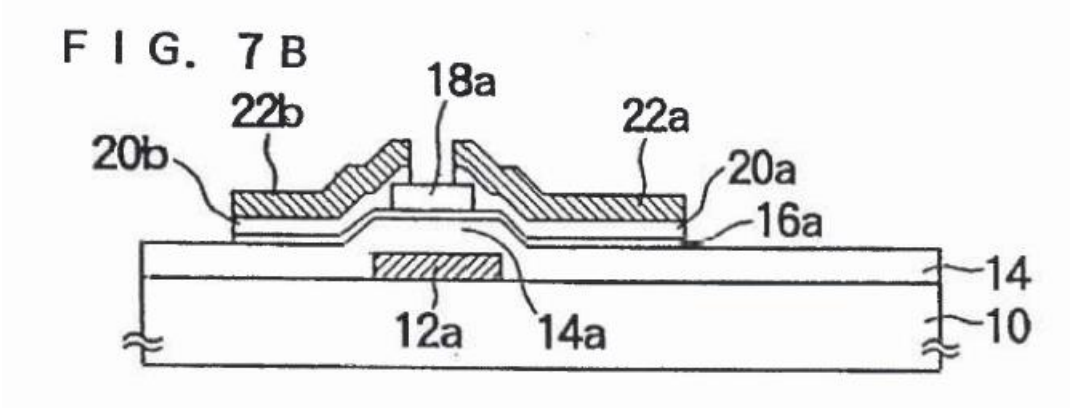


Thus, as shown in Figures 7G, 7H, and 7I above, a distinct patterning and etching step is performed to form the recited structures/elements, i.e., the source electrode, drain bus line, drain electrode and drain terminal. Ex. 1001, 6:1–19.

In comparison, in Takizawa the following structure exists prior to the formation of the source and drain electrodes (Ex. 1003, 15:17–20), as shown in Figure 6B reproduced below.



After the state shown above in Figure 6B, a photoresist pattern is deposited, and then the metal layer 22, the n+-doped a-Si layer 20, and the a-Si layer 16 are "sequentially etched" to form source and drain electrodes, as shown below in Figure 7B of Takizawa. *Id.* at 15:21–25.



As shown in Figure 7B above, the operative semiconductor of Takizawa includes elements 16a, 20a and 20b. Ex. 2024 at 74:3–24. These elements (20a and 20b) are formed after the metal layer 22 is deposited on top of the n +-doped a-Si layer 20. *Id.* Thus, in contrast to the embodiment described in the '589 patent, Takizawa forms its source and drain (22b and 22a) in the same step that forms the operative semiconductor (16a, 20a, and 20b).

Takizawa does require forming an etch-stop (or channel protection layer, referred to as "the protecting film 18" in Takizawa) prior to (and as a necessary prerequisite to) forming the operative semiconductor of the TFT. Ex. 1003 at 15:1–32. However, Takizawa still performs only five patterning steps. In fact, Patent Owner admits that Takizawa performs only five etching/patterning steps. Tr. 40:23–41:9 ("there are five steps in Takizawa"); Ex. 2025 ¶ 49. Patent Owner suggests that to meet the claims limitations, step (c) must be performed before, in a separate and distinct manner from step (d). PO Resp. 47–48.

Petitioner states that, although Takizawa may not perform step (c) of claim 1 before step (d), this claim do not require a specific order of steps. Pet. Reply 16. Patent Owner's argument is premised on construing claim 1 to require performing step (c) of the claim before step (d). As we explained above in the claim construction section, we did not so limit this claim; thus, we are not persuaded by Patent Owner's argument. *See supra* Section II.A.2.

Patent Owner does not address separately Petitioner's contentions and supporting evidence with respect to claims 3, 5, and 6. *See generally* PO Resp. 47–48. We have reviewed Petitioner's proposed ground of anticipation by Takizawa against claims 3, 5, and 6, and we agree with and adopt Petitioner's analysis. Based on the record developed during trial, Petitioner has shown by a preponderance of the evidence that Takizawa anticipates claims 3, 5, and 6.

D. Obviousness of Claims over Takizawa and Hoshino

Petitioner asserts that claim 2 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Takizawa and Hoshino.[8] Pet. 27. To support its contentions, Petitioner provides detailed explanations as to how this proffered combination purportedly meets each claim limitation. *Id.* at 27–31. Petitioner also relies upon a Declaration of Dr. Chiang, who has been retained as a declarant by Petitioner for the instant proceeding. Ex. 1012.

Hoshino discloses methods for fabricating a TFT matrix device. Hoshino teaches two alternative embodiments. In both embodiments, Hoshino teaches first etching gate bus lines, and then etching gate electrodes. Ex. 1005 ¶¶ 24–25, 40–41. Hoshino discloses both a terminal for the auxiliary capacitive bus line ("ACBL") and removal of films from above the ACBL terminal and gate line terminals in the same process step. *Id*. ¶¶ 40, 47–49, Figs. (o), (m), (q).

Claim 2 requires:

> an auxiliary capacitive bus line formed on said substrate in facing relation to said pixel electrode with said gate insulating film therebetween, and wherein a portion of both said gate insulating film and said protection film, located above a terminal of said auxiliary capacitive bus line, is also removed in said step (f).

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[8] Petitioner asserts that "[a person of ordinary skill in the art] would understand that implementation of the method taught by Takizawa would utilize a terminal at the end of the Cs electrode line (the ACBL), even though Takizawa may not expressly describe one." Pet. 27 (citing Ex. 1012 ¶ 67). Nevertheless, Petitioner does not formally present a ground of obviousness over Takizawa alone and we did not institute on such a ground.

Ex. 1001, 10:42–49. We agree with and adopt Petitioner's analysis that Hoshino describes such an auxiliary capacitive bus line. Pet. 27–31; Ex. 1005 ¶¶ 40, 47–49, Figs. (o), (m), (q).

Patent Owner argues that the combination of Takizawa and Hoshino would result in additional photolithography steps beyond the five allowed by the claims, and that Hoshino does not perform steps (c) and (d) separately and distinctly, as Patent Owner asserts is the order required by the claims. PO Resp. 49–50. As we explain in our claim construction section above, we do not construe the claims as limited to five photolithography steps nor do we require the steps to be performed in order or non-concurrently, thus, we are not persuaded by this argument. *See supra* Section II.A.1–2. Additionally, we note that Patent Owner does not argue that step (f) would require more photolithography steps if Hoshino and Takizawa were combined. *See* PO Resp. 51–56.

Petitioner concludes that one of ordinary skill in the art would have recognized that

> the TFT array operates best when the ACBL receives a consistent voltage, which is provided by driving circuitry through the ACBL terminal. Thus, to create a properly operating device, [a person of ordinary skill in the art] would seek out methods of providing a reference voltage to the capacitive electrodes and would incorporate the ACBL terminal of Hoshino into the Takizawa device in order to do so.

Pet. 29; Ex. 1012 ¶ 70. We agree and adopt this stated rationale because it provides specific motivation to make the combination. We credit Petitioner's declarant who testifies that "the [a person of ordinary skill in the art] would know how to etch the ACBL contact hole and gate bus line

contact hole in the same photolithography step because Hoshino provides an example of doing so." Ex. 1012 ¶ 70. Hoshino itself provides the "how" to achieve the claims limitation.

Patent Owner argues that combining Takizawa and Hoshino as a whole would be "impossible." PO Resp. 54–56. Petitioner, however, only adds Hoshino specifically to meet the limitation to a capacitive bus line as part of forming step (f), rather than to combine the processes of Takizawa and Hoshino, as a whole. Pet. 29; Ex. 1012 ¶ 70; Pet. Reply 22–23. Thus, we do not agree with Patent Owner argument that the combination of Takizawa and Hoshino would require more than the five patterning steps disclosed in Takizawa.[9]

Patent Owner also argues that, "[d]espite Petitioners' efforts to insist so, the capacitive electrodes of Takizawa do not necessarily equate to the ACBL of the '589 patent, and the mere mention of capacitive electrodes does NOT necessitate the presence of ACBL *terminals* as in the '589 patent." PO Resp. 39. Although Petitioner argues that Takizawa alone discloses ACBL terminals (Pet. 27–28), our Institution Decision relies only on Petitioner's contentions regarding the combination of Takizawa and Hoshino (*see* Dec. on Inst. 25–26, 34 (instituting, as to claim 2, only the

[9] We note that we determine that claims 3, 5, and 6 are anticipated by Takizawa, which performs five lithography steps, and we determine that claim 2 would have been obvious over the combination of Takizawa and Hoshino, which teaches performing only five lithography steps. Thus, we do not rely on the construction of the number of photolithography steps claimed in determining the patentability of the instituted claims.

combination of Takizawa and Hoshino)). As we noted in our Institution Decision, because Hoshino discloses ACBL terminals (Ex. 1005 ¶¶ 40, 47–49, Figs. (o), (m), (q)), and Patent Owner does not argue that this is not the case, Patent Owner's argument regarding whether Takizawa alone discloses ACBL terminals is meritless.

Patent Owner also argues that one of ordinary skill in the art would have had no reason to combine Hoshino with Takizawa because they have contradictory teachings. According to Patent Owner,

> [r]egarding the contradictory structures of Takizawa and Hoshino, it is clear that Takizawa discloses a pixel electrode 34a above the passivation layer 30. (Ex. 1003 at 15:42-16:9 & Fig. 11C). Takizawa specifically addresses the issue of storage capacitor electrode/pixel electrode shorting by forming the pixel electrode above a passivation layer to introduce additional insulation between the two electrodes. (Ex. 1003 at 4:18-24). Takizawa depicts the problem as it existed in the prior art where the pixel electrode 68a was disposed below the passivation layer 70 and separated from the capacitive electrode 52b by a single insulation layer 54. (Ex. 1003 at 3:9-26 & Fig. 28C). Hoshino teaches exactly what Takizawa specifically seeks to avoid - formation of the pixel electrode 21 below the passivation layer 12. (Ex. 1005 at Fig. 4(1); Ex. 2025 at ¶ 52). One of ordinary skill in the art would have no reason to modify Takizawa with Hoshino, by trying to combine the disparate processes, in view of such directly contradictory teachings. (Ex. 2025 at ¶ 73).

PO Resp. 52–53. The proper test for teaching away is whether or not the reference in question teaches away from the claimed invention, not the reference(s) with which it is combined. *See In re Gurley*, 27 F.3d 551, 553 (Fed.Cir.1994) ("[I]n general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely

to be productive of the result sought by the applicant.")

We also agree with our colleagues that

> [t]here is no requirement that anything disclosed in a prior art reference, such as its stated purpose, goal, or objectives, must be preserved or further developed by every reliance on its teachings as prior art. All of the disclosures of a prior art reference, including non-preferred embodiments, must be considered.

Garmin Int'l v. Cuozzo Speed Techs., LLC, Case IPR2012-00001, slip op. at 36 (PTAB Nov. 13, 2013) (Paper 59) (*citing In re Lamberti*, 545 F.2d 747, 750 (CCPA 1976)) (aff'd by *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131 (2016)); *see also Nat'l Steel Car, Ltd. v. Canadian Pac. Ry., Ltd.*, 357 F.3d 1319, 1339 (Fed. Cir. 2004) ("A finding that two inventions were designed to resolve different problems . . . is insufficient to demonstrate that one invention teaches away from another."). The Patent Owner has not argued Takizawa suggests that the use of an ACBL terminal is unlikely to be productive of the result sought by the method of claim 1 of the '589 patent, nor has Patent Owner explained sufficiently why one of ordinary skill in the art would not look to Hoshino when Hoshino's method is similar to the prior art embodiment of Takizawa. *Compare* Ex. 1003, 15:42–16:9 & Fig. 11C *with* Ex. 1005, Fig. 4(l); *see* Ex. 1012 ¶ 70.

Patent Owner argues that Hoshino requires disfavored additional photolithography steps beyond the five allowed by the claims and, thus, one of skill in the art would not have looked to Hoshino in order to improve Takizawa. PO Resp. 53. As we explain above, Petitioner's instituted ground relies on Hoshino's teaching of an ACBL, rather than Hoshino's total process, thus, we are not persuaded by this argument.

Patent Owner suggests that an embodiment of Hoshino employs a lift-off procedure which, according to Patent Owner, is disclaimed. PO Resp. 53. Nevertheless, Petitioner does not rely on that embodiment for obviousness (*see* Pet. Reply 13); therefore, that argument lacks merit.

Patent Owner states that "a bare recitation that references [Takizawa and Hoshino] could be combined, without an explanation of how and why one of ordinary skill in the art would go about doing so to arrive at the claimed invention, is inadequate under the law to support a determination of obviousness." PO Resp. 55–56.

As noted above, we credit Petitioner's declarant who testifies that "the [a person of ordinary skill in the art] would know how to etch the ACBL contact hole and gate bus line contact hole in the same photolithography step because Hoshino provides an example of doing so." Ex. 1012 ¶ 70. Thus, Hoshino itself provides the "how" to achieve the claims limitation.

Based on the record developed during trial, Petitioner has shown by a preponderance of the evidence that claim 2 would have been unpatentable over Takizawa and Hoshino.

E. Anticipation of Claims over Hoshino

Petitioner asserts that claims 2, 3, and 6 are unpatentable under 35 U.S.C. § 102 as anticipated by Hoshino. Pet. 48. To support its contentions, Petitioner provides detailed explanations as to how Hoshino purportedly meets each claim limitation. *Id.* at 48–60. Petitioner also relies upon a Declaration of Dr. Chiang, who has been retained as a declarant by Petitioner for the instant proceeding. Ex. 1012.

In its Petition, Petitioner contends that Hoshino discloses forming gate electrodes and a gate bus line on a transparent insulating substrate. Pet. 49, 56; Ex. 1005 (multiple paragraphs and figures cited in Petition). Petitioner argues that Hoshino discloses forming a gate insulating film over the substrate and forming an operative semiconductor on the gate insulating film. Pet. 49–51, 56–57; Ex. 1005 (multiple paragraphs and figures cited in Petition). Petitioner further argues that Hoshino discloses forming source electrodes, drain electrodes, and a drain bus line of the TFTs on a gate insulating film and an operative semiconductor, and forming a protection film over the substrate. Pet. 51–52, 57; Ex. 1005 (multiple paragraphs and figures cited in Petition). According to Petitioner, Hoshino discloses removing a portion of both the gate insulating film and the protection film, located above a terminal of said gate bus line, and removing a portion of said protection film located above a terminal of said drain bus line and forming the pixel electrode on the substrate. Pet. 52–53, 57–58; Ex. 1005 (multiple paragraphs and figures cited in Petition).

We agree with and adopt Petitioner's analysis as summarized below. As to claim 2, Petitioner asserts that Hoshino discloses an auxiliary capacitive bus line formed on said substrate in facing relation to said pixel electrode with said gate insulating film therebetween, and wherein a portion of both said gate insulating film and said protection film, located above a terminal of said auxiliary capacitive bus line, is also removed in said step (f) of claim 1. Pet. 58–59 (multiple paragraphs and figures cited in Petition). As to claim 3, Petitioner asserts that Hoshino discloses that that gate insulating film is formed to have a multi-layered structure in said step (b) of

claim 1. Pet. 25 (multiple paragraphs and figures cited in Petition). As to claim 6, Petitioner asserts that Hoshino discloses that the pixel electrode is formed of indium tin oxide (ITO). Pet. 59–60 (multiple paragraphs and figures cited in Petition).

Patent Owner asserts "Hoshino teaches two separate metal deposition steps and two separate photolithography steps to accomplish singular step (a) of the '589 patent." PO Resp. 50. Patent Owner further asserts "Hoshino fails to disclose these two separate steps [for steps (c) and (d) of claim 1], which are specifically enumerated in the claims of the '589 patent." *Id.* at 49–50. Finally, Patent Owner asserts "in the second embodiment of Hoshino, in addition to six explicitly recited photolithography steps, further steps are required to form a polyimide film and subsequently remove *(i.e.*, etch) portions of it, *thus totaling seven photolithography steps.*" *Id.* at 50. Thus, according to Patent Owner, Hoshino performs more steps than required by claim 1. *Id.* at 55–56. Patent Owner's assertion in this regard is premised on us construing claim 1 to require only five photolithography steps. As we explained above in the claim construction section, we did not so limit this claim, thus, we are not persuaded by Patent Owner's argument. *See supra* Section II.A.1.

Patent Owner argues that claim 1 excludes the use of a lift-off procedure. PO Resp. 23–24. Patent Owner further argues, and Petitioner admits, that the first embodiment of Hoshino employs a lift-off procedure to for the pixel electrode. Pet. 49; PO. Resp. 44–45; Ex. 1012 ¶¶ 99. However, the second embodiment of Hoshino does not require a lift-off procedure. Pet. Reply 23; Ex. 1012 ¶¶ 99. Because Petitioner relies only on the second

embodiment of Hoshino (see generally Pet. 48–53; Pet. Reply 13), we are not persuaded by Patent Owner's argument.

Patent Owner does not address separately Petitioner's contentions and supporting evidence with respect to claims 2, 3, and 6. *See generally* PO Resp. 49–51. We have reviewed the proposed ground of anticipation Hoshino against claims 2, 3, and 6, and we agree with and adopt Petitioner's analysis. Based on the record developed during trial, Petitioner has shown by a preponderance of the evidence that Hoshino anticipates claims 2, 3, and 6.

III. CONCLUSION

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence: (1) claims 3, 5, and 6 of the '589 patent are anticipated by Takizawa; (2) claim 2 of the '589 patent would have been obvious over Takizawa and Hoshino; and (3) claims 2, 3, and 6 are anticipated by Hoshino.

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 2, 3, 5, and 6 of the '589 patent are held to be unpatentable; and

FURTHER ORDERED that, because this Final Written Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2015-01417
Patent 5,966,589

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